A Test Strategy for a Current Source Designed for Fast Field-Cycling Nuclear Magnetic Resonance

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***Abstract*— This article presents a novel structural test strategy for a single MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) source designed for Fast Field-Cycling Nuclear Magnetic Resonance (FFC-NMR) systems. The proposed methodology enables in-field fault detection during idle intervals or before experiment initiation, a critical step to ensure the reliability and validity of the experimental outcomes. The circuit under test is divided into two sections: low-power and high-power. Each one is evaluated using tailored analog testing techniques: OBT (Oscillation-Based Test) and direct current testing are applied to the low-power section, while transient analysis with DTW (Dynamic Time Warping) is used for fault detection in the high-power section. This approach achieves high fault coverage—93.7% for the low-power section and 100% for the high-power section—without requiring complex signal processing. The effectiveness of the method is validated through simulation studies complemented by experimental fault injection on a scaled-down prototype. The results demonstrate that this test strategy significantly enhances system reliability, offering a valuable contribution to the development of more robust and maintainable FFC-NMR instrumentation for scientific and industrial applications.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9952

***Index Terms*—Analog test, Current source, Design for test, Oscillation-based test, Scientific instrumentation.**

I. INTRODUCTION

FAST Field-Cycling Nuclear Magnetic Resonance (FFC-NMR) is a powerful technique gaining prominence in low-field Magnetic Resonance Imaging (MRI) [1], [2] and NMR Relaxometry [3]. Unlike conventional NMR systems that operate at a fixed, high magnetic field, FFC-NMR is a technique that measures the nuclear spin relaxation rate over a wide range of magnetic field strengths. This is achieved by rapidly switching the magnetic field through different intensities during a single experiment.

The ability to vary the magnetic field provides access to molecular dynamics occurring on slow timescales—information that is typically inaccessible to fixed-field NMR techniques. As a result, FFC-NMR has become a valuable tool for characterizing complex materials such as polymers, pharmaceuticals, and food products, as well as for studying contrast agents for MRI. FFC-NMR experiments require programmed magnetic field variations, which demand specialized sources capable of delivering high currents and fast switching times. Conventional implementations use high-power sources connected to low-resistance, low-inductance air-cored electromagnets or, less frequently, ferromagnetic-cored systems.

Conventional current source (CS) implementations often use multiple parallel MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), but uneven current distribution among transistors can lead to critical failures [4]. A single-semiconductor implementation solves this problem and is technologically viable for moderate currents (below 150 A). However, the selected MOSFET presents vulnerabilities, primarily from thermal instability during linear operation with high currents [5], and can suffer accelerated degradation from electrical, thermal, and mechanical stress. Thus, early fault detection becomes essential to ensure system reliability and prevent damage to equipment or risk to operators.

To address these concerns, this work proposes an in-field structural test methodology for a single-MOSFET current source designed for FFC-NMR systems. The strategy is intended to be executed either before an experiment or during idle intervals, with the goal of verifying that the circuit remains fault-free under real operating conditions. The Circuit Under Test (CUT) is partitioned into low-power and high-power sections, and each one is evaluated using tailored test techniques.

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II. RELATED WORK

A. Fault Detection in Low-power Circuits

In analog circuit testing, two main approaches are commonly used: functional (specification-based) and structural (fault-oriented). While the first verifies that the circuit meets its performance specifications, the latter focuses on detecting specific modeled faults using targeted stimuli. Structural test-

ing typically requires fewer resources and is more cost-effective than functional testing [6].

Structural testing primarily targets two types of faults: catastrophic faults, characterized by complete circuit failure usually due to events such as open and short circuits, and parametric or deviation faults, which manifest as performance degradation [7].

Structural tests share the same limitations as other analog test approaches [6], [8]. Specifically, component tolerances, nonlinear behavior, lack of standardized fault models, and signal complexity [9], [10]. These limitations often require test strategies tailored to specific circuits or families [6], [11]. As a result, applying a given methodology to a circuit often requires a specific implementation and validation.

A widely adopted structural method is Oscillation-Based Testing (OBT) [12]. OBT transforms the CUT into an oscillator by adding a nonlinear block in the feedback loop. Faults alter oscillation characteristics—such as amplitude or frequency—making them detectable. This technique eliminates the need for external test signal generators and simplifies measurement requirements, making it suitable for high-frequency applications and mixed-signal systems [13]. Specifically, the research performed in [14] demonstrated the usefulness of nonlinear oscillators for OBT implementation. Other authors explored the application of OBT to diverse systems using, in some cases, additional tools for targeting specific demands , , [15-17]. However, its application in a new circuit must be carefully evaluated because it requires the circuit to be divided into fundamental blocks for testing, which can lead to performance issues.

Another simple analog circuit strategy is Direct Current (DC) testing [8]. This strategy consists of stimulating the CUT with a DC stimulus and monitoring one or more circuit nodes. The strategy assumes that a fault alters the values of DC voltages, making the fault observable. This strategy complements OBT, improving the fault coverage values in this article.

A key feature of the proposed test strategy for the low-power section is its minimal signal processing overhead. Unlike methods that rely on complex spectral analysis or feature extraction from the entire transient response [18], our approach identifies faults by simply monitoring fundamental DC levels and global oscillation parameters, such as amplitude and frequency. This simplicity reduces computational requirements and facilitates a straightforward implementation.

B. Fault Detection in Power Circuits

Fault detection in power electronics is critical due to the risks associated with open-circuit (OC) and short-circuit (SC) faults, particularly in switching devices. These faults can lead to equipment damage, system failure, or safety hazards. As a result, numerous studies have focused on developing robust detection techniques.

Researchers explored various approaches for OC fault detection. Model-based methods, such as [19], compared measured and estimated capacitor voltages in multilevel converters. Hybrid approaches combine analytical circuit knowledge with signal processing. For instance, [20] analyzed current symmetry and harmonics in bidirectional converters, [21] utilized current sampling at specific points in interleaved boost converters, and [22] employed Kalman filtering on capacitor voltage measurements. [23] calculated the average current Park vector, and [24] selected specific signal measurements for IGBT and diode faults. Some authors detected faults using a model predictive control (MPC) already implemented in the system [25]. Additionally, other faults (SCs and OCs) were considered for detection [26-28].

While acknowledging the contributions of prior research, it is essential to note that most fault testing studies in power electronics primarily focus on circuits operating in switching mode. This research predominantly targets OC and SC faults in the switching devices themselves [29], [30]. This narrow focus simplifies circuit analysis, often enabling the derivation of analytical expressions for critical parameters. As a result, it diminishes fault detection complexity and facilitates the development of online testing or fault-tolerant systems.

Although relevant, this conventional approach presents two main shortcomings. It frequently overlooks faults in both passive and active components that can compromise system performance. Moreover, existing testing techniques have not proven effective for scenarios demanding linear or mixed-mode operation, such as the application discussed in this article.

Testing mixed-mode circuits with all their components introduces significant challenges in terms of observability and controllability [31]. Overcoming these barriers often requires additional test stimuli and monitoring points, and could result in increased hardware overhead compared to proposals that only targets faults in power devices.

III. Description of the Circuit under Test

This section describes the basic architecture of the CUT, a current source based on a single-MOSFET configuration. As shown in Fig. 1, it includes an air-core electromagnet designed for fast magnetic field modulation. Its low inductance and resistance allow rapid field transitions. A series-connected MOSFET controls current flow, while protection circuitry suppresses voltage spikes during turn-off, safeguarding both the transistor and the magnet. Current sensing is achieved using a precision shunt resistor and instrumentation amplifier, providing real-time feedback (Is) for control.

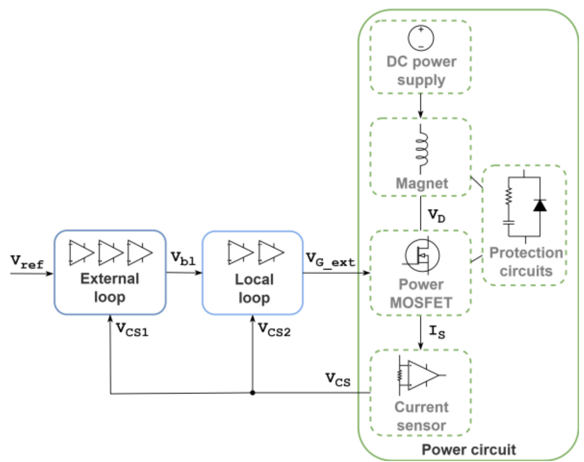


Fig. 1. General block diagram of the CS: a power circuit and a dual-loop controller that regulates the magnet current by adjusting the MOSFET's gate voltage based on Vref and Vcs.

While the topology adheres to standard design principles, its primary challenge is managing high current magnitudes through a single MOSFET. The selected transistor is optimized for switching applications and exhibits high gate voltage sensitivity, which complicates stable linear operation required for this application.

To address this limitation, the CUT incorporates a linearization circuit (local control loop) [32], which effectively compensates for the MOSFET's nonlinear behavior. This approach not only enhances device predictability but also simplifies the controller architecture. As a result, a single external loop regulates magnet current by treating the power stage and linearization circuit as a unified plant, using the feedback signal (Vcs) for closed-loop control. In Fig. 1, the signals Vcs1 and Vcs2 represent the connection from the current sensor output to the inputs of the external and local loops, respectively. Meanwhile, Vbl is the output signal of the external loop, which is injected as the reference for the local loop.

Given the magnet's specialized properties and the high cost of critical components, the system was scaled down to a lower-power version using the original DC power supply. This approach reduces experimental risks and aligns with methods used in prior work [32], [33]. The scaled prototype enables physical fault injection, which is essential for validating the proposed test strategies while ensuring safer operation during testing.

Scaling was achieved primarily by replacing the MOSFET with a device rated for lower current (thus limiting the maximum circuit current to 15 A) and by adjusting the controller parameters, while keeping the basic architecture intact. The magnet was preserved at its nominal value to retain the dynamic behavior of the full-scale system. This preserves functional consistency across scales and supports the preliminary evaluation of the proposed Design-for-Test (DfT) methodology. Simulations confirmed that, upon reintroducing the original high-current MOSFET, the system resumes correct operation with only minor adjustments to the controller. Specifications for the low-power and full-scale prototypes are compared in Table I.

TABLE I
FULL-SCALE AND LOW-SCALE PROTOTYPE PARAMETERS

Description	**Full-scale parameters**	**Low-scale parameters**
DC power supply	5 V	5 V
Limit current	150 A	15 A
Magnet	L=5 μH, R=19 mΩ	L=5 μH, R=19 mΩ
Power MOSFET	IXTN660N04T4	STD18NF03L
Current sensor	INA240	MAX4376H
Shunt resistor	0.1 mΩ	3.33 mΩ

Fig. 2 illustrates the schematic of the circuit, which is the same for both prototypes. The main component in the power circuit is the MOS transistor, protected by redundant circuitry: snubber, TVS (Transient Voltage Suppressor), and FD (Flyback Diode). The figure represents the magnet inductance (Lmagnet) with its resistance (Rmagnet). A special-purpose current-sense amplifier (Ucs) and Rshunt (with parasitic inductance Lshunt) are used to provide a voltage (Vcs) proportional to Is (and the current through the magnet when the MOSFET is on). Rcomp (compensation resistor) and Ccomp (compensation capacitor) are added to preserve the shape of the current transient.

The input voltages for the feedback loops (Vcs2 and Vcs1) are set to Vcs. U4, U5, and their associated circuitry implement the local loop, providing gain and integration effects. The actions performed by this circuit on the power section simplify the external loop, composed only of an error amplifier (U2) and a gain stage (U3). In addition, U1 and its associated components perform minor filtering and buffering of the signal denoted as Vcs2, necessary for reducing second-order effects (small oscillations after pulsing).

IV. TEST STRATEGY

A. CUT Partitioning and Selected Strategies

The CUT includes a power circuit whose operational principles differ significantly from the other sections, posing a considerable challenge for testing. Isolating this circuit during testing can enhance the controllability and observability of its

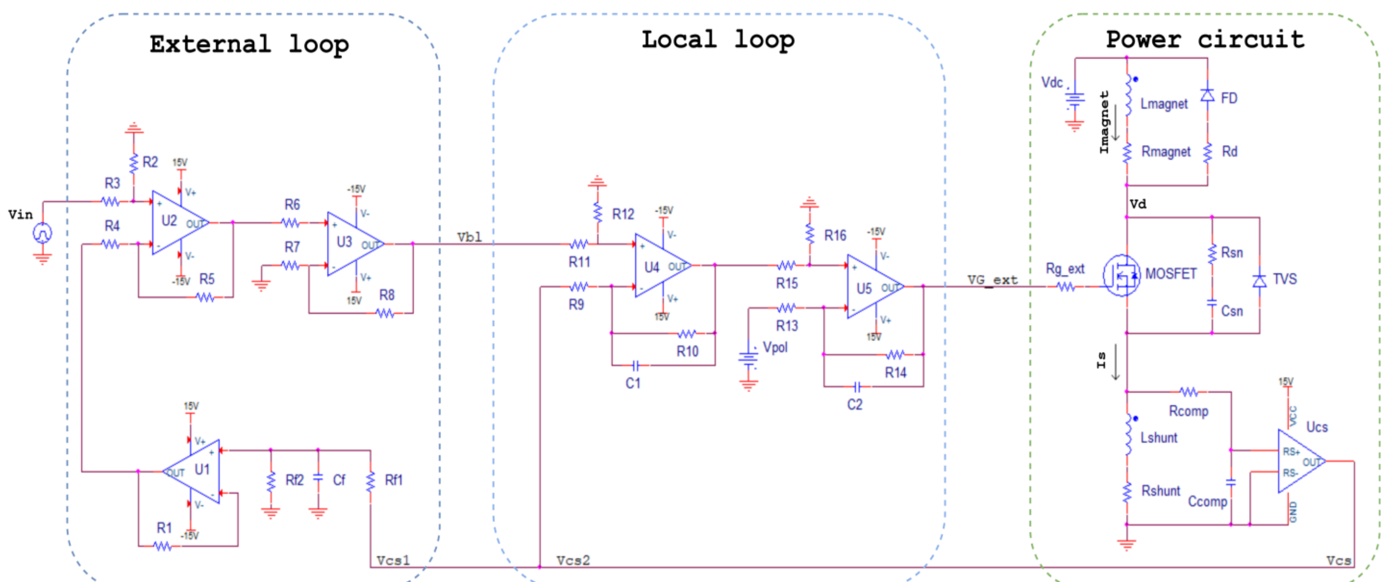


Fig. 2. Schematic of the circuit under test.

internal nodes. However, the MOSFET transistor is highly sensitive to variations in control voltage and exhibits thermal instability under certain operating conditions, making the test environment difficult to control.

Our proposal is to divide the test into sequential sessions. The first session tests low-power blocks (external and local loops) with the power section disconnected. The second one tests the high-power block with the local loop connected. This testing sequence ensures that the local loop is fault-free before testing the power section. In the following, we denote the connection of the low-power blocks as CUT_{LP} and the connection of the internal loop and power circuit as CUT_{HP}.

To implement the test sessions mentioned above, we added switches to isolate the blocks under test and to connect the test resources required for each of the test configurations (Fig. 3). Table II shows the switches position for each test configurations.

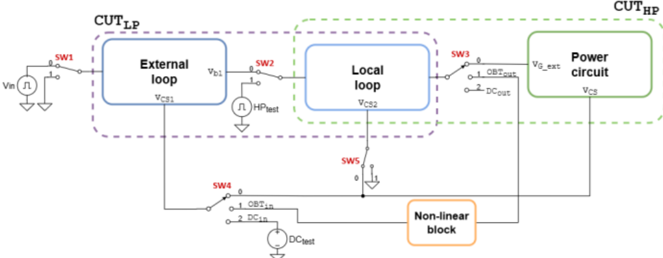


Fig. 3. DfT implementation for the current source. Switches are incorporated to partition the circuit and configure test modes.

TABLE II
SWITCH CONFIGURATION FOR EACH MODE OF OPERATION

Mode	SW1	SW2	SW3	SW4	SW5
a. Normal	0	0	0	0	0
b. OBT	1	0	1	1	1
c. DC test	1	0	2	2	1
d. HP test	1	1	0	2	0

For the CUT_{LP}, we propose a first test sub-session using OBT (Fig. 3 and Table 2.b configuration). In this case, we convert the CUT_{LP} into an oscillator by adding a nonlinear block (NLB) into the feedback loop.

To improve the fault coverage of CUT_{LP} given by OBT, we propose a complementary sub-session using a DC test strategy. This method consist of exciting the CUT with a DC input and measuring the output voltage (Fig. 3 and Table 2.c configuration).

Once these test sub-sessions are completed, the local loop is connected to the power circuit, and both sections (CUT_{HP}) are tested to detect faults in the power section. We propose a simple transient analysis of a single pulse for this session (Fig. 3 and Table 2.d configuration). The following sections present in-depth implementation details of each session.

The proposed DfT requires the switches' on-state resistance to be as low as possible and stable across temperature variations. The switches must also withstand the operational amplifiers' voltage (±15 V) and should not alter the dynamic behavior of the circuits under test. Their switching speed is not critical as they do only switch during the configuration of the test modes.

B. Test Validation

The techniques to validate structural test methods, such as those proposed here, typically employ fault injection and simulation procedures, allowing to inject faults that can be difficult or even impossible in real circuits [7]. In addition, these techniques facilitate early evaluations of the design for test, an essential aspect because DfT introduces additional circuitry that may compromise the performance in normal mode. Furthermore, early evaluations allow the optimization of test conditions before the final implementation of the circuit.

Implementing this type of evaluation requires a simulation model of the CUT that can represent the faults addressed by the test, as well as a convenient simulation platform. We adopt SPICE as the simulation platform because the SPICE models provided for CUT_{LP} are accurate and reliable. Furthermore, we implement the overall test circuitry for CUT_{LP} in the simulator without experimental implementation of the circuit. This aspect contributes to lowering the test development costs. It is worth noting that these conditions are no longer applicable when addressing the CUT_{HP} test. For this section, it was necessary to resort to experimental validations to complement the simulations, as explained later in this article.

V. LOW-POWER CIRCUIT TESTING

Test engineers often work with systems containing passive components and commercial integrated circuits (ICs), such as our CUT. For ICs, developing a structural test strategy is challenging due to the lack of internal design information. However, when ICs operate with negative feedback, as in our CUT, internal parametric faults typically result in negligible performance deviations. In contrast, catastrophic faults within ICs usually cause significant changes, which are easily detected by tests targeting external faults. Meanwhile, both catastrophic and parametric faults in passive components significantly affect CUT behavior, making them suitable targets for analog and mixed-signal test strategies. Therefore, our focus was on detecting faults in the passive components of the low-power sections of the CUT.

A. OBT Oscillator Design

OBT requires converting the CUT_{LP} into an oscillator. Research in [14] demonstrates that nonlinear oscillators are effective for OBT implementation. This approach involves adding a NLB to the feedback loop (Fig. 3 and Table 2.b configuration), enabling stable oscillation startup and amplitude control.

The NLB input-output relation is shown in Fig. 4.a. This block can be implemented using a comparator and analog multiplexer (Fig. 4.b). The CUT_{LP} output (OBTout) drives the multiplexer, which selects between ±Vref based on the input signal. The complete oscillator configuration is shown in Fig. 5, with switches omitted for clarity.

To analyze the oscillator, the Describing Function Approach (DFA) is used, which is especially effective when the CUT exhibits low-pass or band-pass behavior [34]. DFA approximates the nonlinear element with an equivalent gain and phase, allowing linear design techniques to be applied.

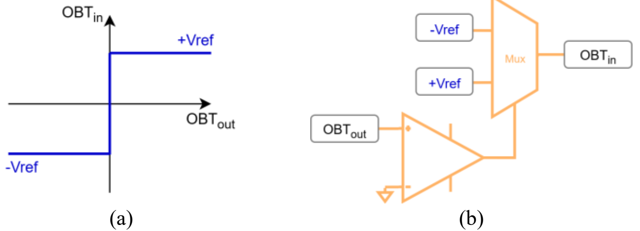


Fig. 4. NLB: a) input-output relation, b) connection to the CUT_{LP}.

Using DFA, the equivalent gain of the NLB is expressed as (1), where A is the oscillation amplitude:

$$N(A) = 4V_{ref}/(\pi A). \quad (1)$$

N(A) enables the application of Bode plots to determine the oscillation conditions. Once the critical points are identified in the Bode diagrams, it is only necessary to provide the required gain to force the oscillation by adjusting the value of N(A).

Following the aforementioned procedure, high Vref values were required; however, increasing R8 to 500 kΩ boosted the CUT_{LP} gain, thereby reducing the demand on the NLB. Fig. 6 depicts the resulting Bode plot, where the vertical green line indicates the critical point. Under these conditions, the oscillations can be established at 4.37 MHz by providing an additional gain of 7.22 dB. Since the analog multiplexer supports up to 3.3 V, a noninverting amplifier (U8) was added to achieve the desired amplitude. The final parameters are MUX_{Vref} = 3 V and $U8_{Gain}$ = 2.2.

The simulation model of the complete oscillator, including the NLB (Fig. 5), exhibits a stable oscillation at 3.8 MHz with an amplitude of 4.6 V. The discrepancy between these simulated values and the DFA predictions is attributed to a non-ideal delay between the zero-crossing of the NLB's input (OBTout) and the corresponding transition at its output (OBTin), which can be modeled as a hysteretic response that was not accounted for in the initial DFA-based analysis.

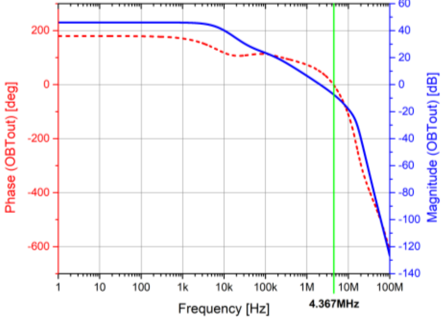


Fig. 6. The Bode plot of the transfer OBTin/OBTout to establish the oscillation condition. In blue is the magnitude (dB), and in red is the phase (degrees). The green line marks the critical point.

B. DC Test Setup

For this test, a DC voltage is connected to the input of CUT_{LP} in an open-loop configuration (Fig. 3 and Table 2.c configuration). The voltage used in the test is approximated by simulation. DCtest = 0.5 V is selected to obtain a voltage level close to half the operating range of the operational amplifier U5 at the output of the CUT. A measurement sensitivity of 10 mV is required for reliable fault detection. This threshold is derived directly from the performed fault coverage analysis, in which fault-induced deviations were resolved with a precision of two decimal places.

C. Fault Dictionary Considerations

Evaluating test efficiency requires the construction of a fault dictionary that enumerates the faults to be detected. For the passive components of the CUT_{LP}, we consider single catastrophic and deviation faults.

To assess the effectiveness of the proposed test strategies, we formulated a fault dictionary of catastrophic faults (OCs and SCs) and deviation faults of ±30% and ±50% in the passive components of the CUT_{LP}. This leads to a dictionary

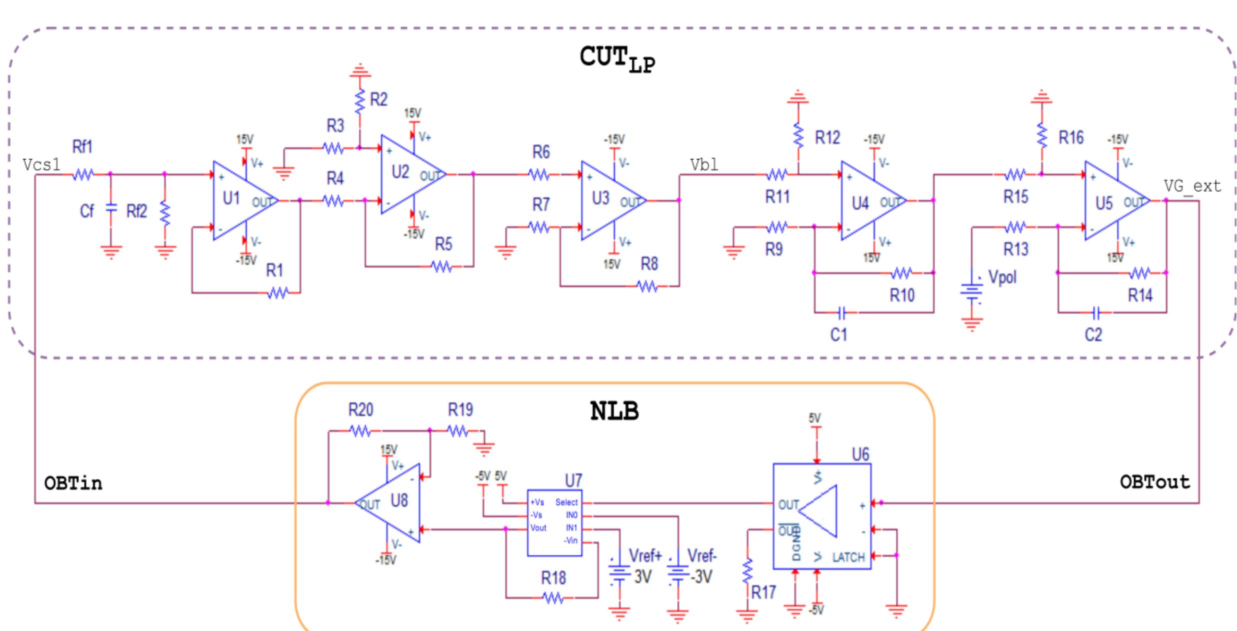


Fig. 5. Schematic of the CUTLP configured for OBT, incorporating the NLB used to force the circuit to oscillate.

containing 127 faults, to be injected in eighteen resistances and four capacitors (Cf in Fig. 2 is implemented with two capacitors of 380 pF in a series connection).

D. Tolerance of the Test Parameters

The test strategy evaluation requires estimating parameters variability during the testing process. While Monte Carlo simulations are typically used to model variations within component tolerances, they are less critical here, as the test targets a unique research instrument, eliminating the need to validate across multiple prototypes.

A potential concern is the thermal drift of test signals. A worst-case temperature variation of 10°C is considered, with a focus on passive components, following the same considerations as in the previous section. Resistance and capacitance (np0 capacitor) changes in the low-power circuit are linear over this range. The worst-case variation in the test parameters due to temperature drift is less than 0.5%, which is considered negligible for our application. Another factor that could affect measurements accuracy is noise. However, this is mitigated through signal averaging performed by the oscilloscope.

Given the minimal impact of noise and thermal drift, conservative tolerances of 5% for OBT and 2% for DC measurements are adopted. During fault simulation, if any parameter exceeds these limits, the fault is declared detected.

Specifically, for OBT, the first 25 µs of the CUT simulation (under faulty and fault-free conditions) are processed in Matlab, obtaining the amplitude (positive and negative) and frequency of the oscillations. Fig. 7 shows the CUT fault-free output response (nominal) and with selected faults in resistors that cause detectable changes in amplitude or frequency.

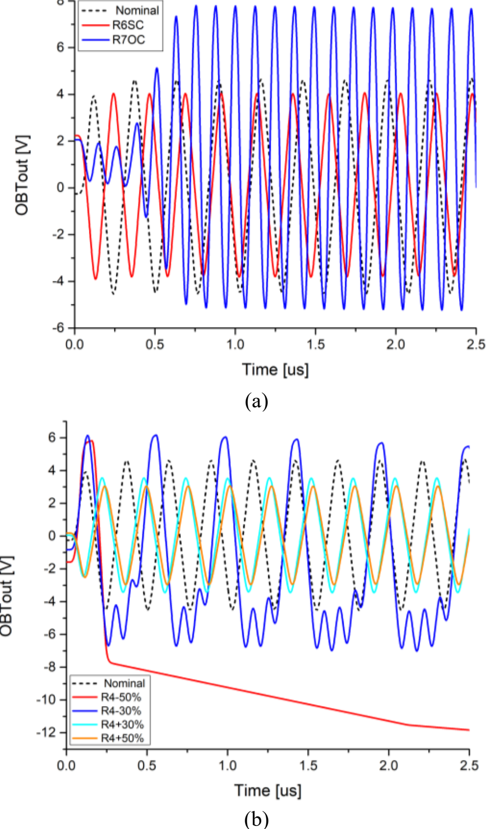


Fig. 7. a) CUT output, nominal and with catastrophic faults in R6 and R7. b) CUT output, nominal and with deviations faults in resistor R4.

E. Fault Simulation Results

The fault simulation process achieves a fault coverage of 93.7%, with only 8 undetected faults (±30% and ±50% deviations on capacitors C1 and C2).

To evaluate how the undetected faults affect the behavior of the overall system, we injected them into the complete system (with the external loop connected). This way, the circuit is exercised in normal mode for input signals of 1 V, 2 V, and 3 V, covering a wide range of output currents. During fault simulations, we monitored the current in the magnet. The results showed that the impact of the undetected faults is negligible. Considering the marginal effects of the undetected faults on the system performance, it is concluded that the fault coverage obtained by our approach (OBT + DC test) meets the requirements for effective fault detection.

VI. Power Circuit Testing

A. Test Proposal

The second test session addresses the high-power section once the low-power circuit test verifies the fault-free condition of the CUT_{LP} (Fig. 3 and Table 2.d configuration). The test involves applying a pulse to the CUT_{HP} and analyzing the resulting transient response, composed of: the current sensor output (Vcs) and the voltages at the gate and drain terminals of the MOSFET (Vg and Vd, respectively). We use a square pulse as input to ensure the test exercises all the power section components, including the protection devices.

The pulse duration is a tradeoff between the time required to observe the on and off transients and the steady-state conditions, and the need to protect the power devices from dangerous self-heating effects. For the same reason, the high pulse value is only the minimum required to exercise all the MOSFET conditions. Following these considerations, we establish the input pulse with an amplitude of 2 V, an on-state duration of 100 µs, and a signal period of 1 ms.

We consider the overall output waveforms and compare them with those obtained under fault-free conditions. To this end, we employ the elastic similarity measurement known as Dynamic Time Warping. DTW finds an optimal path with a minimal value between two time series and enables the comparison of test responses from multiple sources under different conditions [24]. In the operative phase of the test, we use DTW to compare two time series: a fault-free pattern, obtained from the circuit operating under typical test conditions (nominal response), and the CUT test response. A fault is detected if the DTW distance measure exceeds a pre-established threshold [35].

Specifically, we propose calculating three DTW distances for each test output. To achieve this, each signal is divided into three consecutive 50 µs intervals. This approach allow us to evaluate three of the most representative characteristics of the response: the off-to-on transient (T1 = 0–50 µs), the steady-state regime (T2 = 50–100 µs), and the on-to-off transient (T3 = 100–150 µs).

The experiments described below were conducted using an Agilent 33220A function generator to provide the input pulses to the CUT_{HP}. The circuit's transient responses were captured by a digital oscilloscope Tektronix TDS2014C (100 MHz bandwidth), with the signals sampled at 10 MSa/s. To accom-

modate the distinct voltage ranges of the monitored nodes, the oscilloscope's full-scale vertical range for each channel was configured individually: 8 V for Vg, 4 V for Vcs, and 16 V for Vd.

B. Variability of the Test Signals

The effect of temperature was considered in a characterization campaign, where the MOSFET case temperature was varied from 25°C to 45°C through adjustments to the test signal period. Then, we collected 100 test signals across the temperatures in the range, with each signal averaged over 128 oscilloscope acquisitions to mitigate the noise. The results show that the variability of the signals at the three test points proposed in this article are negligible over the considered temperature range. For this reason, we disregard it in the following. Instead, we consider that noise and discretization in the instruments are the primary sources of variability in the test signals.

Based on the above, the DTW thresholds are obtained using the following procedure [35]:

- A collection of 40 test signals from fault-free circuit is experimentally obtained. Each one is the result of averaging 128 signals in the oscilloscope.
- The test signals are averaged to obtain a pattern signal.
- The DTW distances are calculated for each test signal and the regions proposed (T1, T2, and T3).
- A maximum of the obtained value for each interval is preliminarily adopted as the distance threshold.
- A safety margin of 25% is adopted to avoid false positives (fault-free circuits declared faulty).

C. Fault Dictionary

As mentioned, the test performance evaluation requires a fault injection, which could be simulated or physically implemented. Consequently, defining a fault model and a procedure to estimate the fault coverage is necessary.

Many of the fault detection strategies proposed in the literature target catastrophic faults in the active components of the power circuits. In this article we adopt the same approach, focusing on single catastrophic faults, but extend the fault injection to all circuit components. Table III constitutes the fault dictionary employed to evaluate the test proposal.

TABLE III
FAULT DICTIONARY FOR CUT_{HP}, WHICH DETAILS THE ADDRESSED FAULTS AND THEIR ASSIGNED ALIASES

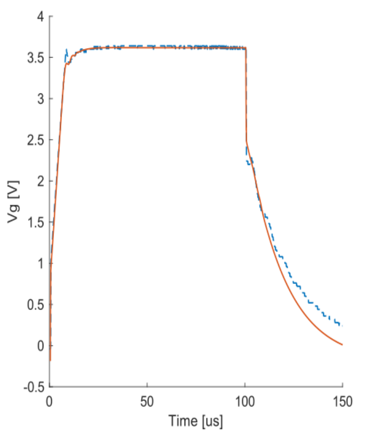
Component	Fault	Alias	Component	Fault	Alias
MOSFET	Gate OC	f1	Rsn	SC	f14
MOSFET	Drain OC	f2	Csn	OC	f15
MOSFET	Source OC	f3	Csn	SC	f16
MOSFET	G-D SC	f4	Rshunt	OC	f17
MOSFET	G-S SC	f5	Rshunt	SC	f18
MOSFET	D-S SC	f6	Rcomp	OC	f19
TVS	OC	f7	Rcomp	SC	f20
TVS	SC	f8	Ccomp	OC	f21
FD	OC	f9	Ccomp	SC	f22
FD	SC	f10	Magnet	OC	f23
Rd	OC	f11	Magnet	SC	f24
Rd	SC	f12	Rg_ext	OC	f25
Rsn	OC	f13	Rg_ext	SC	f26

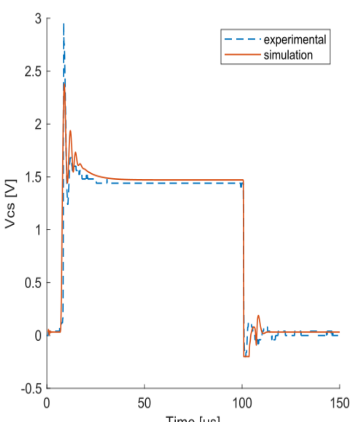
For the MOS device, we considered all possible single SC and OC in its terminals. Additionally, we consider faults in the magnet and shunt resistor terminals. On the other hand, the fault injection process does not consider the current sensor due to the lack of a structural simulation model for this purpose. In this sense, the considerations regarding catastrophic faults in the operational amplifiers of the CUT_{LP} (Section 5) also apply here.

D. Proposal of a Mixed Fault Injection Process for CUT_{HP}

It is possible to implement a fault simulation process to estimate the CUT_{HP} test performance, as done for the CUT_{LP}. Nevertheless, the simulation models of the MOSFET (and the other power devices) might not match the circuit behavior.

To evaluate the difference between the simulation and the real circuit, we physically implemented the CUT_{HP} in the laboratory. This is the plant controlled by the external loop and the primary source of divergences between simulation and experimental outcomes. On the other hand, the SPICE simulation of the CUT_{HP} employed the models provided by the vendors and included the effects of the parasitic inductances of wires. The remaining parts of the CUT are simple circuits that do not pose a challenge for simulation, as they have realistic simulation models provided by the vendors and operate with negative feedback. For these reasons, they were not included in the experimental validation.





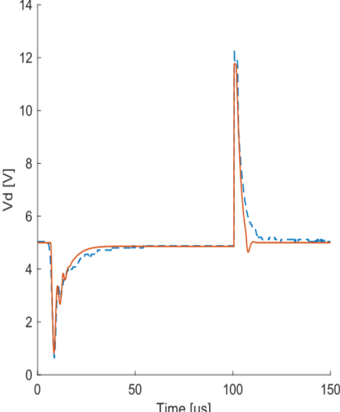


Fig. 8. Simulated versus experimental outputs.

Fig. 8 compares the simulated against the experimental CUT_{HP} outputs for a 2 V pulse amplitude. The figure shows that the simulated outputs reasonably match with the experimental ones. Therefore, we conclude that the model is similar enough to design and evaluate the overall system. However, using this model presents drawbacks from a testing standpoint due to the divergences observed in regions of the transient response, which raises concerns about the validity of a transient analysis test based solely on simulation. We propose a combination of simulation-based and experimental fault injection procedures for the test validation.

Although an entirely experimental fault injection procedure is feasible in principle, some of the considered catastrophic faults could cause irreversible damage to the CUT_{HP}.

To prevent damaging the device, we implemented a two-step procedure. The first step involves injecting and simulating all the considered faults in SPICE. Then, we identify the faults that produce severe effects in the circuit as they are easily detectable. In the second step, we identify faults that cause deviations where the simulation model exhibits divergences compared to the real circuit. Then, those faults are experimentally injected into the circuit to avoid distorting the fault coverage evaluation. This way, we protect the CUT_{HP} from the effects of dangerous faults while overcoming the limitations of the simulation model.

E. Fault Simulation and Selection of Faults for Experimental Injection

The simulation uses a 1 mΩ resistor to emulate a short circuit and a 1 MΩ resistor to represent an open circuit, avoiding convergence-related issues. We considered all the faults in Table III.

Faults f1 to f6, f8, f17 to f19, and f22 to f25 show behaviors significantly different from the fault-free simulation. Fig. 9 shows the three monitored outputs for the faults f1 to f6 and f8, which are faults in the semiconductors. Fig. 10 reports simulation results for the faults f17 to f19 and f22 to f25, which are faults in the passive components.

The remaining faults produced changes in regions where the simulation model diverges from the experimental results. For this reason, we resort to experimental fault injection to obtain significant test performance metrics.

The experimental fault injection requires the removal of connections in the board to introduce open-circuit faults or the addition of jumpers to emulate short-circuit faults. For consistency with all fault injection procedures, the oscilloscope captures and averages 128 signals to obtain a test signal for each considered fault.

The test showed that all the injected faults produced outputs that were slightly different from the fault-free ones and very different from the catastrophic behaviors observed in Fig. 9 and 10. Due to space constraints, we present in Fig. 11 just one of the results obtained in the laboratory. The figure shows that the faulty outputs differ from the nominal one where the simulation is inaccurate (mainly during the on and off transients), justifying the experimental fault injection.

F. Fault coverage results

After the fault simulation and experimental fault injection process, we compare the DTW distances at the three intervals

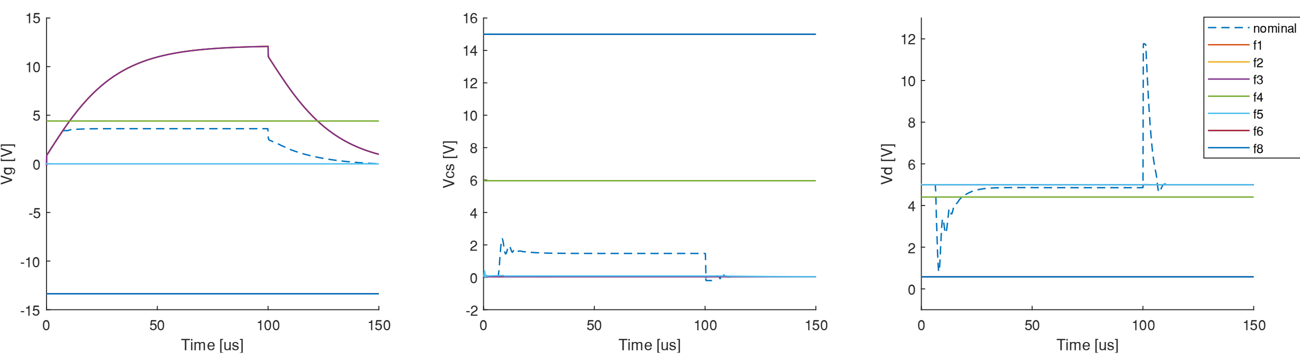


Fig. 9. Simulation results for f1 to f6 and f8 faults (semiconductor devices).

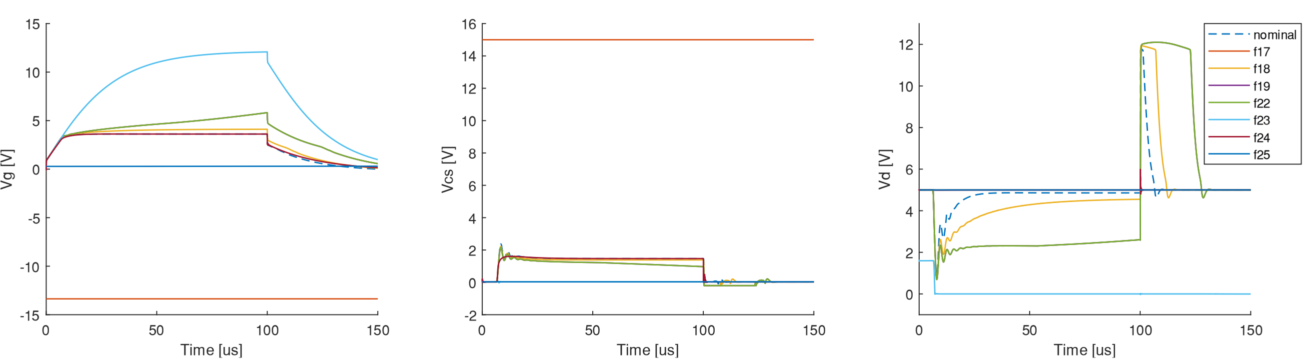
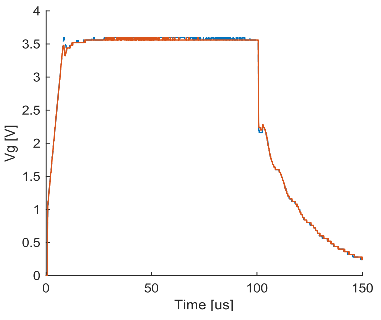
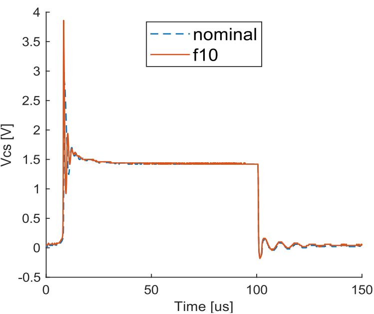


Fig. 10. Simulation results for f17 to f19 and f22 to f25 faults (passive devices).





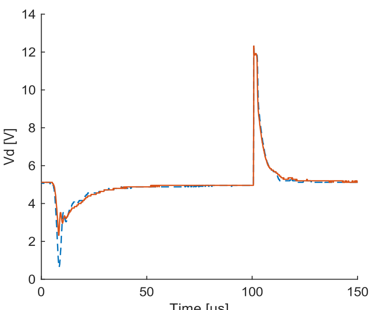


Fig. 11. Experimental fault simulation results, fault f10.

of the signals (T1, T2, and T3) with the signals obtained from fault-free conditions, using a 25% margin to prevent false positives. The faults that exhibited behaviors different from those of fault-free systems were all detected. Table IV shows the results for the remaining faults. In the table, we mark an x if the DTW distance of the faulty signal is higher than that of the fault-free one (and the fault is detected).

By analyzing the voltage signals in all specified time regions (T1, T2, and T3) at the monitored nodes (Vcs, Vg, and Vd), the proposed test effectively detects all induced faults. Consequently, the achieved FC is 100% for the set of faults under consideration.

TABLE IV
SUMMARY OF EXPERIMENTAL FAULT DETECTION RESULTS. AN 'X' INDICATES THAT A FAULT WAS DETECTED BY THE ANALYSIS OF THE CORRESPONDING PARAMETER

Fault → **Parameter↓**	**f7**	**f9**	**f10**	**f12**	**f13**	**f14**	**f16**	**f20**	**f21**	**f26**
VcsT1			x			x	x	x		
VcsT2		x	x			x	x	x		
VcsT3	x	x	x	x	x	x	x	x	x	x
VgT1	x	x	x		x	x	x	x	x	x
VgT2		x		x	x		x	x		
VgT3	x	x		x			x	x		x
VdT1	x	x	x	x	x	x	x	x		x
VdT2	x					x		x		
VdT3	x	x	x	x	x	x	x	x		x

VI. CONCLUSIONS

This article presents an efficient solution for in-field testing of a single-MOSFET FFC-NMR CS, a problem previously unaddressed in the literature. Furthermore, our proposal successfully addressed the challenges posed by the heterogeneous nature of the system under test, which is composed of low-power and high-power sections with significant differences in their operational principles.

The validation methodology was another significant contribution of the article, which combined experimental and simulation-based fault injections to provide a robust metric of fault coverage. The characterization campaign shows excellent results with high FC values. It is worth noting that the undetected faults had a negligible effect on the variable of interest.

By enabling early fault detection, this methodology contributes to more robust, safe, and maintainable instrumentation, reducing downtime and preventing costly damage due to undetected failures. Moreover, the design-for-test enhancements introduced can be adapted for use in other analog and power circuits employed in industrial and scientific environments.

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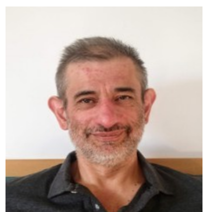

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