A High Step-up Dual-switch Luo Non-isolated DC-DC Converter with Fault-tolerant Capability for Critical Load Applications

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***Abstract*—This article presents a high step-up dual-switch Luo non-isolated DC-DC converter designed for critical load applications, which ensures fault-tolerant capability. The proposed converter offers several advantages, including increased voltage gains with a reduced duty cycle, common grounding between the source and load, a lower component count, and decreased voltage and current stress. In addition, it has reconfiguration capability and reduces the power handling demands on devices, thus enhancing overall converter efficiency. The performance characteristics of the proposed converter are analyzed in continuous current mode (CCM), with a detailed discussion of its features. Experimental results validate the effectiveness and feasibility of the proposed converter at an output power of 400 W.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9718

***Index Terms*—Common grounding, critical loads, high voltage gain, reduced voltage stress, reconfiguration capability.**

I. Introduction

MODERN critical loads such as aerospace, biomedical applications, telecommunication, data-centers, and electric vehicles demand reliable and efficient high voltage gain DC-DC converters. Even conventional boost converters provide high voltage gain at higher duty cycles, but suffer various drawbacks, including a reverse recovery time of the diodes, increased conduction losses, and increased voltage stress, which limits their applicability in critical loads. Many converter topologies are reported in the literature with the goal of maintaining a lower duty cycle for adequate higher voltage gain. A modified SEPIC converter explored in [1], allows a high voltage gain over a traditional boost converter. In [2], a topology is introduced with a voltage gain of (5+D)/(1-D), where "D" represents the duty cycle. Both converters in [1] and [2] encounter similar issues such as pulsating input current, requiring a high-duty cycle for high voltage gain, and not being able to offer common grounding. In [3] and [4], quadratic boost converters are explored where these converters produce high voltage gain for a duty ratio exceeding 70%, operating at high duty cycles, resulting in core saturation. In [5], a passive switched-inductor and capacitor network is examined, utilizing more components without providing a common ground, resulting in a discontinuous input current. To overcome this drawback, converters with higher voltage gain at lower duty cycles are explored in the literature. In [6]-[9], it explores the quasi-Z-source (QZS) and Z-source (ZS) networks integrated along with switched capacitors, switched inductors, and voltage boosting techniques, which are used to increase the voltage gain. The converters in [6] and [8] exhibit a lower voltage gain while incurring high voltage stress on the converter components. The converter configurations proposed in [7] and [9] achieve a higher voltage gain at the expense of an increase in component count. In addition, a dual switch-based configuration with switching capacitors and a booster network is explored to improve voltage gain in [10]-[14]. However, this converter suffers from several issues such as pulsating input currents, high voltage stress, a large number of components count, and common grounding.

In the past decade, significant attention has been focused toward the development of fault-tolerant configurations to improve the reliability of converters. The integration of fault-tolerant and diagnostic techniques is explored to improve the reliability of the converter in [15]-[17]. However, enhancing reliability often inadvertently increases the cost of the converter due to redundant components. Reliability challenges in converters arise predominantly due to the failure of passive components and switches [18]. Maintaining a balance between cost reduction, efficiency optimization, and reliability enhancement remains a challenge. In converter malfunction scenarios, especially critical loads applications need fault-tolerant capability [19] for converters. As a result, DC-DC converters designed for these applications are incorporated with fault-tolerance to ensure the provision of partial or full power to the load [20]. Various fault-tolerant DC-DC converters are explored in [21]-[31], but these converters typically exhibit low voltage gain, lower efficiency, and increased voltage stress in the normal and fault operation of the converter.

To overcome these issues, a high step-up dual-switch Luo DC-DC converter is designed and developed for critical load applications to achieve higher voltage gain at a lower duty cycle, low component count, minimized voltage and current stress, reconfiguration capability, common ground, and reduced electromagnetic interference (EMI). The main drawback of the proposed converter topology is that an equal amount of current flow through the switch and diode during fault operation leads to increased conduction losses, reducing overall efficiency.

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II. Operational Principle and Performance Characteristics

A. Operational Principle

The proposed high step-up dual-switch Luo non-isolated DC-DC converter with fault-tolerant capability is shown in Fig. 1. This onsists of 1-inductor (L), 2-MOSFETs (S_{w1-2}), 5-capacitors (C_{1-5}), and 6-diodes (D_{1-6}). The arrangement of components in such a way that it provides higher voltage gain with reduced duty cycle, while minimizing voltage stress and ensuring a common ground. To examine the performance of the converter in continuous conduction mode (CCM), it is assumed that all components are ideal.

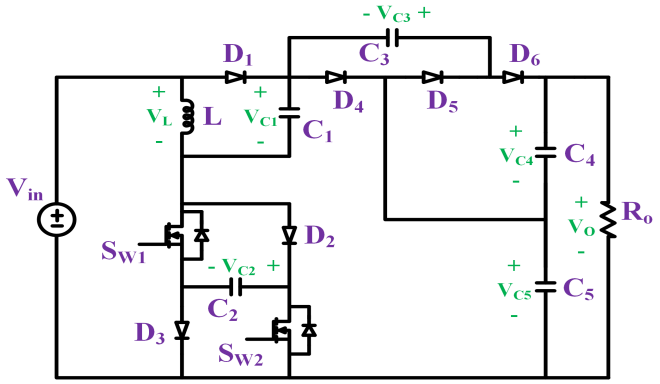


Fig. 1. Proposed converter with fault-tolerant capability.

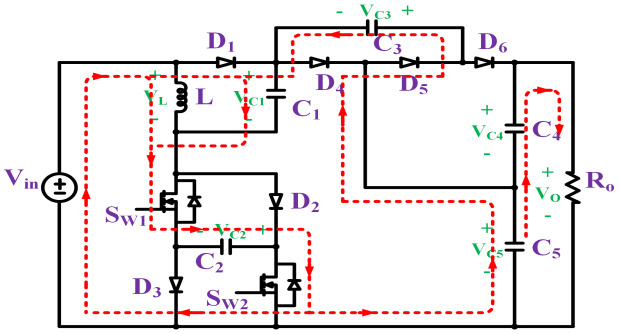


Fig. 2. Current flow during mode-1 operation.

1) Mode 1 {0–DT_S}: In this mode, S_{w1}, S_{w2}, D_1 and D_5 are in conduction, and D_2, D_3, D_4 and D_6 are OFF as shown in Fig. 2. The source voltage (V_{in}) charges L, C_1, C_2, and C_3. The C_2 and C_5 charge C_3, while C_4 and C_5 discharge through load. The voltage equations are obtained by applying Kirchhoff's law and are as follows:

$$\begin{cases} (V_L = V_{in} + V_{C2} = V_{C1}) \\ (V_{C1} + V_{C3} = V_{C2} + V_{C5}), (V_o = V_{C4} + V_{C5}) \end{cases} \tag{1}$$

2) Mode 2 {DT_S–T_S}: In this mode, S_{w1}, S_{w2}, D_1 and D_5 are OFF and D_2, D_3, D_4 and D_6 are in conduction, as shown in Fig. 3. The voltage V_{in}, L, and C_1 discharge through C_5 and C_2. The C_4 discharge through C_3. Fig. 4 shows the typical operating waveforms of proposed converter. The voltage equations are obtained by applying Kirchhoff's law and are as follows:

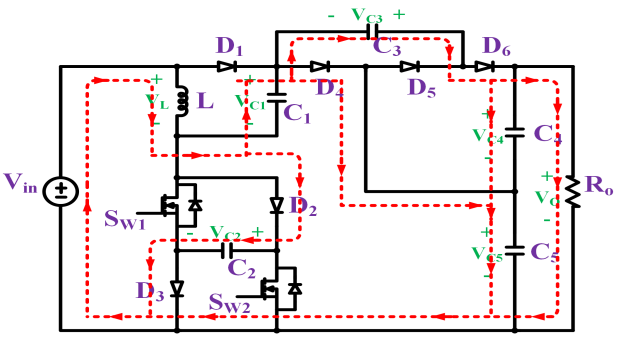


Fig. 3. Current flow during mode-2 operation.

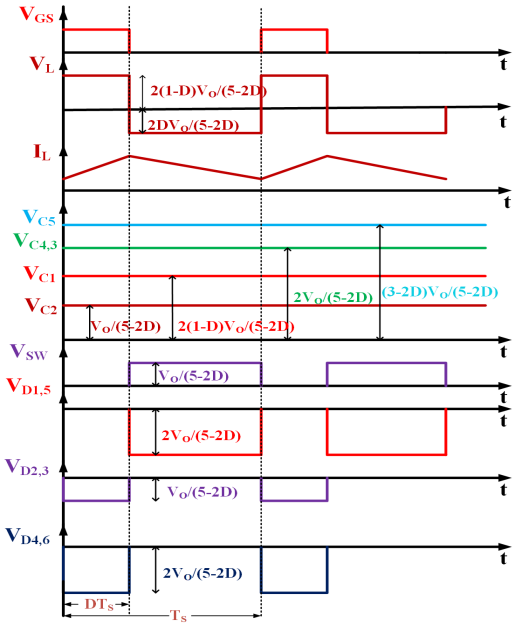


Fig. 4. Typical waveforms of proposed converter (a)V_{GS}, (b)V_L, (c)I_L, (d)V_{C1-5}, (e)V_{SW}, (f)$V_{D1,5}$, (g)$V_{D2,3}$, (h)$V_{D4,6}$.

$$\begin{cases} (V_L = V_{in} - V_{C2}), (V_{C1} + V_{C2} = V_{C5}) \\ (V_{C3} = V_{C4}), (V_o = V_{C4} + V_{C5}) \end{cases} \tag{2}$$

B. Voltage Gain Conversion Ratio

Apply the voltage-sec balance across the inductor.

$$\int_0^{DT_S} (V_L) = -\int_{DT_S}^{T_S} (V_L) \tag{3}$$

From eq. (1) and eq. (2). we get

$$\begin{cases} V_{C1} = \left(\frac{2(1-D)V_{in}}{(1-2D)}\right), \quad V_{C2} = \left(\frac{V_{in}}{(1-2D)}\right) \\ V_{C3} = V_{C4} = \left(\frac{2V_{in}}{(1-2D)}\right) \text{ and } V_{C5} = \left(\frac{(3-2D)V_{in}}{(1-2D)}\right) \end{cases} \tag{4}$$

The voltage gain of the converter is expressed as follows.

$$M_{CCM} = \left(\frac{V_o}{V_{in}}\right) = \left(\frac{5-2D}{1-2D}\right) \tag{5}$$

C. Inductor Current

Consider that the converter is ideal.

$$V_o I_o = V_{in} I_{in} \tag{6}$$

During normal operation, the current through the inductor can be described as follows.

$$I_L = \left(\frac{4I_o}{1-2D}\right) \tag{7}$$

The current flowing through an inductor can be described using eq (1):

$$L * \frac{di}{dt} = (V_{in} + V_{C2}) \tag{8}$$

The peak-to-peak ripple in the inductor current can be calculated using the following equation:

$$\Delta I_L = \left(\frac{V_{in} + V_{C2}}{L}\right) DT_S \tag{9}$$

D. Calculation of Inductance

To calculate the required inductance value, rewrite the above eq. (9) for L, as follows:

$$L = \left(\frac{V_{in} + V_{C2}}{\Delta I_L}\right) DT_S \tag{10}$$

The peak-to-peak current can be expressed in relation to the average current of the inductor.

$$\Delta I_L = x\%\ of I_L \tag{11}$$

where x represents the allowed percentage of ripple.

It is possible to calculate the value of inductance as follows.

$$L = \left(\frac{V_{in}(1-D)^2 D}{x\%2I_o F_s(1-2D)}\right) \tag{12}$$

Where F_s = switching frequency.

E. Voltage Stress of Components

Voltage stress occurs when active devices are reverse biased or turned off. Consequently, it is necessary to calculate the voltage stress in all of these devices.

In mode-1 operation, D_2, D_3, D_4, and D_6 are OFF as shown in Fig. 2. The voltage across $V_{D2} = V_{D3} = V_{C2}$, $V_{D4} = V_{C3}$ and $V_{D6} = V_{C4}$. In mode-2 operation, S_{w1}, S_{w2}, D_1, and D_5 are OFF as shown in Fig. 3. The voltage across $V_{Sw1} = V_{Sw2} = V_{C2}$, $V_{D1} = V_{C1} + V_{C2} - V_{in}$ and $V_{D5} = V_{C3}$. Table I shows the voltage stress across the devices.

TABLE I
NORMAL OPERATION VOLTAGE STRESS

Device	Voltage stress	Device	Voltage stress
$S_{w1,2}$	$\left(\frac{V_o}{5-2D}\right)$	D_1,D_4	$\left(\frac{2V_o}{5-2D}\right)$
D_2,D_3	$\left(\frac{V_o}{5-2D}\right)$	D_5,D_6	$\left(\frac{2V_o}{5-2D}\right)$

F. Current Stress of Components

The RMS current stress of semiconductor devices is as follows.

$$\begin{cases} I_{sw1} = I_{sw2} = \frac{2I_o}{(1-2D)\sqrt{D}}, \\ I_{D1} = \frac{(1+D)I_o}{\sqrt{D}}, I_{D5} = \frac{I_o}{\sqrt{D}}, \\ I_{D2} = I_{D3} = \frac{2I_o}{(1-2D)\sqrt{(1-D)}}, \\ I_{D4} = I_{D6} = \frac{I_o}{\sqrt{(1-D)}} \end{cases} \tag{13}$$

III. FAULT REDUNDANCY AND VOLTAGE CONVERSION GAIN

The proposed converter can be reconfigured during faults without additional components to provide redundancy by using one switch at a time, while also allowing for voltage gain conversion, as explained in detail below.

A. Fault Redundancy

The following is a comprehensive discussion of converter fault-tolerant operation in various potential scenarios.

Case-1: When S_{w2} is open circuit:

In this case, the converter functions in two modes within one switching cycle.

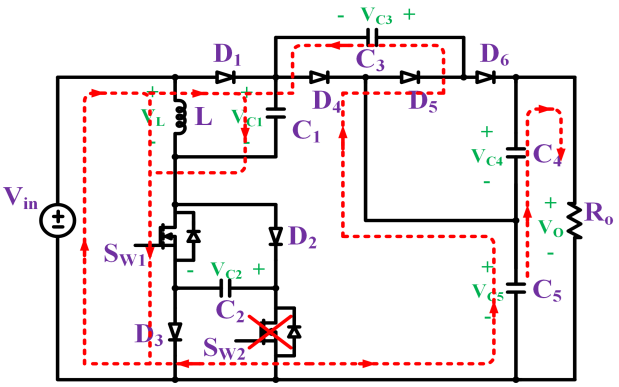


Fig. 5. Current flow (S_{w2} fails) during mode-1 operation.

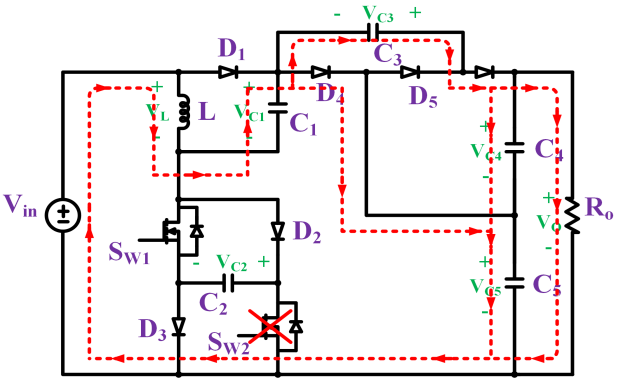


Fig. 6. Current flow (S_{w2} fails) during mode-2 operation.

1) Mode 1 $\{0$–$DT_S\}$: In mode-1, S_{w1}, D_1, D_3, and D_5 are in conduction, while D_2, D_4 and D_6) are OFF. The current flow in mode-1 operation while S_{w2} fails is shown in Fig. 5. The voltage V_{in} energizes C_1 and L and C_5 charge C_3. While C_5 and C_4 discharge to the load simultaneously. The voltage equations are derived by applying Kirchhoff's law and are as follows:

$$\begin{cases}(V_L = V_{in} = V_{C1}) \\ (V_{C4} = V_{C1} + V_{C3}), (V_o = V_{C4} + V_{C5})\end{cases} \tag{14}$$

2) Mode 2 $\{DT_S$–$T_S\}$: In this mode, S_{w1}, D_2 and D_5 are OFF and D_4 and D_6 are in conduction. The current flow in mode-2 operation while S_{w2} fails is shown in Fig. 6. L and C_1 discharge through the voltage V_{in} and C_5, while C_3 discharge through C_4. The voltage equations are derived by applying Kirchhoff's law and are as follows:

$$\begin{cases}(V_L = V_{in} + V_{C1} - V_{C5}) \\ (V_{C3} = V_{C4}), (V_o = V_{C4} + V_{C5})\end{cases} \tag{15}$$

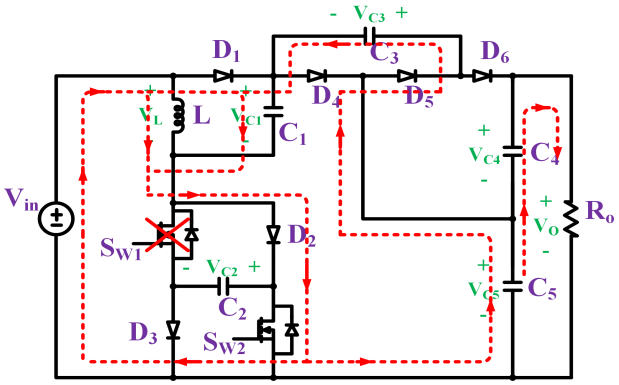


Fig. 7. Current flow (S_{w1} fails) during mode-1 operation.

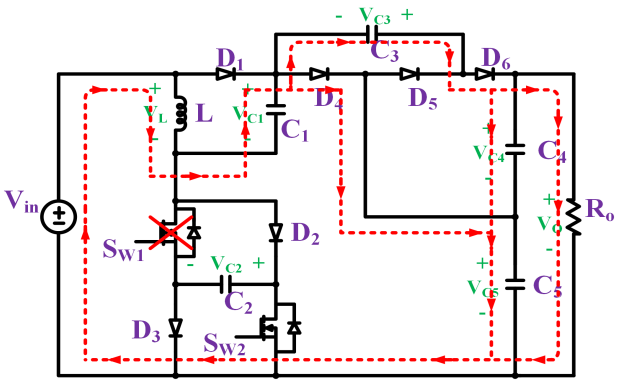


Fig. 8. Current flow (S_{w1} fails) during mode-2 operation.

Case-2: When S_{w1} is open circuit:

Similarly to case-1, the converter functions in two modes. The current flow when S_{w1} fails is shown in Fig. 7 and Fig. 8. Based on Fig. 7 and Fig. 8, it is observed that the voltage equations are closely related to those of case-1 with a few changes in terms of active component.

B. Voltage Conversion Gain

Case-1: When S_{w2} is open circuit:

By applying volt-sec balance across inductor.

$$\int_0^{DT_S} (V_L) = -\int_{DT_S}^{T_S} (V_L) \tag{16}$$

Table II summarizes the voltage stress of the capacitors in terms of input voltage and duty cycle when S_{w2} is open circuit. The voltage gain of converter when S_{w2} fault operation is given as.

$$M_{CCM} = \left(\frac{V_o}{V_{in}}\right) = \left(\frac{3-D}{1-D}\right) \tag{17}$$

Case-2: When S_{w1} is open circuit:

By applying volt-sec balance across inductor.

$$\int_0^{DT_S} (V_L) = -\int_{DT_S}^{T_S} (V_L) \tag{18}$$

TABLE II
FAULT OPERATION CAPACITOR VOLTAGES

Faulty Switch	S_{w2}	S_{w1}
Devices	**Voltage Gain**	**Voltage Gain**
V_{C1}	V_{in}	V_{in}
V_{C3},V_{C4}	$\left(\frac{V_{in}}{1-D}\right)$	$\left(\frac{V_{in}}{1-D}\right)$
V_{C5}	$\left(\frac{(2-D)V_{in}}{1-D}\right)$	$\left(\frac{(2-D)V_{in}}{1-D}\right)$

Table II summarizes the voltage stress of the capacitors in terms of the input voltage and duty cycle when S_{w1} is open circuit.

The voltage gain of the converter when S_{w1} fault operation is given as

$$M_{CCM} = \left(\frac{V_o}{V_{in}}\right) = \left(\frac{3-D}{1-D}\right) \tag{19}$$

TABLE III
FAULT OPERATION VOLTAGE STRESS

Faulty Switch	S_{w2}	S_{w1}
Devices	**Voltage Stress**	**Voltage Stress**
Switch	$\left(\frac{V_o}{3-D}\right)$	$\left(\frac{V_o}{3-D}\right)$
Diodes	$\left(\frac{V_o}{3-D}\right)$	$\left(\frac{V_o}{3-D}\right)$

C. Voltage Stress Calculations

Voltage stress occurs when active devices are reverse biased or turned OFF. Table III lists the voltage stress of diodes and switches with S_{w2} or S_{w1} is under open circuit fault.

IV. Modeling of Proposed Converter

Pulse Width Modulation (PWM) converters are classified as non-linear time-invariant circuits, which makes dynamic and stability analysis challenging. To address this issue, a small-signal state-space averaging modeling approach is used to linearize the converters. The state space representation of a PWM converter can be formulated using state variables, control inputs, and output variables.

$$\dot{x} = Ax + Bu \tag{20}$$

$$y = Cx \tag{21}$$

It is essential to recognize that all energy storage components, including (L, C_1, C_2, C_3, C_4 and C_5), are assumed as state variables. The state equation of the converter over a one-switching period is as follows.

$$\begin{pmatrix} \dot{\hat{I}}_{L1} \\ \dot{\hat{V}}_{C1} \\ \dot{\hat{V}}_{C2} \\ \dot{\hat{V}}_{C3} \\ \dot{\hat{V}}_{C4} \\ \dot{\hat{V}}_{C5} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & \left(\frac{2D-1}{L}\right) & 0 & 0 \\ -\left(\frac{1}{C_1}\right) & 0 & 0 & 0 & 0 & 0 \\ -\left(\frac{2D-1}{C_2}\right) & 0 & 0 & 0 & 0 & 0 \\ \left(\frac{D}{C_3}\right) & 0 & 0 & 0 & 0 & -\left(\frac{1-D}{R_o C_3}\right) \\ 0 & 0 & 0 & 0 & 0 & -\left(\frac{1}{R_o C_4}\right) \\ -\left(\frac{2D-1}{C_5}\right) & 0 & 0 & 0 & 0 & -\left(\frac{2D-1}{R_o C_5}\right) \end{pmatrix} \begin{pmatrix} \hat{I}_L \\ \hat{V}_{C1} \\ \hat{V}_{C2} \\ \hat{V}_{C3} \\ \hat{V}_{C4} \\ \hat{V}_{C5} \end{pmatrix} + \begin{pmatrix} I_L\left(-\frac{2}{C_2} + \frac{1}{C_3} - \frac{2}{C_5}\right) \\ 0 \\ V_{C2}\left(\frac{2}{L}\right) \\ 0 \\ 0 \\ V_{C5}\left(\frac{1}{R_o C_3} + \frac{2}{R_o C_5}\right) \end{pmatrix} \hat{d} \tag{22}$$

$$\left(V_o\right) = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{pmatrix} \begin{pmatrix} \hat{I}_L \\ \hat{V}_{C1} \\ \hat{V}_{C2} \\ \hat{V}_{C3} \\ \hat{V}_{C4} \\ \hat{V}_{C5} \end{pmatrix} + \left(0\right)\left(\hat{d}\right) \tag{23}$$

Every element indicated by ($\wedge$) represents a small ac variation.

The open-loop transfer function of the proposed converter is as follows.

$$\frac{V_o}{d(s)} = \frac{16312(s - 1.22e^5)(s - 219.5)(s - 25)}{s(s + 1600)(s - 1600)(s - 8)} \tag{24}$$

To assess dynamic performance, a small-signal frequency analysis is performed. Fig. 9 shows the open-loop frequency response transfer function. Fig. 10 shows the closed-loop control system of the converter, which integrates both a PID controller and a fault detection unit. This configuration enables dynamic adjustment of the output voltage to maintain optimal performance under varying operating conditions. To design the PID controller, the Ziegler-Nichols tuning method was used. This approach involved determining the ultimate gain K_u and the ultimate period P_u by analyzing the system stable oscillatory response. Using these values, the proportional,

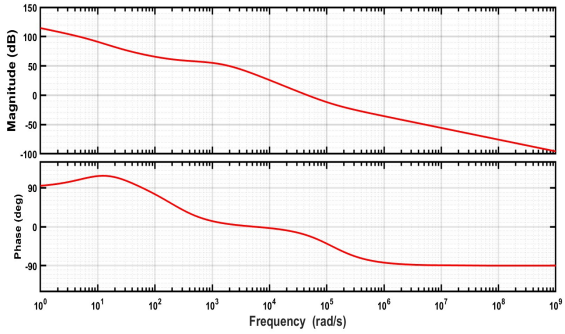


Fig. 9. Proposed converter open loop frequency response.

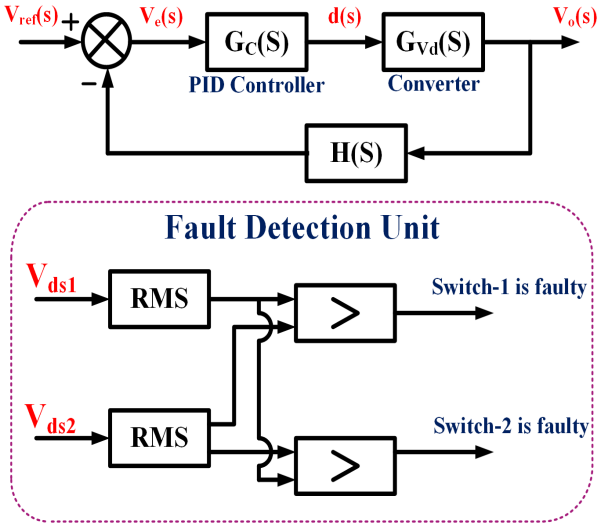


Fig. 10. Closed-loop Control strategy of proposed converter.

integral and derivative gains were calculated in accordance with the standard Ziegler-Nichols formulas. The resulting PID parameters ensure effective regulation of the output voltage, delivering consistent system performance while accommodating fluctuations in operational demands.

The fault detection unit plays a critical role in ensuring the reliability and functionality of the system by continuously monitoring switch voltages to detect anomalies or irregularities. By analyzing these voltages, the unit can quickly identify faults, such as deviations from expected voltage levels that may indicate issues with one or more switches in the converter. Upon detecting a fault, it provides a notification for corrective action. The identified fault can then be addressed during scheduled maintenance, allowing replacement or repair of the defective switch.

During normal operation of switch S_{w1} , the system exhibits a specific voltage condition where the RMS values of the switch voltages remain the same. However, an open circuit in S_{w1} interrupts the current flow, causing this distinctive switch voltage pattern. Identifying this anomaly, the fault detection unit efficiently recognizes the fault in S_{w1}. This detection allows for timely maintenance actions, such as replacement or repair, ensuring the reliability and functionality of the converter.

TABLE IV
COMPARISON OF HIGH GAIN DC-DC CONVERTERS

Topology	L/C/D/S/TC	Common Grounding	Voltage Gain (M)	Max. Normalized Switch Stress	Max. Normalized Diode Stress	Max. Normalized Capacitor Stress	Max. Normalized Inductor Current Stress	Max. Normalized Switch Current Stress
[13]	1/3/4/2/10	No	$\left(\frac{3-D}{1-2D}\right)$	$\left(\frac{1}{3-2D}\right)$	$\left(\frac{2}{3-2D}\right)$	1	$\left(\frac{3}{1-2D}\right)$	$\left(\frac{1}{\sqrt{D}(1-2D)}\right)$
[14]	1/5/6/2/14	Yes	$\left(\frac{4}{1-2D}\right)$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\left(\frac{4}{1-2D}\right)$	$\left(\frac{2}{\sqrt{D}(1-2D)}\right)$
[6]	2/4/3/1/10	Yes	$\left(\frac{2-D}{1-2D}\right)$	$\left(\frac{1}{2-D}\right)$	$\left(\frac{1}{2-D}\right)$	$\left(\frac{1}{2-D}\right)$	$\left(\frac{2-D}{1-2D}\right)$	$\left(\frac{1+D}{\sqrt{D}(1-2D)}\right)$
[10]	1/4/5/2/12	Yes	$\left(\frac{3}{1-2D}\right)$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{2}{3}$	$\left(\frac{3}{1-2D}\right)$	$\left(\frac{2}{\sqrt{D}(1-2D)}\right)$
[7]	3/5/4/2/14	No	$\left(\frac{3-3D-2D^2}{(1-D)(1-2D)}\right)$	$\left(\frac{1-D}{3-3D-2D^2}\right)$	$\left(\frac{2-D}{3-3D-2D^2}\right)$	$\left(\frac{2-4D^2}{3-3D-2D^2}\right)$	$\left(\frac{2}{1-2D}\right)$	$\left(\frac{1+2D}{\sqrt{D}(1-2D)}\right)$
[11]	1/3/4/2/10	Yes	$\left(\frac{3-2D}{1-2D}\right)$	$\left(\frac{1}{3-2D}\right)$	1	1	$\left(\frac{2}{1-2D}\right)$	$\left(\frac{2}{\sqrt{D}(1-2D)}\right)$
[8]	3/7/5/1/16	No	$\left(\frac{2+D}{1-2D}\right)$	$\left(\frac{1}{2+D}\right)$	$\left(\frac{1}{2+D}\right)$	1	$\left(\frac{2+D}{1-2D}\right)$	$\left(\frac{2+D}{\sqrt{D}(1-2D)}\right)$
[12]	1/4/5/2/12	Yes	$\left(\frac{3}{1-2D}\right)$	$\left(\frac{1}{3}\right)$	$\left(\frac{2}{3}\right)$	1	$\left(\frac{3}{1-2D}\right)$	$\left(\frac{1+D}{\sqrt{D}(1-2D)}\right)$
[9]	3/6/4/1/14	No	$\left(\frac{3-2D}{1-2D}\right)$	$\left(\frac{1}{3-2D}\right)$	$\left(\frac{1}{3-2D}\right)$	1	$\left(\frac{2}{1-2D}\right)$	$\left(\frac{2}{\sqrt{D}(1-2D)}\right)$
Proposed	**1/5/6/2/14**	**Yes**	$\left(\frac{\mathbf{5-2D}}{\mathbf{1-2D}}\right)$	$\left(\frac{\mathbf{1}}{\mathbf{5-2D}}\right)$	$\left(\frac{\mathbf{2}}{\mathbf{5-2D}}\right)$	$\left(\frac{\mathbf{3-2D}}{\mathbf{5-2D}}\right)$	$\left(\frac{\mathbf{4}}{\mathbf{1-2D}}\right)$	$\left(\frac{\mathbf{2}}{\sqrt{\mathbf{D}}\mathbf{(1-2D)}}\right)$

TABLE V
COMPARISON OF DC-DC CONVERTERS WITH FAULT-TOLERANT OPERATION

Parameters \ References		[22]	[23]	[24]	[25]	[26] N=2	[27] N=2	[28]	[29]	[30] N=3	Proposed
No. of elements		10	22	6	13	13	8	10	10	18	14
Reconfiguration capability		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Redundancy replacement		No	Converter	Leg	Element	No	No	No	No	No	No
Voltage gain (M_{CCM})	**Pre-fault**	$\frac{1}{1-D}$	$(\frac{1}{1-2D})^2$	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$(N+1)$	$\frac{1+D}{1-D}$	$\frac{2}{1-D}$	$\frac{3-D}{1-D}$	$\frac{3}{1-D}$	$\frac{5-2D}{1-2D}$
	Post-fault	$\frac{1}{1-D}$	$\frac{1}{1-2D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$	(N)	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2-D}{1-D}$	$\frac{2}{1-D}$	$\frac{3-D}{1-D}$
Voltage stress (V_{sw}/V_o)	**Pre-fault**	1	0.5,1	1	0.5	0.5	$\frac{1}{1+D}$	0.5	$\frac{1}{3-D}$	$\frac{1}{3}$	$\frac{1}{5-2D}$
	Post-fault	1	1	1	1	1	1	$1, \frac{1}{2-D}$	$\frac{1}{2-D}$	$\frac{1}{2}$	$\frac{1}{3-D}$
Common grounding		Yes	Yes	No	No	Yes	No	No	Yes	Yes	Yes

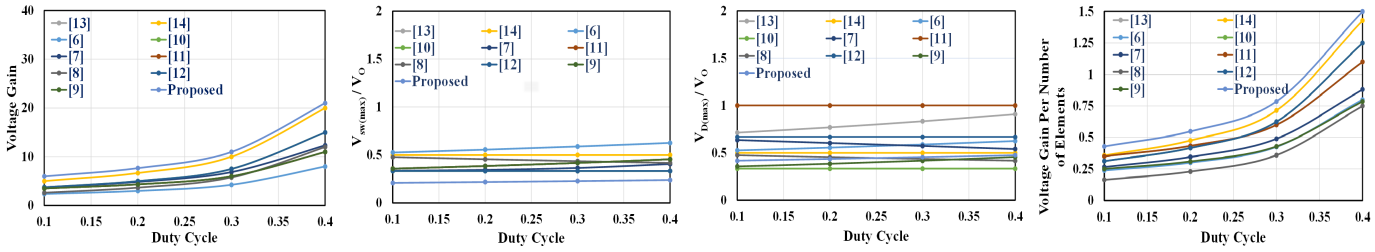


Fig. 11. Comparison of (a). Voltage gain (b). Maximum voltage stress across switches (c). Maximum voltage stress across diodes (d). Voltage gain per number of elements.

V. COMPARATIVE ANALYSIS

The performance of the proposed converter is compared with that of other high-gain converters reported in the literature, as shown in Table IV. This analysis includes important performance metrics such as component count, voltage gain in Continuous Conduction Mode (CCM), voltage stress on power devices, and whether there is a common ground. In Table IV, graphical representations of voltage gains versus duty cycle, maximum normalized switch voltage stress versus

duty cycle, maximum normalized diode voltage stress versus duty cycle, and voltage gain per number of components versus duty cycle are shown in Fig. 11. These graphs highlight the performance characteristics of the proposed high DC-DC converter. Furthermore, the performance of the proposed converter is compared with other DC-DC converters that possess fault-tolerant capabilities, as presented in Table V.

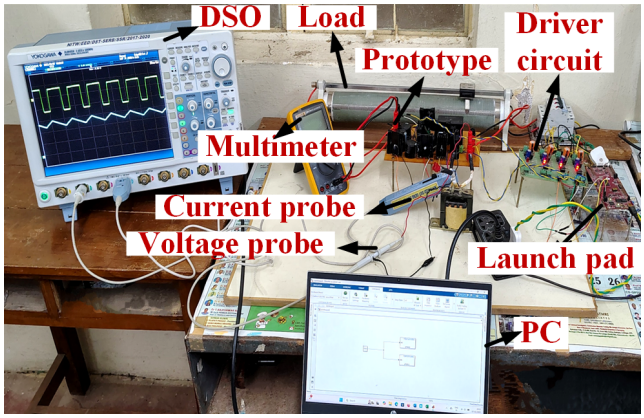


Fig. 12. Experimental setup of proposed converter topology.

VI. Experimental Results

The proposed converter has been fabricated using the components detailed in Table VI, and the control logic was implemented with the LAUNCHXL-F28379D processor. Fig. 12 shows the experimental setup for the converter. Tests were conducted to evaluate its performance under normal and fault conditions.

TABLE VI
Specifications of Converter

Component	Rating/Value
Input voltage	30 V
Inductor	0.5 mH
Capacitor C_{1-2}, C_{3-5}	50 μF, 100 μF
Load	400 Ω
PID Controller Coefficients	K_P=0.008, K_I=2.5 K_D=1.5$*e^{-6}$, N_D=11000
Switching Frequency	33 kHz
Switches	IRFP4668PbF
Diodes	STTH61W04S

A. Normal Operation:

During normal operation, the converter offers a high gain of M = 13.5(D = 0.34) at an output power of 400 W at 400 V and 1 A, as shown in Fig. 13(a). The voltage across C_5 and C_4 is shown in Fig. 13(a) whose average values are 185.18 V and 214.81 V respectively. The voltage across C_3, C_2 and C_1 is shown in Fig. 13(b) whose average values are 122.22 V, 92.59 V and 185.18 V respectively. Fig. 13(c) shows the voltage and current of L, whose average current value of inductor is 12.89 A. Fig. 13(d) shows the voltage stress across S_{w1} and S_{w2} whose peak value are 92.59 V and 92.59 V, which is less than the output voltage. Fig. 13(e) and Fig. 13(f) shows the voltage stress across D_1, D_2, D_3, D_4, D_5, and D_6, whose peak value are 185.18 V, 92.59 V, 92.59 V, 185.18 V, 185.18 V, and 185.18 V, respectively.

B. Closed Loop Operation

To evaluate the performance of the system under varying input conditions, an input voltage step-change experiment was carried out, in which the V_{in} transitions from 30 V to 50 V and 50 V to 30 V. The corresponding output voltage and current responses are shown in Fig. 14(a). Furthermore, to assess the converter resilience against load variations, a load step-change experiment was carried out. In this test, the output power of the converter alternates between 400 W and 200 W, ensuring a stable V_o of 400 V throughout the process. As expected, the output current at 200 W is observed to be precisely half of that at 400 W. The experimental results for this test are shown in Fig. 14(b).

C. Fault Operation

During switch-1 fault operation converter offers a high gain of M = 13.5(D = 0.85) at an output power of 400 W at 400 V and 1 A , as shown in Fig. 15(a). The voltage across C_5 and C_4 is shown in Fig. 15(a) whose average values are 214 V and 186 V respectively. The voltage across C_3, and C_1 is shown in Fig. 15(b) whose average values are 186 V and 29 V respectively. Fig. 15(c) shows the voltage and current of L whose average current values is 13.33 A and voltage stress across S_{w2} whose peak value is 186 V. Fig. 15(d) shows the S_{w1} and S_{w2} currents whose Rms value are 0 A and 10.24 A respectively. Fig. 15(e) and Fig. 15(f) shows the voltage stress across D_1, D_2, D_4, D_5, and D_6 whose peak value are 186 V, 186 V, 186 V, 186 V, and 186 V, respectively. The fault dynamic behavior in open-loop operation of converter during S_{w1} fault is shown in Fig. 16(a) and Fig. 16(b) at D=0.34. Fig. 16(a) shows the fault dynamics across output voltage, output current, and input current. Fig. 16(b) shows the fault dynamics across switch voltages.

Similarly switch-2 fault operation converter offers a high gain of M = 13.5(D = 0.85) at an output of 400 W at 400 V, as shown in Fig. 17(a). The voltage across capacitors (C_5 and C_4) is shown in Fig. 17(a) whose average values are 214 V and 186 V respectively. The voltage across C_3, and C_1 is shown in Fig. 17(b) whose average values are 186 V and 29 V respectively. Fig. 17(c) shows the voltage and current of L whose average current values is 13.33 A and voltage stress across S_{w2} whose peak value is 186 V. Fig. 17(d) shows the S_{w1} and S_{w2} currents whose Rms value are 10.24 A and 0 A respectively. Fig. 17(e) and Fig. 17(f) shows the voltage stress across D_1, D_3, D_4, D_5, and D_6 whose peak value are 186 V, 186 V, 186 V, 186 V, and 186 V, respectively. The fault dynamic behavior in open-loop operation of converter during S_{w2} fault is shown in Fig. 18(a) and Fig. 18(b) at D=0.34. Fig. 18(a) shows the fault dynamics across output voltage, output current and input current. Fig. 18(b) shows the fault dynamics across switch voltages.

D. Closed Loop Fault Dynamic

The proposed converter fault-tolerant capability when S_{w1} is open circuit, and S_{w2} is ON is assessed in closed loop. Fig. 19(a) shows the fault dynamic behavior of the output voltage

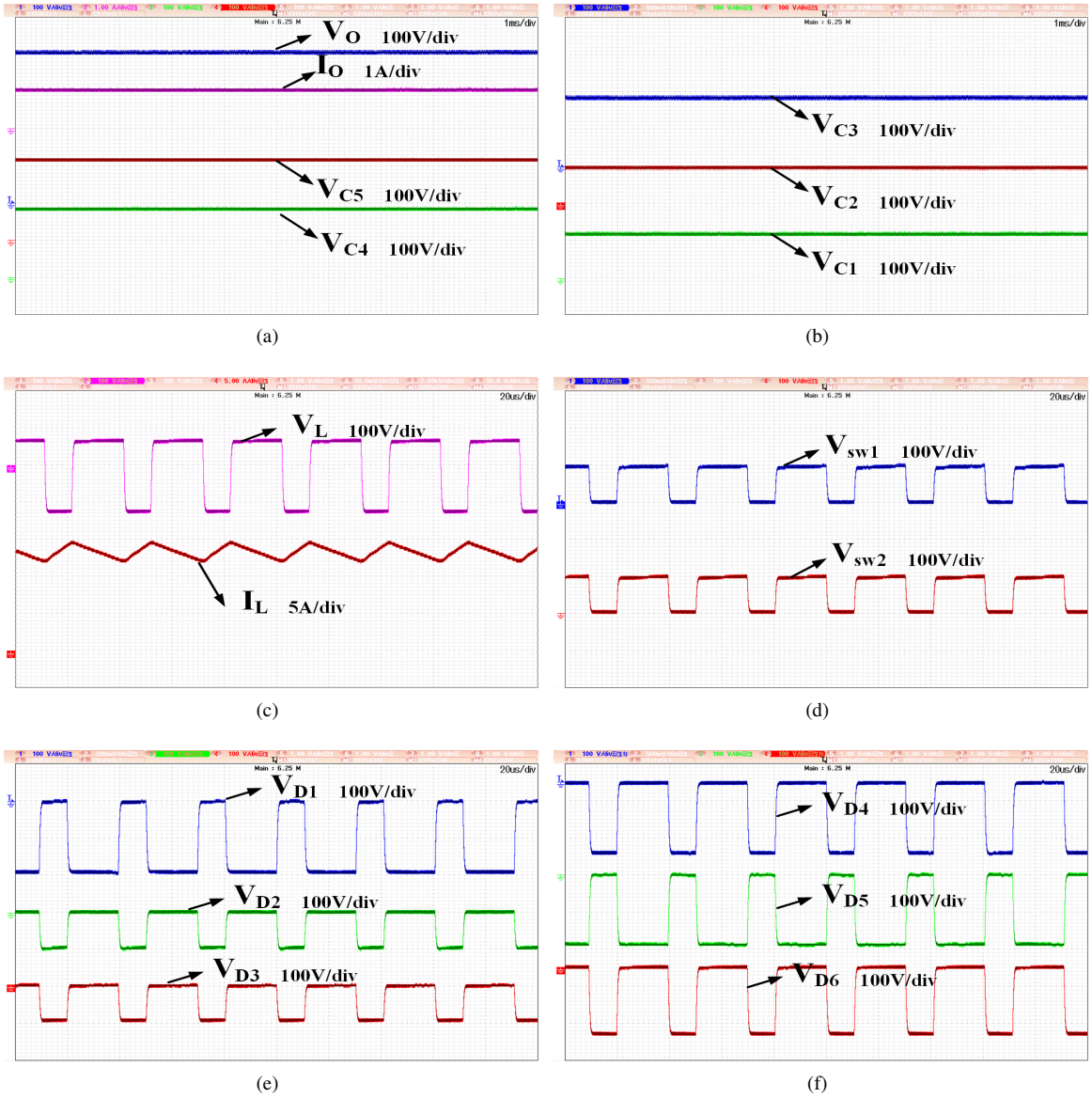


Fig. 13. Experimental waveforms during normal operation (a). Output voltage & current and voltage across capacitor-5, 4 (b). Voltage across capacitor-3, 2, 1 (c). Inductor voltage and current (d). Voltage across switches (e). Voltage across diode-1, 2, 3 (f). Voltage across diode-4, 5, 6.

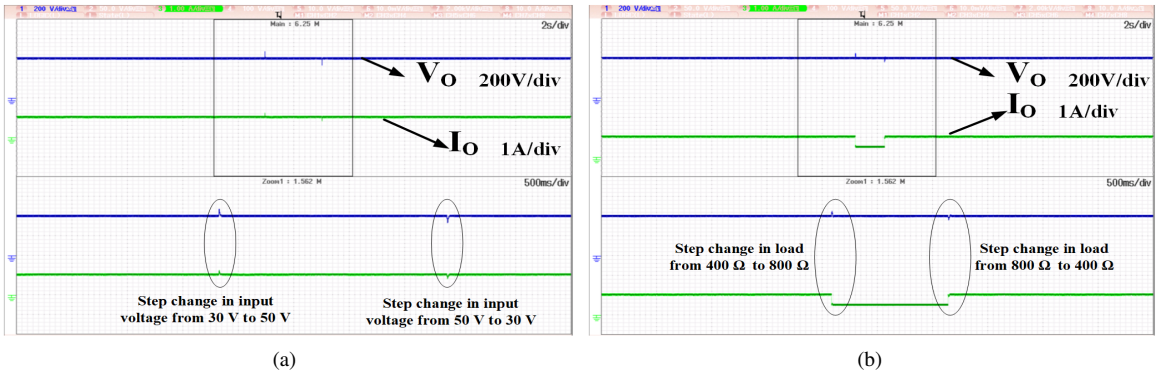


Fig. 14. Experimental waveforms during closed loop operation (a). Step change in input voltage (b). Step change in load.

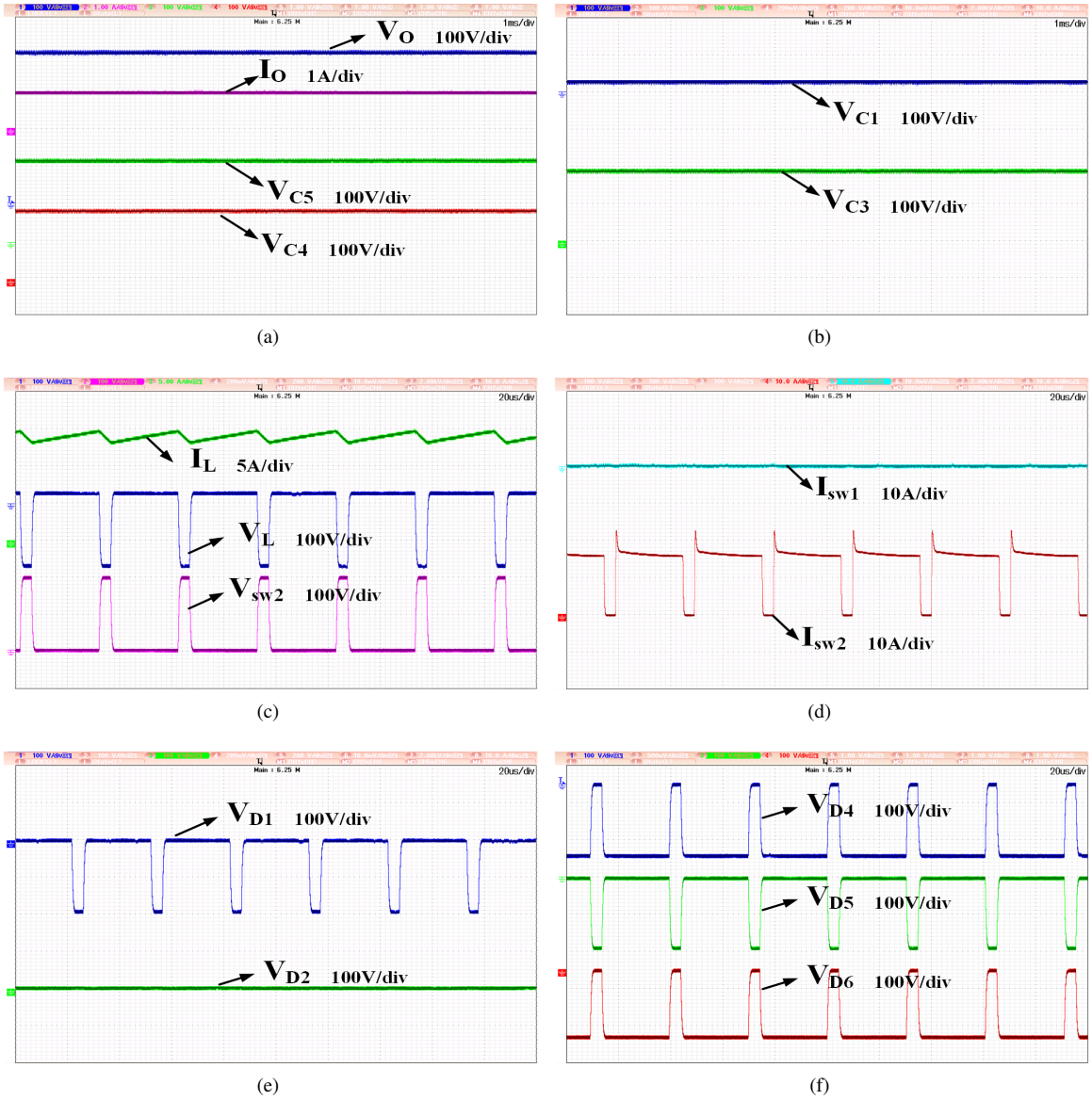


Fig. 15. Experimental waveforms during switch-1 fault operation (a). Output voltage & current and voltage across capacitor-5, 4 (b). Voltage across capacitor-3, 1 (c). Inductor voltage and current and voltage across switch (d). Switch currents (e). Voltage across diode-1, 2 (f). Voltage across diode-4, 5, 6.

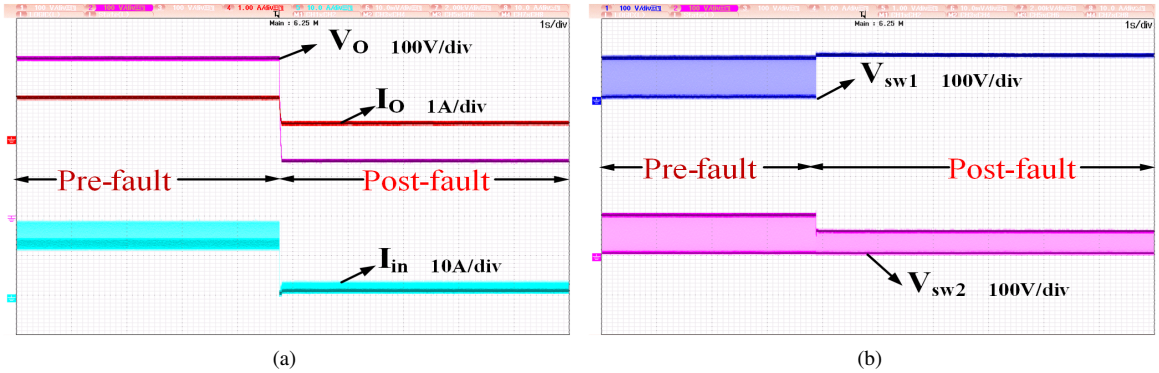


Fig. 16. Experimental waveforms during open loop fault dynamic of switch-1 fault (a). Output voltage, output current and input current (b). Voltage across switches.

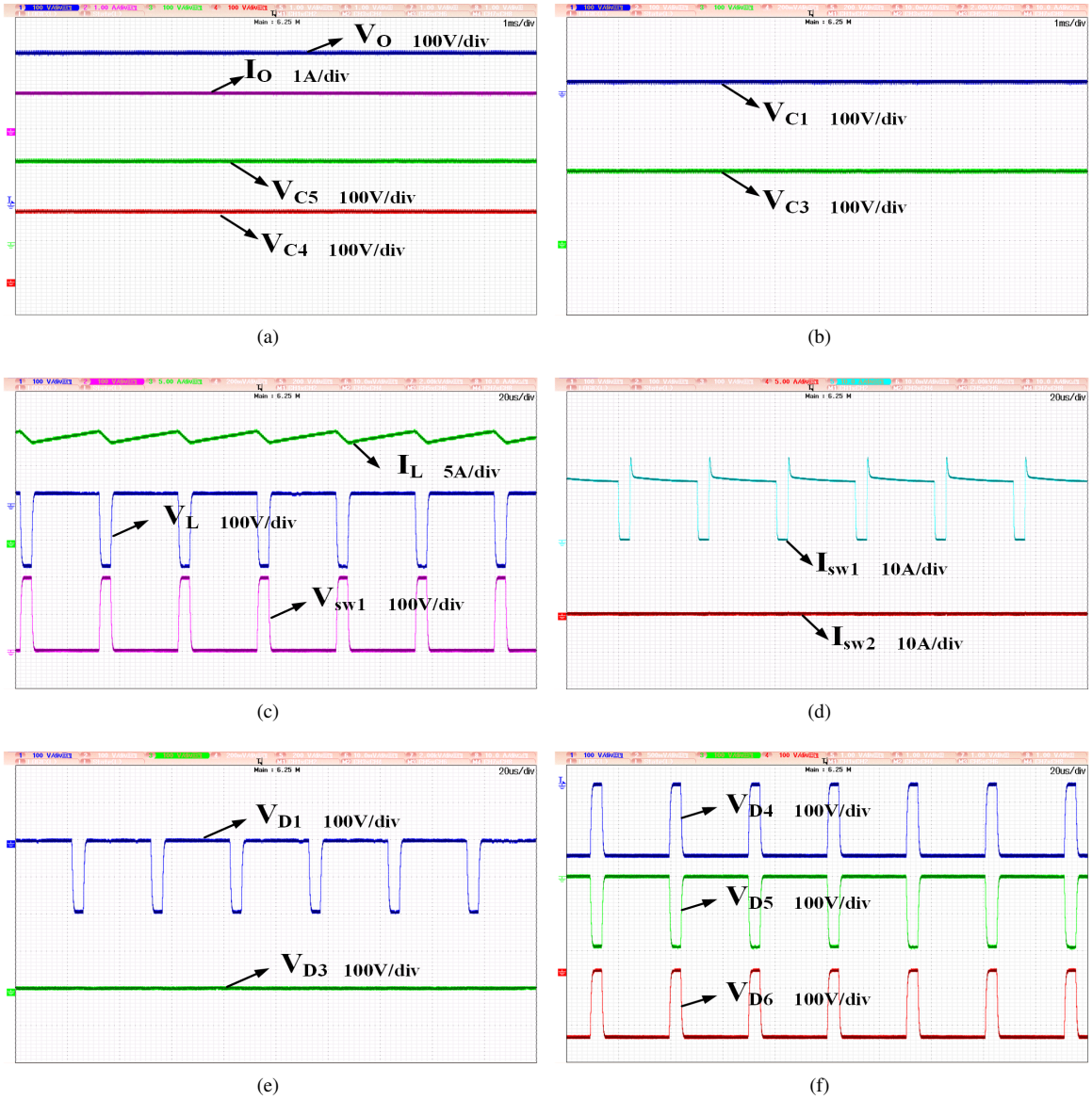


Fig. 17. Experimental waveforms during switch-2 fault operation (a). Output voltage & current and voltage across capacitor-5, 4 (b). Voltage across capacitor-3, 1 (c). Inductor voltage and current and voltage across switch (d). Switch currents (e). Voltage across diode-1, 3 (f). Voltage across diode-4, 5, 6.

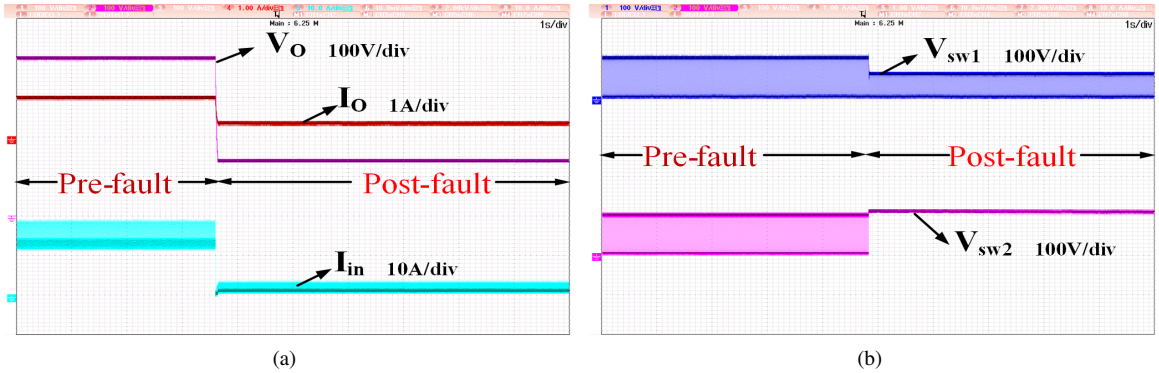
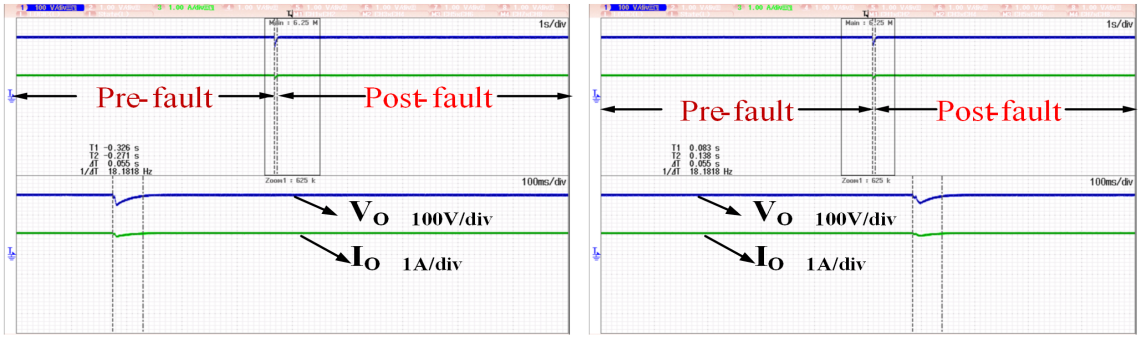
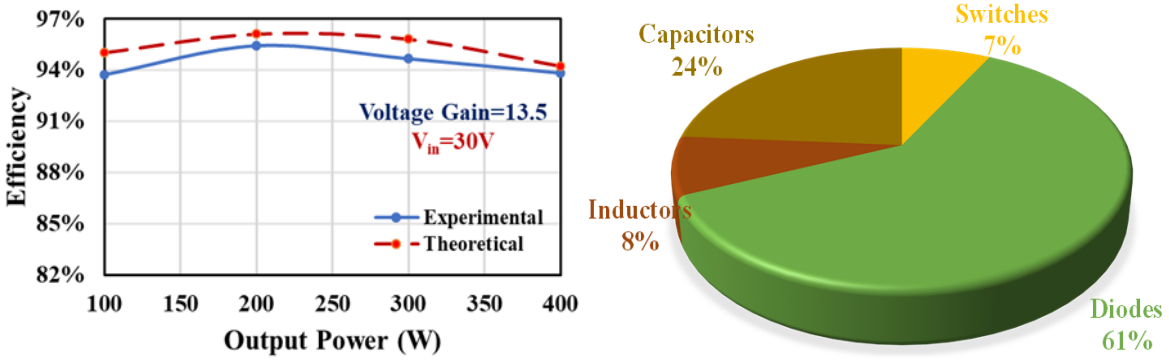


Fig. 18. Experimental waveforms during open loop fault dynamic of switch-2 fault (a). Output voltage, output current and input current (b). Voltage across switches.



(a) (b)

Fig. 19. Experimental waveforms during closed loop fault dynamics (a). Output voltage and output current during switch S_{w1} fault (b). Output voltage and output current during switch S_{w2} fault.



(a) (b)

Fig. 20. (a). Performance comparison of converter (b). Power loss distribution in the proposed converter.

and current. Similarly when S_{w2} is open circuit, and S_{w1} is ON is considered. Fig. 19(b) shows the fault dynamic behavior of the output voltage and current.

E. Efficiency Analysis

The efficiency is shown to exhibit dependency on the voltage gain. The theoretical power loss distribution of the converter thoroughly evaluated at a rated output power of 200 W and a high voltage gain ratio of M = 13.5.

Inductor Loss:

$$\begin{cases} P_{Loss,L} = r_L I_{Rms,L}^2 \\ P_{Loss,L} = 0.65\ W \end{cases} \tag{25}$$

Capacitor Loss:

$$\begin{cases} P_{Loss,C} = r_C I_{Rms,C}^2, \\ P_{Loss,C} = 2.01\ W \end{cases} \tag{26}$$

Diode Loss:

$$\begin{cases} P_{Loss,D} = P_{Forward\ drop,D} + P_{conduction,D} \\ = V_{FD} I_{Avg,D}^2 + r_D I_{Rms,D}^2 \\ P_{Loss,D} = 4.8\ W \end{cases} \tag{27}$$

Switch Loss:

$$\begin{cases} P_{Loss,sw} = P_{Turn-on\ and\ off} + P_{conduction} \\ = 0.5 F_s \left(t_r + t_f\right) I_{Avg} V_{DS} + r_{sw} I_{Rms}^2 \\ P_{Loss,sw} = 0.56\ W \end{cases} \tag{28}$$

The efficiency of the converter can be obtained as follows:

$$P_{Losses} = P_{(L)} + P_{(C)} + P_{(D)} + P_{(sw)} = 8.01\ W \tag{29}$$

Therefore, converter theoretical efficiency is $\eta_{converter} = 96.14\%$

Fig. 20(a) shows the efficiency of the proposed converter at different power levels during normal operation with a voltage gain of $M = 13.5$. The total experimental power losses are rigorously determined through thermal modeling analysis conducted within the PSIM software by modeling individual components of the converter. The experimental results indicate an efficiency of 95.4 % at a power output of 200 W during normal operation. Fig. 20(b) shows the distribution of power losses in the converter during normal operation, with a voltage gain of $M = 13.5$ and an output power of 200 W. From the analysis in Fig. 20(b), it is evident that most of the losses occur in the diodes, followed by the capacitors.

VII. Conclusion

This paper presents a comprehensive analysis of a high step-up dual-switch Luo non-isolated DC-DC converter to

achieve higher voltage gains at reduced duty cycles, common grounding, high efficiency, and capable of reconfiguring. The converter exhibits low-voltage stress during normal and fault conditions. The stability of the converter is evaluated using small-signal analysis. The converter has been designed, fabricated, and tested to achieve an output power of 400 W at an output voltage of 400 V by offering a peak efficiency of 95.4% (200 W) at a voltage gain of 13.5. Experimental results demonstrate the effectiveness of w.r.t, performance and reliability for critical load applications.

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