Rapid Prototyping of FPGA Controlled Common Ground Single-Phase Transformerless Five-Level Inverter using Xilinx System Generator

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***Abstract*—This paper presents a Field Programmable Gate Array (FPGA) implementation for rapid prototyping of a new single-phase transformerless five-level inverter for PV applications. The inverter features a reduced device count, a common ground that eliminates the leakage current issue, and 100 % DC utilization. It is capable of supplying both real and reactive power. A simple proportional-resonant (PR) controller is developed and uses a level-shifted pulse width modulation (LS-PWM) scheme to generate the firing pulses. Grid synchronization is achieved using a robust arc-tangent method-based phase-locked loop (PLL) strategy. To evaluate the open-loop performance, an experimental prototype is developed, and its responses are presented. Moreover, a hardware-in-the-loop (HIL) co-simulation is performed for grid interface to achieve real-time constraints on an Atlys Spartan 6 FPGA using Xilinx System Generator in the MATLAB/Simulink environment, and the results are reported. Finally, a detailed comparison of various five-level inverter topologies is presented to highlight the merits of the proposed topology.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9599

***Index Terms*—multi-level inverter, real power and reactive power, PR controller, FPGA, Pulse width modulation.**

I. Introduction

THE growing demand for the need of electricity, the finite fossil fuel resources and increasing concerns about global environmental pollution have driven a shift towards renewable energy power generation including photovoltaic (PV) systems, wind energy, fuel cells. Among these, photovoltaic technology has gained significant attention in recent years due to substantial reductions in initial costs and enhancement in the efficiency and effectiveness of PV panels. However, the advancement of power electronic interface has a vital role for efficiently transferring power from PV panels to the load. This can be achieved either through a single-stage inverter or a two-stage system that includes a DC/DC boost converter between the PV panels and the inverter. Typically, two-stage systems exhibit lower efficiency than single-stage systems due to the higher component count. Grid-connected transformerless inverters are becoming more popular because of their higher efficiency, compact design, and lower cost. Since they lack galvanic isolation, these inverters connect directly to the grid. This results a parasitic capacitance between the PV system and the ground, leading to a resonant path that can cause leakage current[1]. However, a significant drawback of these inverters is the unwanted leakage current. According to the German standard VDE 0126-01-01, this leakage current must be kept below 300 mA. Additionally, leakage current poses a significant challenge, as it results the flow of current through parasitics between the grid and PV panels [1]-[3]. As highlighted above, numerous researchers have sought effective solutions to reduce unwanted leakage current. One of the simplest approaches involves using the bipolar pulse width modulation strategy or a half-bridge (HB) inverter instead of a full-bridge (FB) inverter [4], [5]. This method ensures that the overall variations in common-mode voltage remain constant under all loading conditions.

On the other hand, to meet the requirements of strict grid codes, the compatibility between the grid voltage peak and the DC voltage from renewable energy sources, such as PV string panels, must be considered. Additionally, the issue of power quality enhancement (PQE) should be addressed, as it can impact the quality of the current injected into the grid and the design of the filter interface [6]. Compared to two-level inverters, multilevel inverters are getting more popularity due to their advantages, such as reduced voltage stress on devices, lower electromagnetic interference (EMI), and superior output voltage waveform quality with reduced total harmonic distortion (THD). Traditional topologies like neutral-point-clamped (NPC) and half-bridge inverters remain widely used in industries, as they effectively clamp common-mode voltage (CMV) and reduce the need for extensive filtering. However, they are limited by the partial utilization of the DC source [3], [7]. As a result, improving DC-link voltage utilization has become a key focus to enhance the overall system performance.

Due to the aforementioned limitations, significant research has recently been directed towards single-phase transformerless five-level inverters that feature reduced switch count, lower leakage current, and higher efficiency. Recent research has thus prioritized transformerless inverters (TLI) with a common ground design to address issues caused by common-mode voltage and leakage current, while also avoiding bulky transformers that add to size and cost. Many of these topologies incorporate a common ground design to mitigate leakage current while minimizing component count [8]-[10]. The Switched-

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Capacitor Converters (SCCs) has a feature of inherent self-voltage balancing of capacitors and lower electromagnetic interference, enhancing their appeal for diverse applications[8]. Consequently, balancing techniques that rely on active control or external circuits and sensors have become unnecessary. Typically, the development of these topologies is motivated by the demand for multiple output voltage levels and optimal utilization of DC-link voltage, all while aiming to minimize component count, manage reasonable maximum voltage stress (MVS) on switches, and enhance efficiency and power density. However, the devices used in these configurations are constrained by a maximum peak inverse voltage of 1.5, which limits their ability to handle a wide range of DC variations from PV panels. Some studies have suggested introducing an additional boost stage at the front-end [10], though this results in a two-stage process, leading to higher costs and reduced efficiency. From the literature [11-20], it is evident that each topology has its advantages and disadvantages. However, most topologies require more device count and lack of common ground features, as reported in [11], [12], [18] & [19].

Therefore, this paper proposes a common ground single-phase five-level inverter for grid-connected PV applications with reduced switch count, aimed at supporting a wide range of operations. The key features include:

1) Inherent self-voltage balancing capability, enabling simple pulse width modulation (PWM) operation.
2) The common ground design resolves the leakage current issue.
3) Use of a maximum of three switches in operation enhances the overall system efficiency.
4) A Simple closed-loop PR controller is introduced, providing both real and reactive power control.

Moreover, the testing and implementation of the developed system are more costly and time-consuming. In recent years, digital control platforms have been developed using high-end equipment such as OPAL-RT, MicroLab (dSPACE), and real-time simulators, which are very expensive. Consequently, HIL systems are becoming very popular for testing and realizing the practical constraints associated with prototype setups in the laboratory. Therefore, a low-cost FPGA board is used to perform HIL Co-simulation using Xilinx System Generator blocks interfaced with MATLAB software.

The organization of the paper is as follows: Section II outlines the complete operation and practical implementation of the digital control platform for the PLL, PR controller, and the generation of pulses using level-shifted pulse width modulation schemes. These are discussed extensively for closed-loop control using low-cost Xilinx System Generator blocks. Section III describes the development of a rapid prototype and details its open-loop response. Additionally, the procedure for HIL co-simulation for grid-connected mode and the corresponding results are presented. Section IV provides an extensive comparison of various five-level inverters in the literature to showcase the merits of the proposed topology. Finally, Section V concludes with the remarks.

II. Proposed Five-Level Inverter

Fig. 1 shows the proposed single-phase transformerless five-level inverter for PV applications, consisting of six switching devices and three capacitors for grid-connected operation [21]. The main advantage of the proposed topology is the common ground feature, which eliminates the leakage current problem between the PV panels and the grid due to parasitic capacitance, resulting in zero common mode voltage. In addition, it has inherent capacitor voltage balancing capability and 100 % utilization of DC input voltage. Moreover, the schematic view of the closed-loop control implemented on an FPGA board for both hardware and HIL operation is presented for easy understanding. It can be noticed that the proposed five-level topology is built with two simple H-bridges cascaded with a charge pump circuit, allowing the inverter to operate in five distinct switching states, as shown in Fig. 2. The switching sequence and their corresponding level generations are shown in Table I.

A. Switching States Operation

The operation of the five-level inverter and their corresponding output voltage generations are as follows

1) *State A*: During this state, the switches S_1, S_3 *and* S_5 is turned on, and the input voltage is directly connected to the grid to generate maximum output voltage $V_{out} = V_{dc}$, as shown in Fig. 2(a). During this condition the capacitor C_3 is floating and charges to the input DC voltage of V_{dc}.

2) *State B*: In this state, switches S_2, S_3 *and* S_5 are turned on, and the output of the inverter equal to half the dc input voltage, $V_{out} = V_{dc}/2$, as shown in Fig. 2(b). The stored energy across the capacitor C_2 is appeared at the output of the inverter.

3) *State C*: In this state, only switches S_4 *and* S_5 are turned on, and the output voltage is synthesized to zero voltage such that $V_{out} = 0$, as shown in Fig. 2(c). Moreover, there is no power flow from the source and the capacitors.

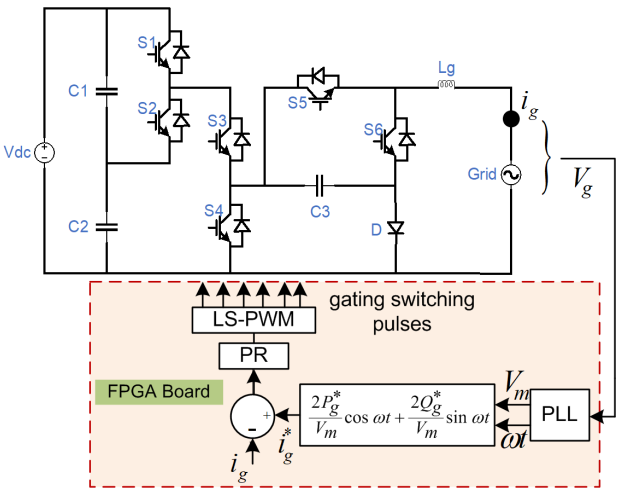


Fig. 1. Single-phase transformerless five-level inverter with closed-loop control scheme.

4) *State D*: During this state, the switches S_2, S_3 *and* S_6 are triggered, which results in the capacitors C_2 *and* C_3 are being connected in series in an opposing nature, causing half of the

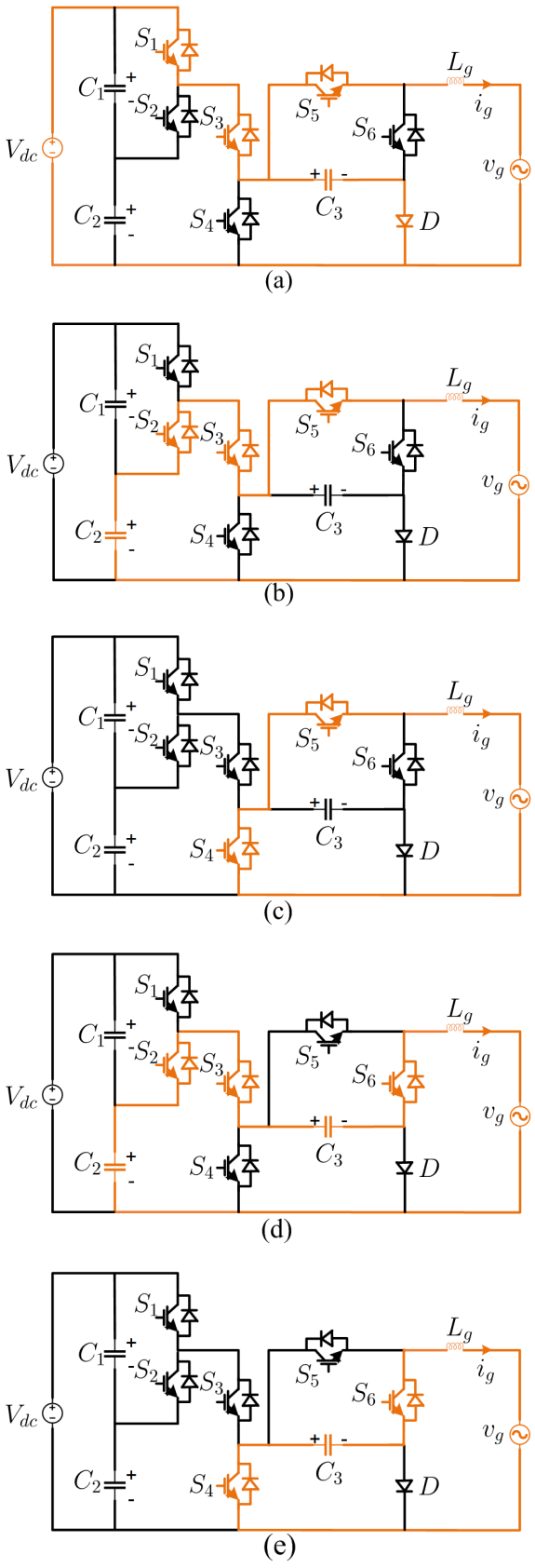


Fig. 2. Operating modes and current directions for output voltage generations (a) state A, (b) state B, (c) state C, (d) State D, & (e) State E.

TABLE I
SWITCHING STATES FOR FIVE-LEVEL OUTPUT VOLTAGE WAVEFORM

Level	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	1	0	1	0	1	0
$V_{dc}/2$	0	1	1	0	1	0
0	0	0	0	1	1	0
$-V_{dc}/2$	0	1	1	0	0	1
$-V_{dc}$	0	0	0	1	0	1

negative output voltage to be generated. It can be noted that output is equal to V_{out} = $(V_{dc}/2 - V_{dc}) = -V_{dc}/2$, as shown in Fig. 2(d).

5) *State E*: Finally, in this state, switches S_4 *and* S_6 are turned on the inverter output voltage is equal to the capacitor voltage C_3, synthesizing $V_{out} = -V_{dc}$ as shown in Fig. 2(e). During this state, C_3 supplies the load current and the remaining capacitors C_1 *and* C_2 are just floating and charges to half of the V_{dc}.

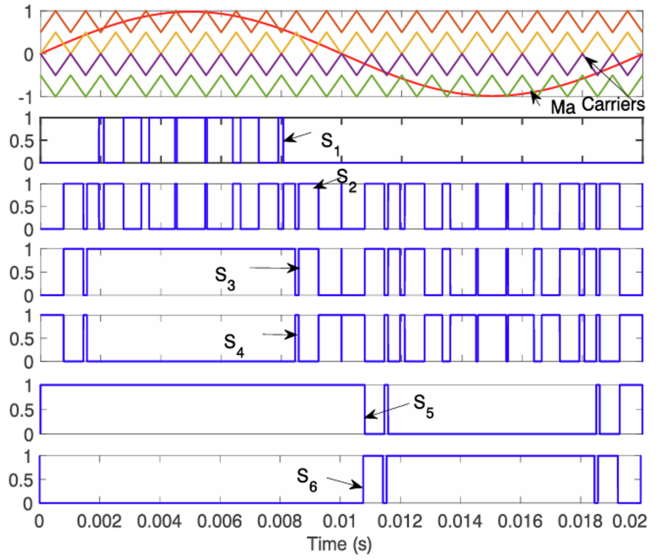
Finally, it can be noticed that the need of blocking voltage of each device is a major concern in the development of topology in recent years to reduce the power loss and cost of the system. The proposed topologies demands three switches S_1, S_2 & S_4 to generate half of the input DC-link voltage and the devices S_3, S_5 & S_6 need to block full DC-link voltage. Moreover, it can be observed that a maximum of 3 devices is only in conduction which will increase overall efficiency of the proposed system.

B. Pulse Width Modulation Scheme

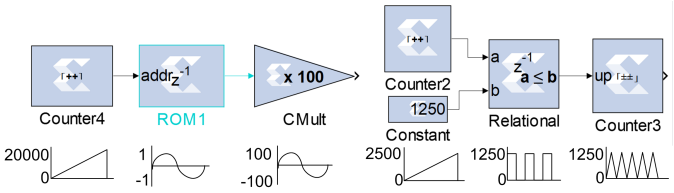
In this work, a simple level-shifted pulse width modulation scheme is implemented using Xilinx System Generator blocks, as shown in Fig. 3(a). It consists of four carriers and one sinusoidal fundamental voltage waveform to produce output voltages in the range of V_{dc}, $V_{dc}/2$, *0*, $-V_{dc}/2$ & $-V_{dc}$. The basic blocks used for the sine wave and carrier generation are shown in Fig. 3(b). It can be noticed that the sine waveform is generated using counter and ROM blocks, and the gain is adjusted as required. Similarly, the triangular waveform is generated using counters and relational operators, with a peak of 1250 achieved for a 2 kHz switching frequency. For example, the equation shows that the FPGA clock frequency of 100 MHz is scaled down to a 2500 count value for appropriate selection of the count value and explicit period. Furthermore, the four carriers are produced using addition blocks as per the requirement. Finally, simple logic gates are used to realize the five-level output voltage waveform and generate the switching signals, as shown in Fig. 3(a).

$$f = \frac{f_{\text{system clock}}}{\text{count value} \times \text{explicit period}} = \frac{100\,\text{MHz}}{2500 \times 20} = 2\,\text{kHz} \tag{1}$$

A simple phase-locked loop (PLL) is used to generate the reference ωt and V_m to compute the reference current i_g^*. Further, the actual sine waveform extracted from the grid is compared with the reference, and the error is passed through the PR controller to modulate the output of the waveform. This modulated waveform is then compared with the carrier signals



(a)



(b)

Fig. 3. (a) Level-shifted PWM and the switching signal for each device S_1 to S_6, (b) Xilinx blocks for sinewave and triangular wave generation.

to generate the gating pulses using LS-PWM, as discussed in the previous section. This PR controller primarily removes the steady-state error in the output waveform compared to the PI controller in [22]. Here, the tuning of PR parameters K_p *and* K_i are done based on the procedure adopted in ref. [23]. Moreover, the complete PR controller and generation of reference signals are implemented in digital form using Xilinx

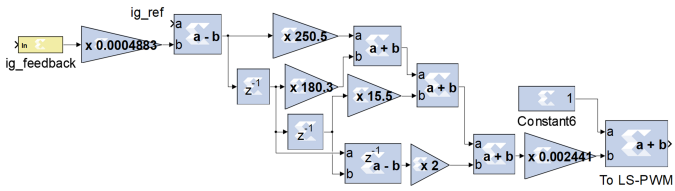


Fig. 4. Implementation of PR controller using xilinx blocks.

generator blocks, as discussed in the previous section as shown in Fig. 4.

C. Resonant Current Controller Design

In modern days, the PR current controller is gaining more attention due to its simplicity, easy implementation, and fast dynamic performance. Compared to various optimized technique-based controllers like fuzzy, neuro, or others, the PR controller is robust and can be implemented without complexity on digital platforms. Fig. 1 shows the implementation of the PR controller by comparing the reference current with the actual grid current. The reference current can be computed using the simple equation 2 for the real and reactive power demand.Here i_g^* is the reference grid current, P_g^* is the reference active power, Q_g^* is the reference reactive power, V_m is the peak value of the grid voltage, ω is the angular frequency of the grid ($\omega = 2\pi f$, $f = 50\,\text{Hz}$), $\cos(\omega t)$ and $\sin(\omega t)$ represent the phase components of the grid voltage.

$$i_g^* = \frac{2P_g^*}{V_m}\cos\omega t \pm \frac{2Q_g^*}{V_m}\sin\omega t \tag{2}$$

D. Phase-Locked Loop

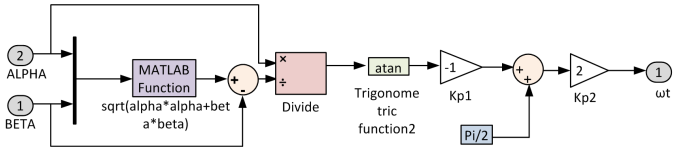
In the literature, various phase-locked loop (PLL) algorithms are proposed for single-phase grid-connected applications. However, this work uses a simple arc-tangent method for synchronization, as proposed in [24], to extract the angle. It is highly advantageous and provides a quick response without the use of any intermediate PI controller. The orthogonal signals $\alpha(t)$ and $\beta(t)$, extracted from the grid voltage, are processed through Matlab function, and the arctangent method is applied to detect the fundamental angle. Figs. 5 (a) and (b) show the PLL strategy of both the Simulink model and the implementation using Xilinx blocks. The PLL model built using Xilinx blocks makes the system very simple by using addition, multiplication, gain, and CORDIC 4.0 blocks for processing the digital signal and generating the angle. Finally, grid synchronization is achieved by tracking the angle and transforming it into sine and cosine angles multiplied by the magnitude of power demands to generate the grid reference current. Fig. 5(c) shows the sawtooth waveform generation and the corresponding sine and cosine signal generation, demonstrating that the PLL strategy is working effectively.

III. Results And Discussion

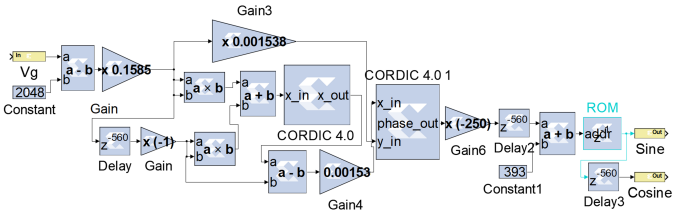
A. Standalone Mode

First and foremost, a prototype model of the proposed five-level inverter was built and tested in standalone mode with the available facilities in the laboratory. Figs. 6 and 7 shows the experimental setup developed, with pulses generated using Xilinx System Generator blocks in the MATLAB environment.The Atlys Spartan 6 FPGA board is used to generate the firing pulses using level-shifted PWM, as shown in Fig. 3. In addition, the waveforms are captured using a Tektronix 4 channel Mixed Signal Oscilloscope (MSO) MDO3024. The specifications of the prototype model are listed in Table II for easy understanding.

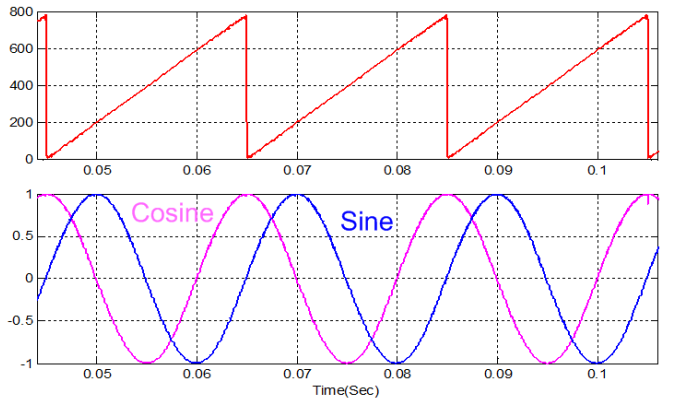
Fig. 8 shows the experimental results of the measured inverter output voltage and the corresponding load current. The inverter is tested with a DC input of 400 V, and the same voltage is observed in the inverter output voltage waveform. An RL load consisting of a 100 Ω resistor and a 10 mH inductor is used to test the inverter, resulting in a sinusoidal output current. Fig. 9 shows the measured capacitor voltages V_{C1}, V_{C2} and V_{C3}. It can be noticed that the DC-link voltage of $V_{dc}/2$ is maintained across capacitors C_1 and C_2, while



(a)



(b)



(c)

Fig. 5. Single-phase PLL proposed strategy (a) Simulink model, (b) Xilinx model, and (c)Measurement of PLL outputs:Sawtooth waveform and generation of sine & cosine waveforms.

TABLE II
PARAMETERS FOR HIL SIMULATION AND EXPERIMENTATION

Parameters	Value
Input voltage (V_{dc})	400 V
Output voltage (V_{ac})	230 V(RMS)
Switching Frequency (f_{sw})	5 kHz
Power Switches	IGBT CT60
Filter Inductor	6 mH
DC Capacitors	1000 μF, 500 V
Load Power	2 kW

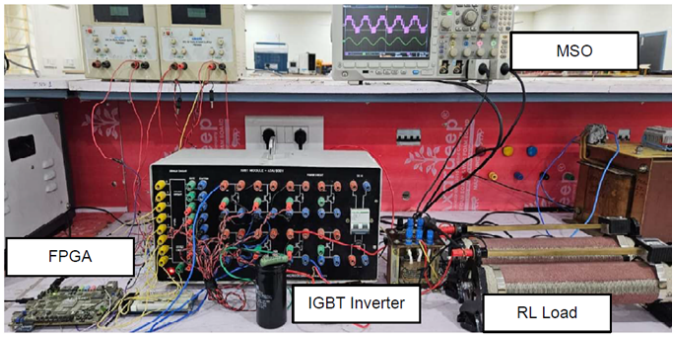


Fig. 6. Experimental setup of the five-level inverter prototype.

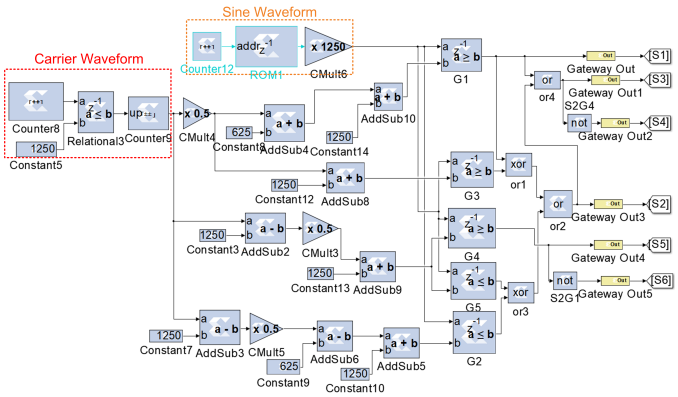


Fig. 7. PWM generation using xilinx system generator.

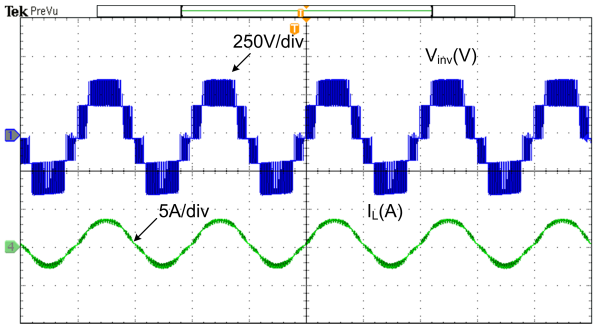


Fig. 8. Experimental results of inverter output voltage and load current.

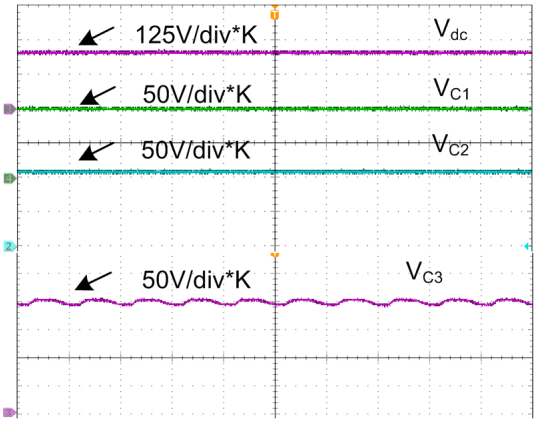


Fig. 9. Measured input voltage and voltage across the capacitors V_{C1}, V_{C2}, & V_{C3}.

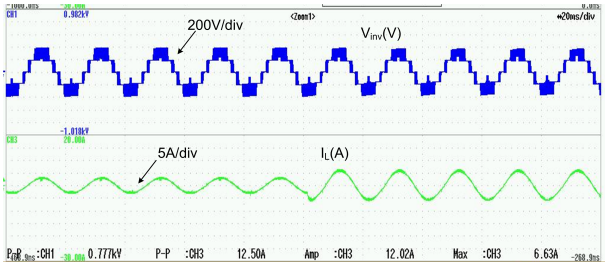


Fig. 10. Measured waveforms of inverter output voltage(V_{inv}), and load current(I_L) during load changes.

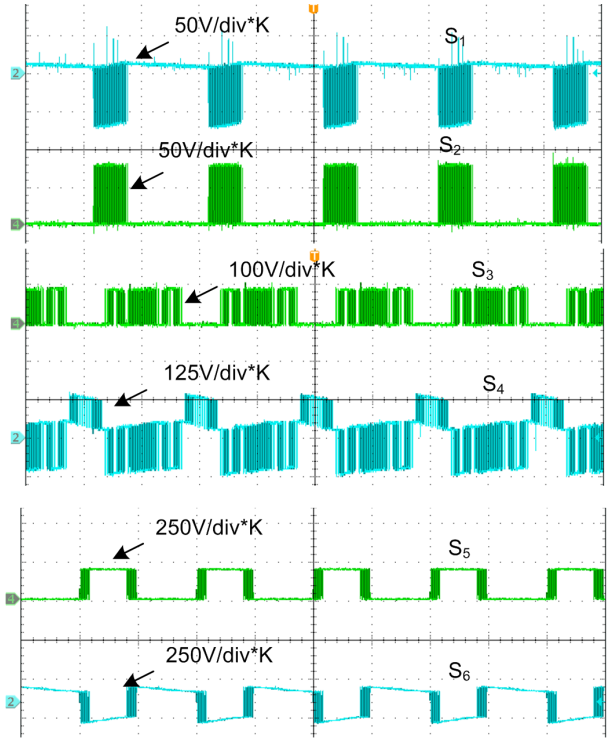


Fig. 11. Experimental results of voltage stress across switching devices S_1 to S_6.

TABLE III
FPGA RESOURCE UTILIZATION

Parameters	Open-loop PWM	PR controller	%
Slice Registers	24	191	0
Slice LUTs	203	153	0
Fully used LUT-FF pairs	16	50	24
Bonded IOBs	7	8	6
BUFG/BUGGCTRLs	1	1	12

C_3 is charged to the full magnitude of the 400 V DC input. Fig. 10 shows the response of the inverter output voltage and the corresponding load current as it changes from 2 A to 5 A while operating at 400 V. The expected pattern of output voltage and current is achieved, demonstrating that the developed five-level inverter is an optimal solution for PV applications in transformerless operation. Additionally, Fig. 11 shows the measured voltage stress on various switching devices.

B. HIL Co-Simulation: Grid Mode

Real-time testing of any circuit and control scheme is essential before the erection of any kind of power electronic converters for grid-connected PV applications. Hardware-in-the-loop (HIL) testing offers simple, cost-effective procedures and also saves time. Regarding cost-effectiveness, various FPGA boards from multiple vendors are available across a wide price range, typically from $100 to $400, and can be procured based on specific requirements such as telecommunications, automotive and aerospace, power electronics and motor control, renewable energy systems, and digital twin technology. In contrast, systems like Opal-RT, Typhoon HIL, and Microlab Box require expensive proprietary software for modeling, simulation, and HIL testing, increasing the overall cost. However, they may be preferred for industrial applications as they help optimize design and reduce development time. Therefore, in this work, hardware co-simulation is performed using the ATLYS SPARTAN 6 FPGA board connected with the HS2 Joint Test Action Group (JTAG) for interfacing the hardware and simulation environment as shown in Fig. 12. The JTAG easily communicates the signal between the MATLAB simulation and the FPGA hardware. The building blocks of the control schemes using the PR controller, PLL for synchronization, and gating pulses are very simple and take less time for easy implementation.

In order to realize the waveforms, the FPGA clock frequency of 100 MHz is scaled down appropriately to generate various signals. For example, to generate a sawtooth waveform with a frequency of 5 kHz, a count value of 2000 and an explicit period of 10 must be selected. Similarly, scaling can be adjusted as needed using Equation 1. Finally, the blocks are automatically converted into very high-speed integrated circuit hardware description language (VHDL) code generated by XSG [25], [26]. In general, XSG and HDL Coder are both tools for hardware design in MATLAB and Simulink, but they differ in ease of use and flexibility. XSG is a block-based tool, especially suitable for beginners who prefer graphical design. It simplifies the design process by reducing the need for coding and minimizing design effort, while still ensuring efficient FPGA implementation. It integrates seamlessly with Simulink, allowing for direct conversion of block diagrams into optimized HDL code, but it is limited to Xilinx hardware.

In contrast, HDL Coder provides a more versatile solution by converting MATLAB algorithms and Simulink models into generic VHDL or Verilog, supporting multiple FPGA vendors. While HDL Coder offers greater flexibility and control over the generated code, it requires more manual effort for optimization. Additionally, writing HDL code demands expertise in VHDL or Verilog and requires digital design, which can be more time-consuming due to manual design, verification, and increased complexity.

Moreover, the automatic code conversion process in Xilinx System Generator is highly efficient because of its smooth integration with Simulink and Xilinx blocks. System Generator automatically converts high-level Simulink designs into optimized HDL code, reducing manual coding effort. The hardware co-simulation feature enables real-time testing in Simulink, enhancing the accuracy of the FPGA implementation. This automatic code conversion process ensures faster and more efficient FPGA implementation compared to manual HDL coding. Overall, to achieve high performance with minimal development complexity, System Generator is more user-friendly for Xilinx-based designs, whereas HDL Coder is better suited for broader FPGA development requiring deeper customization.

To process various signals, the PWM generation and controller implementation utilize signed fixed-point data with a 32-bit format and a binary precision of 30 bits. Table III highlights the resources, such as slice registers, look-up tables (LUTs), Bonded IOB Pins, and general clock

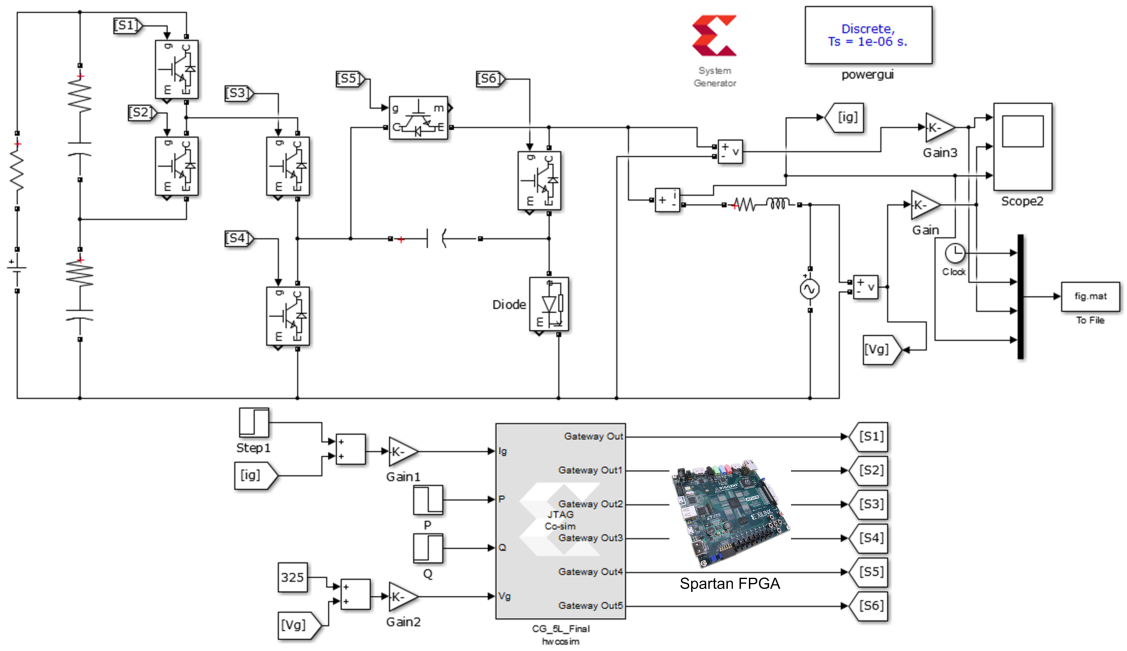


Fig. 12. FPGA based HIL co-simulation verification of proposed five-level inverter.

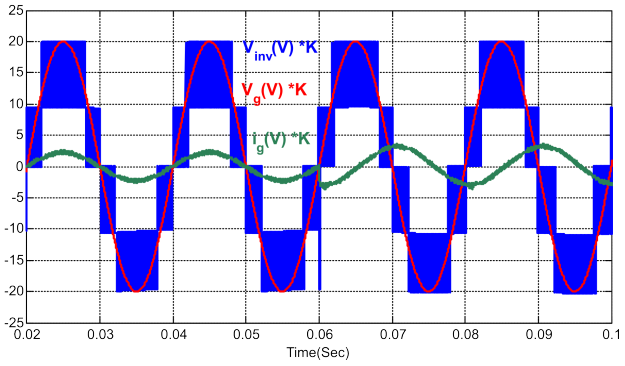


Fig. 13. Measured waveforms of inverter output voltage(V_{inv}), grid voltage(V_g), and injected grid current(i_g).

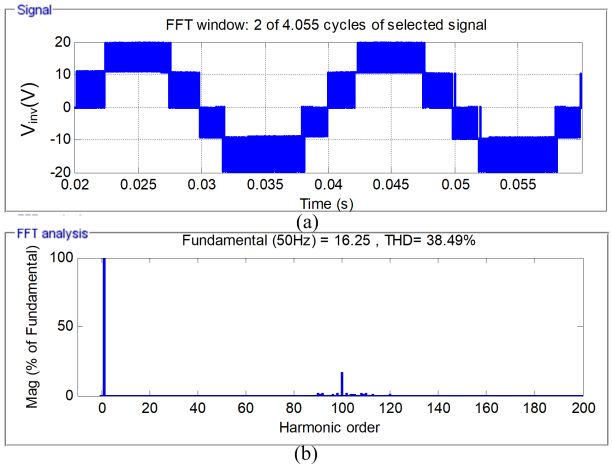


Fig. 14. Measured waveforms of (a) Inverter output voltage & (b) % THD_V.

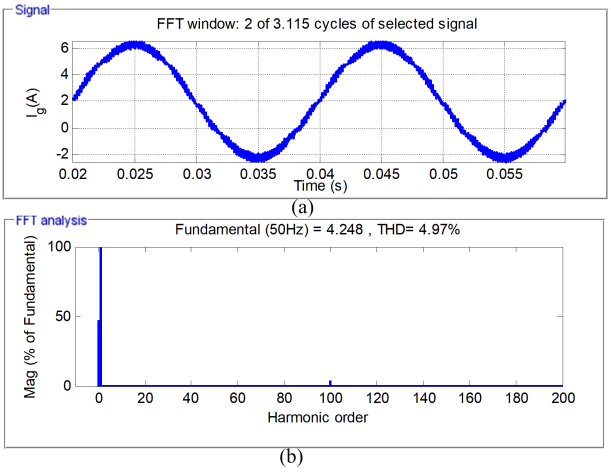


Fig. 15. Measured waveforms of (a) Injected grid current & (b) % THD_i.

buffers BUFG/BUGGCTRLs required for implementing both the open-loop response level generation and the PR controller, which regulates the injected grid current as per the design. It can be observed that the resource utilization for the real-time implementation of the system is minimal and highly efficient. Fig. 12 shows the developed five-level inverter with grid connection operation using Hardware Co-Simulation blocks consisting of 4 inputs and 6 output signals. The inputs consist of P, Q, Vg, and Ig sensed from the power circuit, whereas the 6 outputs feed the gating signals for the inverter.

Fig. 13 shows the five-level inverter output voltage, grid voltage, and the corresponding grid current waveforms. Here, the grid current changes from unity to lagging power factor at 0.06 seconds, and it is observed that both the inverter output voltage and grid voltage are synchronized and de-

TABLE IV
COMPARISON OF VARIOUS FIVE-LEVEL INVERTERS FOR PV APPLICATIONS

Topology	**No. of Components**						N_{max}	TSV_{pu}	**RPC**	I_x	**CGT**	**P**	$\%\eta$
	N_S	N_D	N_L	N_C	N_{dc}	N_{GD}							
[8]	8	0	1	3	1	8	5	5.5	-	Zero	Yes	1 kW	96.08%
[9]	8	0	1	3	1	8	5	13	Yes	Zero	Yes	1 kW	97%
[10]	10	0	1	2	1	10	7	-	Yes	Zero	Yes	0.6 kW	97.13%
[11]	7	2	0	2	1	7	3	6	Yes	Non-zero	No	0.7 kW	97%
[12]	8	2	0	4	1	8	3	7	-	Non-zero	No	1 kW	97.2%
[13]	6	0	0	3	1	6	3	6	Yes	Zero	Yes	1 kW	97.5%
[14]	6	1	0	3	1	6	3	6	Yes	Zero	Yes	1 kW	96.4%
[15]	9	0	0	2	1	9	5	6.5	Yes	Zero	Yes	1 kW	96.1%
[16]	4	3	2	2	1	4	3	7	Yes	Zero	Yes	0.5 kW	97.8%
[17]	6	1	0	3	1	6	3	5.5	Yes	Zero	Yes	1.1 kW	96.9%
[18]	9	0	0	1	1	9	6	9	-	Non-zero	No	0.6 kW	97.91%
[19]	8	1	0	2	1	8	5	6	Yes	Non-zero	No	0.5 kW	96.8%
[20]	8	1	0	2	1	8	4	6.5	Yes	Non-zero	No	1 kW	96.3%
[Proposed]	6	1	0	3	1	6	3	5.5	Yes	Zero	Yes	1 kW	98.7%

N_S=No. of semiconductor switches; N_D=No. of diodes; N_L=No. of inductors; N_C=No. of capacitors; N_{dc}=No. of dc sources; N_{GD}= No. of Gate Drivers; N_{max} =No. of maximum switches in conduction; TSV_{pu} =Total standing Voltage; RPC= Reactive Power Capability; I_x =leakage current; CGT = Common Ground Topology; $\%\eta$ = Efficiency; P= Power Rating.

veloped control regulates the injected current into the grid well. Furthermore, the developed single-phase PLL performs well for grid synchronization without any PI controller which is an added benefit of the inverter for grid-connected PV applications. It is also observed that only two signals, Vg and Ig, are required for the implementation of the control scheme during synchronization, which reduces the cost of the sensing circuits and the system.

Figs. 14 & 15 show the frequency spectra of the inverter output voltage and the injected grid current. For better understanding and visualization, these magnitudes are reduced with some gain. It can be noticed from the voltage waveform that the most dominant harmonic occurs at the switching frequency. It is also observed that the total harmonic distortion (% THD) of the current is around 4.97 %, which is below the IEEE 1547 standards [27]. This smoothens the current waveform due to the introduction of the filter inductor. Finally, it can be concluded that based on experimental and HIL results, the HIL results are on par with the experimental results and save time and cost of testing.

IV. COMPARATIVE ANALYSIS

Table IV provides a detailed comparison of various five-level inverter topologies based on components, total standing voltage (TSV), reactive power capability, leakage current, common-mode features, and efficiency. Although some studies [8]-[20] mention topologies with a common ground feature, reduced TSV, and good efficiency above 96 %, these topologies have a higher device count, leading to increased system size and cost. In contrast, the proposed topology has the fewest switching devices and achieves an efficiency of 98.7 % for a 1 kW power rating, as verified through PLECS simulation software. For a fair comparison, the efficiency estimates are made with most topologies based on the PLECS model, using a power device loss model derived from real-time data obtained from the device manufacturer, as well as from theoretical analysis based on conduction losses, switching losses, and capacitor ripple losses proposed in [28]. It is evident that the reported efficiency is high and mainly due to a maximum of three devices being in conduction. Additionally, the topology's TSV, which is approximately 5.5, provides an added advantage. The inclusion of a common ground feature eliminates the need for a bulky isolated transformer to mitigate leakage current between the PV panels and the grid. Therefore, the proposed transformerless five-level inverter for grid-connected PV applications presents a superior solution compared to other topologies.

V. CONCLUSION

This paper presents low-cost FPGA-controlled HIL co-simulation for rapid prototyping of a single-phase five-level transformerless inverter for PV applications. The control platforms developed in MATLAB using Xilinx blocks make the system simple and easier to implement, realizing the system's dynamics during grid interface. Experimental results demonstrate the superiority of the proposed topology with the merits of 100 % DC input, soft charging capability, and the ability to deliver both real and reactive power support. Moreover, in the proposed topology, a maximum of three switches are in conduction during level generation, resulting in higher efficiency of 98.7 % for a 1 kW power rating compared to other recently proposed topologies in the literature. Finally, it is evident that the common ground feature makes the proposed topology most preferred for PV applications.

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