Bidirectional Step-Up Multi-Input Converter with Improved Voltage Gain for DC Microgrids

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***Abstract*— High-gain converters are widely used in industrial and commercial applications, particularly in high-power systems such as Fuel Cell Electric Vehicles (FCEVs) and grid-connected Renewable Energy Sources (RES). However, high-gain topologies derived from a single energy source often suffer from reliability issues in RES applications due to increased component stress and device count. In the event of a source failure, these designs can lead to energy supply disruptions. To address this challenge, integrating multiple energy sources with step-up voltage capability presents a promising solution for both DC microgrid and Electric Vehicle (EV) applications. This study proposes a Dual-Input Single-Output (DISO) converter designed to integrate multiple energy sources while achieving high voltage gain, equivalent to 5 times the input voltage. The converter operates by charging the inductors in parallel and discharging them in series, enhancing the overall voltage boost. Additionally, in the event of a source failure, the converter can seamlessly supply power to the load using the available source. It also supports bidirectional operation, further improving system flexibility and reliability. The paper provides a comprehensive theoretical analysis, covering circuit modeling, design considerations, and performance evaluation. Furthermore, a comparative analysis with other converter topologies is presented. The proposed converter is validated through experimental results obtained from a 250 W laboratory prototype and demonstrating an efficiency of 92.37%.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9579

***Index Terms*— Energy, multiport, multi-input single output (MISO) configuration and bidirectional.**

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I. Introduction

THE growing use of alternative energy sources like wind, solar, and fuel cells in power generation systems highlights the need for DC-DC converters to regulate voltage in renewable energy integration [1], [2]. Due to the sensitivity of these energy sources to environmental conditions, it is essential to design efficient power converters that can handle multiple energy sources [3]. Recent research has focused on the design configurations of multi-input converters (MICs) to overcome the limitations of single-input converters [4]. Furthermore, multi-input converters (MICs) offer a more compact and lightweight design by removing redundant components, improving power flow management, and providing greater flexibility to integrate sources with varying voltage levels.

In [5], double-input step-up converters with parallel and series switched-diode-capacitor cells offer high voltage gain, low ripple, and reduced device stress. However, they lack bidirectional operation and a common ground, leading to high electromagnetic interference (EMI). A two-input buck converter with a single switch and inductor is proposed in [6], [7], offering a compact design, high efficiency, and low voltage stress. However, its main limitation is the restricted output voltage range and lack of bidirectional operation. In [8], a MISO converter using buck-boost and boost converters is proposed to enhance voltage gain. In [9], adding a switched capacitor (SC) cell improves voltage gain and reduces stress. In [10], a high step-up MISO DC-DC converter enables bidirectional operation and continuous input current, extendable to N-inputs. However, the increased component count raises system costs.

In [11], a multiplier circuit and coupled inductor improve voltage gain and enable independent control, simplifying the control circuit. However, leakage flux in the coupled inductor causes conduction losses, reducing efficiency. The converter in [12] features two unidirectional ports, a bidirectional battery port, and a DC link with low device stress. However, its high component count may increase cost and size. The topology in [13] employs series-connected switched capacitors to mitigate partial shading and PV module mismatches, achieving soft switching without extra components, thereby enhancing converter efficiency. However, the increased device count may raise costs. In [14], the proposed converter integrates voltage gain techniques to achieve a 21.11 gain with efficient current sharing in parallel high gain converters. However, the higher device count may increase costs. In [15], the converter

uses an input inductor and switched capacitors for continuous input current and voltage gain. However, more components and diodes increase conduction losses, reducing efficiency.

The topology in [16] provides high voltage gain, low output ripple, and scalability for N-input hybrid energy systems. However, it has voltage gain limitations. The MIMO converter in [17] employs a diode-capacitor voltage multiplier to enhance voltage gain and reduce semiconductor stress; nevertheless, it increases component count and complexity. The DIDO converter with a switched-inductor-capacitor (SLC) achieves high voltage gain with a low duty ratio and reduced peak voltage stress in [18]. Nevertheless, increases complexity due to extra components and the absence of a common ground between the source and load. The DIDO converter with a Z-Quasi Resonant network, as presented in [19], is utilized to achieve step-up voltage for EV applications. A MISO converter based on the SEPIC topology [20] and the switched-inductor technique [21] are used to improve voltage gain at low duty cycle operation. However, bidirectional operation is not addressed. A DISO converter with a zero-voltage turn-off auxiliary circuit [22] enables soft switching across varying loads, reducing losses and enhancing efficiency. Nevertheless, requires more components and has a low voltage conversion ratio. A switched-inductor-capacitor-based single-switch step-up MISO converter is presented in [23], featuring fewer components to reduce cost. However, it experiences high semiconductor stress. A single-switch MISO converter in [24] enhances voltage gain using an inductor-capacitor cell. Nevertheless, it has higher component count, no common ground, and lacks bidirectional operation. The voltage multiplier cell used in [25] achieves twice the voltage gain of a conventional boost converter while reducing power switch voltage stress by half. However, lack of bidirectional operation. Bidirectional DISO converter are suggested in [26], [27] with reduced part count and support the bidirectional operation.

Summarizing findings from existing literature, the limitations of MISO converter topologies are as follows

- Some configurations have few components, leading to compact size and cost-effectiveness. However, offers low voltage conversion.
- Improving voltage gain often results in a higher component count.
- The lack of bidirectional functionality.
- The absence of a common ground between the load and source causes EMI.
- Limited in scalability to multiple inputs (N-inputs).
- Lack of source fault-tolerant

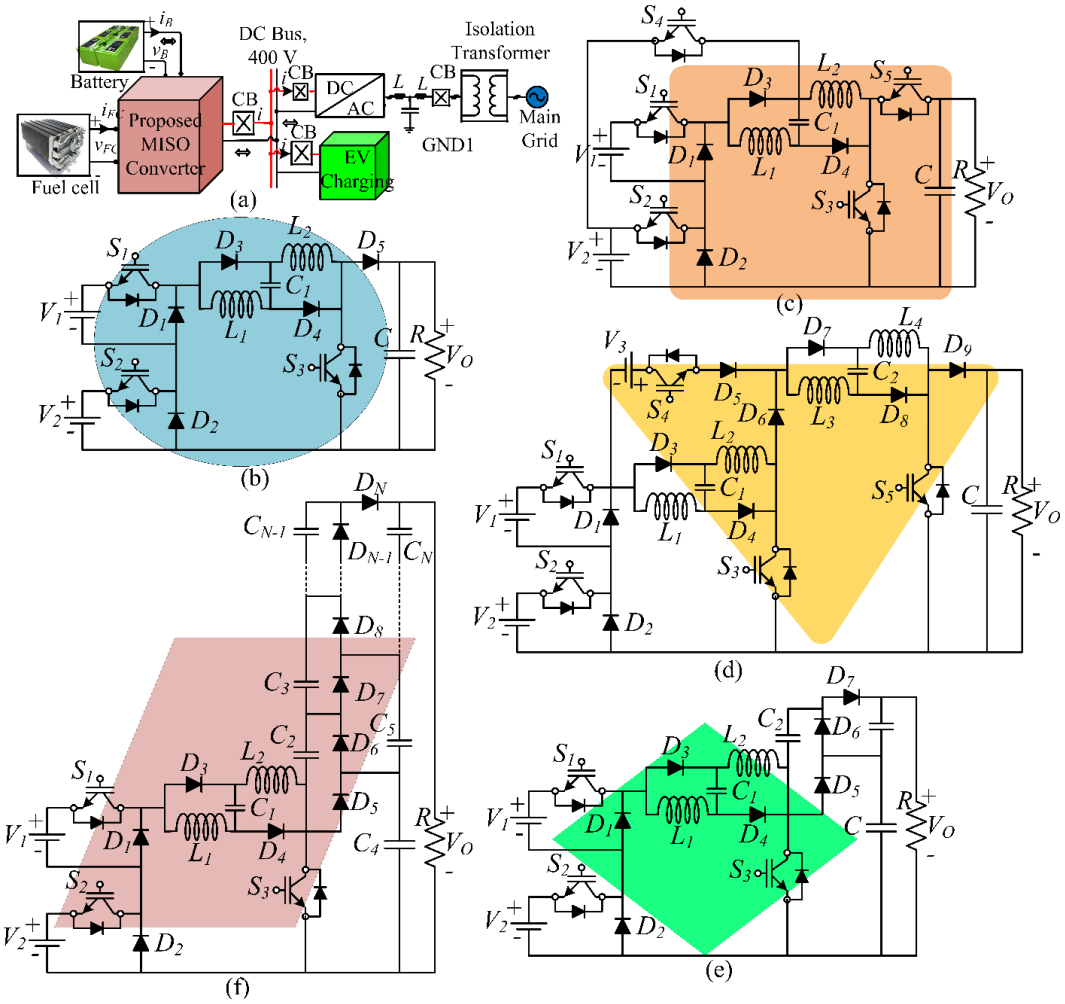


Fig. 1. Circuit of the: (a) DISO application, (b) Proposed DISO converter, (c) Extended for bidirectional mode, (d) Extended multiple input, (e) Extended extra voltage gain, and (f) Extended for ultra voltage gain.

The paper is structured as follows: the proposed structure and its operations are outlined in Section II, while Section III covers the small-signal modeling. Section IV discusses parameter design considerations, loss analysis, stress analysis, and comparative evaluation. Results and discussions presented in Sections V and VI concluding the study.

II. Proposed Configuration and Operation

The MISO application and the proposed step-up DISO topology are illustrated in Fig. 1(a) and (b), respectively. The configuration includes power IGBTs (S_1-S_5), diodes (D_1-D_4), inductors (L_1, L_2), capacitors (C, C_1), two input sources (V_1, V_2), a load (R), load current (I_O), and output voltage (V_O). Voltage gain is enhanced by utilizing energy-storing components. During the turn-ON period, passive components are charged in parallel by the input supply, while in the turn-OFF period, the stored energy is delivered to the load. Fig. 1(c) and 1(d) illustrate the extension of the proposed converter for bidirectional operation and an N-input version. Additionally, modifications for achieving high and ultra-high voltage gains are shown in Fig. 1(e) and (f). The current flow paths for buck-boost, boost, and bidirectional operation are depicted in Fig. 2-4 respectively. The proposed design is well-suited for microgrids and EV powered by fuel cells. It offers the following benefits:

- Simple design with a minimal number of components, ensuring cost-effectiveness.
- Enhanced voltage gain capabilities.
- Supports multi-input operations in buck (BU), boost (BO), and buck-boost (BB) modes.
- Capable of operating either individually or simultaneously.
- Extendable to accommodate N-inputs and achieve ultra-high voltage gain.
- Source fault-tolerant capability
- Support for bidirectional operation

A. Operating Modes in Buck-Boost Mode

Mode 1: In this mode, the inductors are energized, and capacitor C_1 is charged by the input source (V_1) through switches (S_1, S_3) and diodes (D_2, D_3, D_4), as shown in Fig. 2(a). Meanwhile, capacitor (C) discharges its stored energy to the load (R). The inductor and capacitor voltages are given in Eq. (1).

$$V_{L_1} = L_1 \frac{di_{L_1}}{dt} = V_1; \quad V_{L_2} = L_2 \frac{di_{L_2}}{dt} = V_1, \quad V_{C_1} = V_1 \tag{1}$$

Mode 2: The inductors are energized, and capacitor (C_1) is charged by the supply ($V_1 + V_2$) through switches (S_1, S_2, S_3) and diodes (D_3, D_4). Meanwhile, capacitor (C) discharges its stored energy to the load (R). The circuit operation in this mode is depicted in Fig. 2(b), with the corresponding Eq. (3) provided below.

$$V_{L_1} = L_1 \frac{di_{L_1}}{dt} = V_1 + V_2; \quad V_{L_2} = L_2 \frac{di_{L_2}}{dt} = V_1 + V_2, V_{C_1} = V_1 + V_2 \tag{2}$$

Mode 3: In this mode, switches (S_2 and S_3) are turned ON, while the remaining switches are OFF, and diodes (D_1, D_3, and D_4) are forward biased, as illustrated in Fig. 2(c).

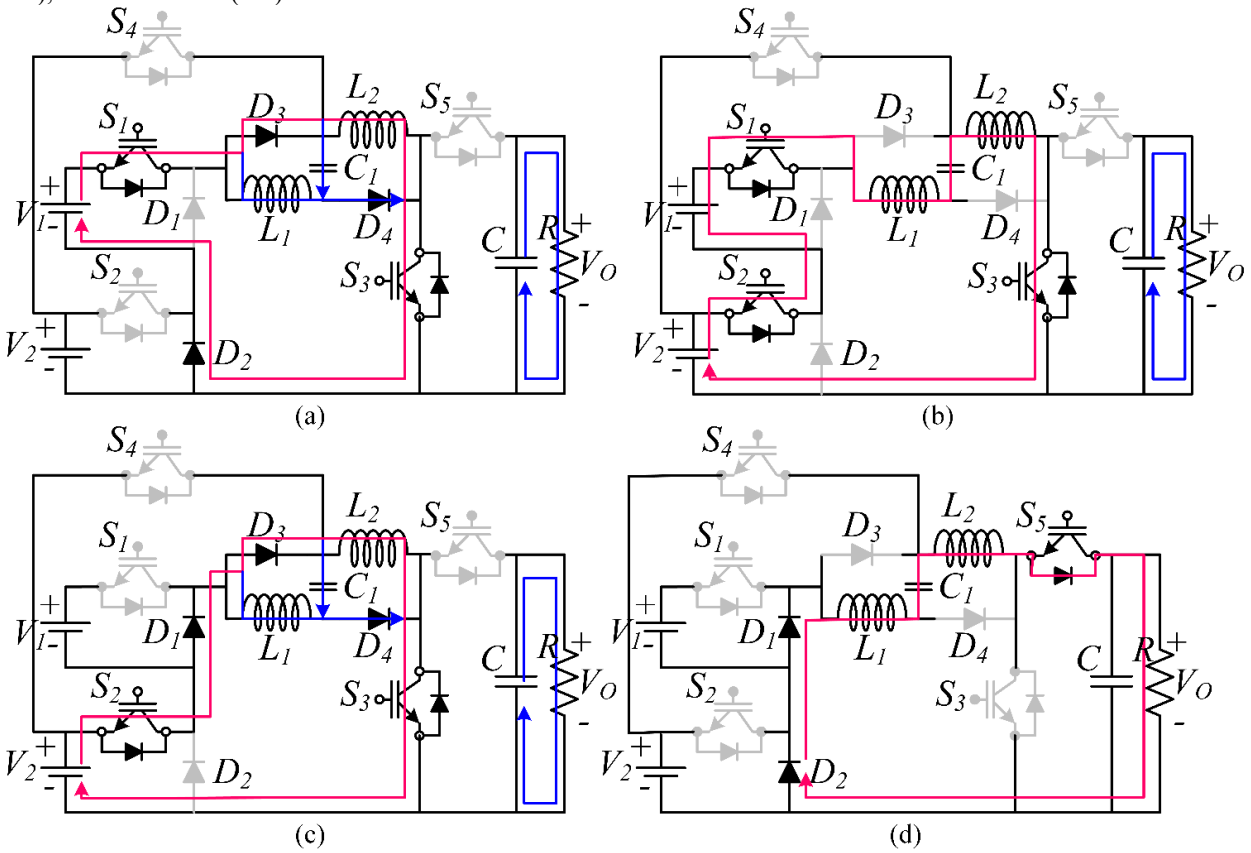


Fig. 2. Buck-boost Operating Modes: (a) Mode-1, (b) Mode-2, (c) Mode-3, and (d) Mode-4.

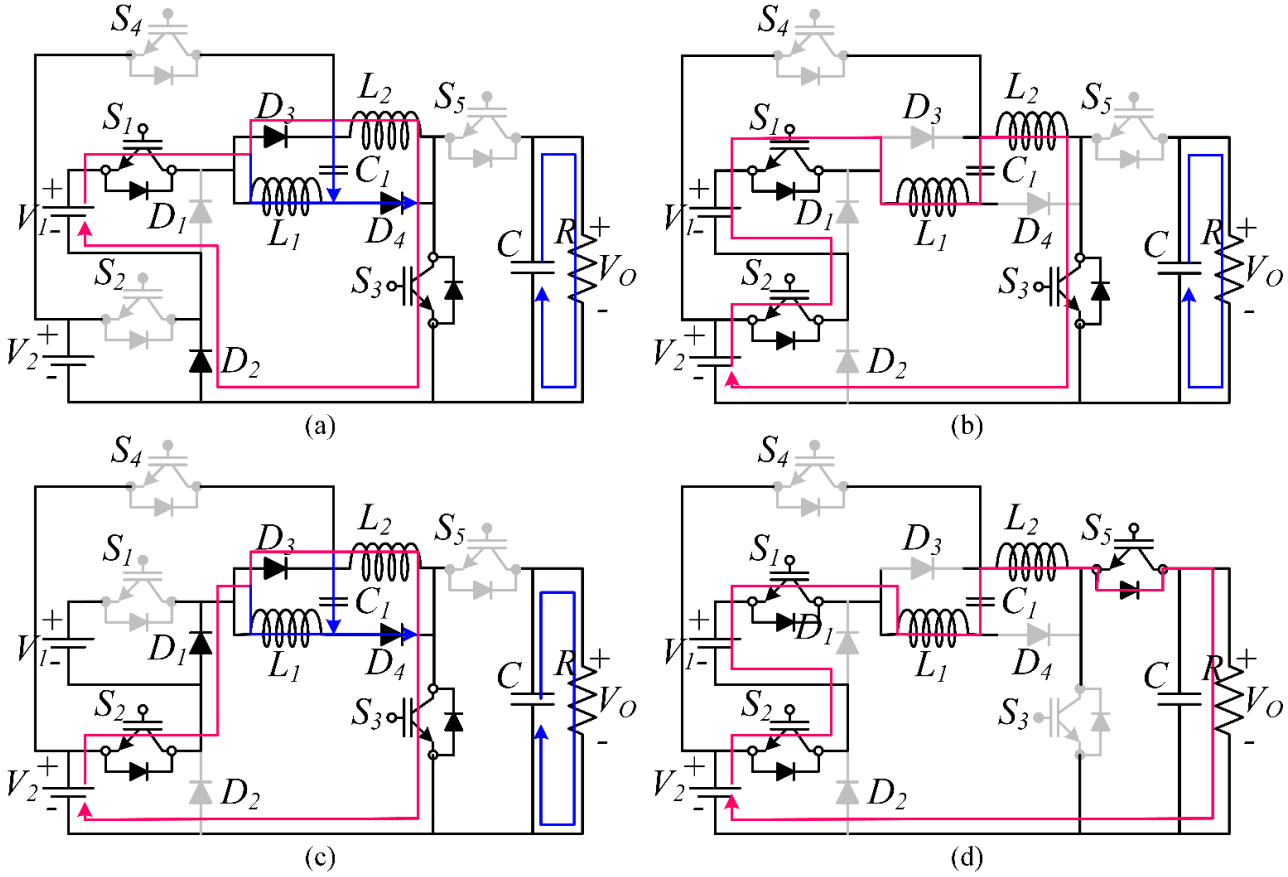


Fig. 3. Boost operation: (a) Mode-1, (b) Mode-2, (c) Mode-3, and (d) Mode-4.

The inductors and capacitor C_1 are energized by the source (V_2). The capacitor and inductor voltages are given in Eq. (3).

$$V_{L_1} = L_1 \frac{di_{L_1}}{dt} = V_2;\ V_{L_2} = L_2 \frac{di_{L_2}}{dt} = V_2,\ V_{C_1} = V_2 \tag{3}$$

Mode 4: The input source, along with the energy-stored inductors and capacitor C_1, are connected in series, supplying their stored energy to the load through diodes (D_1, D_2) and the body diode of switch (S_5), as shown in Fig. 2(d). The voltage across the inductor is derived as in Eq. (4).

$$V_{L_1} = V_{L_2} = \frac{V_{C_1} - V_0}{2} \tag{4}$$

$$V_{0\_BB} = \frac{2\left[V_1 d_1 + (V_1+V_2)d_2 + V_2 d_3\right] + V_{C_1}(1 - d_2 - d_2 - d_3)}{\left(1 - d_1 - d_2 - d_3\right)}$$

$$V_{0\_BO} = \frac{2\left[V_1 d_1 + (V_1+V_2)d_2 + V_2 d_3\right] + (V_1 + V_2 + V_{C_1})(1 - d_2 - d_2 - d_3)}{\left(1 - d_1 - d_2 - d_3\right)} \tag{5}$$

$$V_{0\_BU} = 2\left[V_1 d_1 + (V_1+V_2)d_2 + V_2 d_3\right] + (V_1 + V_2 + V_{C_1})(1 - d_2 - d_2 - d_3)$$

Where in Eq. (5), V_{0_BB}, V_{0_BB}, and V_{0_BU} represent the output voltages in buck-boost, boost and buck modes of operation respectively, while 'd_1, d_2, and d_3' represent the duty cycle of their corresponding switches.

B. Bidirectional Mode

In bidirectional operation, the load (R) functions as the input source (V_0), while the input voltage (V_2) acts as the load. The respective operating modes and current paths are illustrated in Fig. 4. The output voltage is provided by Eq. (6).

$$V_2 = V_0 \times d \tag{6}$$

C. Source Fault-tolerant Condition

The proposed converter features source fault tolerance, enabling it to continuously supply energy to the load even if either source V_1 or V_2 fails.

V_2-Out of Working Condition: In this scenario, when source (V_2) is not operational, the available source (V_1) supplies energy to the load. The corresponding mode of operation and current path are illustrated in Fig. 5, and the output voltage expression is provided in Eq. 7.

$$V_0 = \frac{2V_1}{1-d} \tag{7}$$

V_1-out of working condition: In this mode of operation, source (V_1) is considered the failed source, and the available source (V_2) supplies energy to the load, as depicted in Fig. 6. The output voltage is given by Eq. 8.

$$V_0 = \frac{2V_2}{1-d} \tag{8}$$

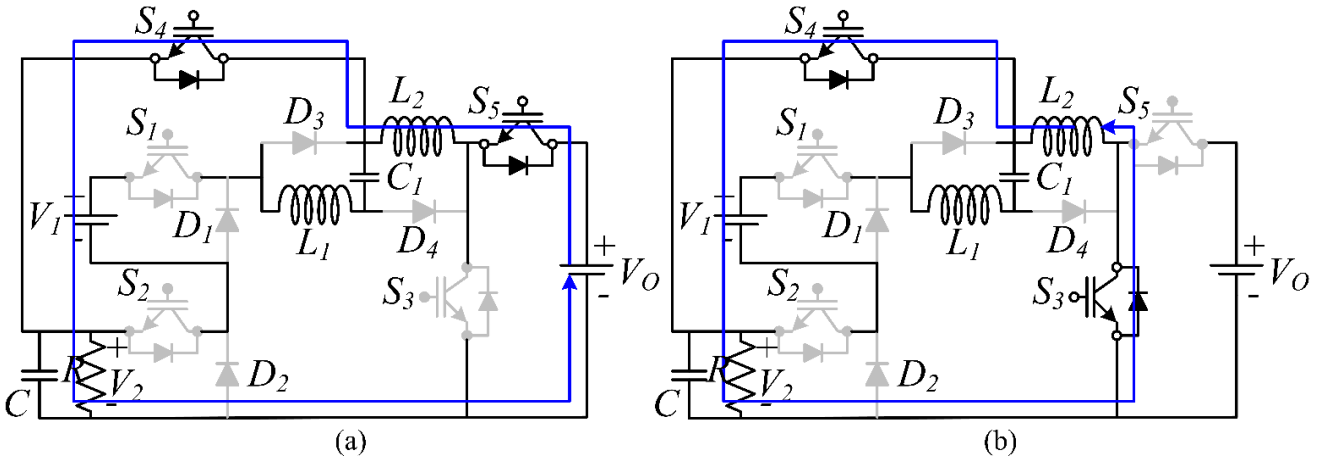


Fig. 4. Bidirectional operation: (a) Mode-1, (b) Mode-2, (c) Mode-3, and (d) Mode-4.

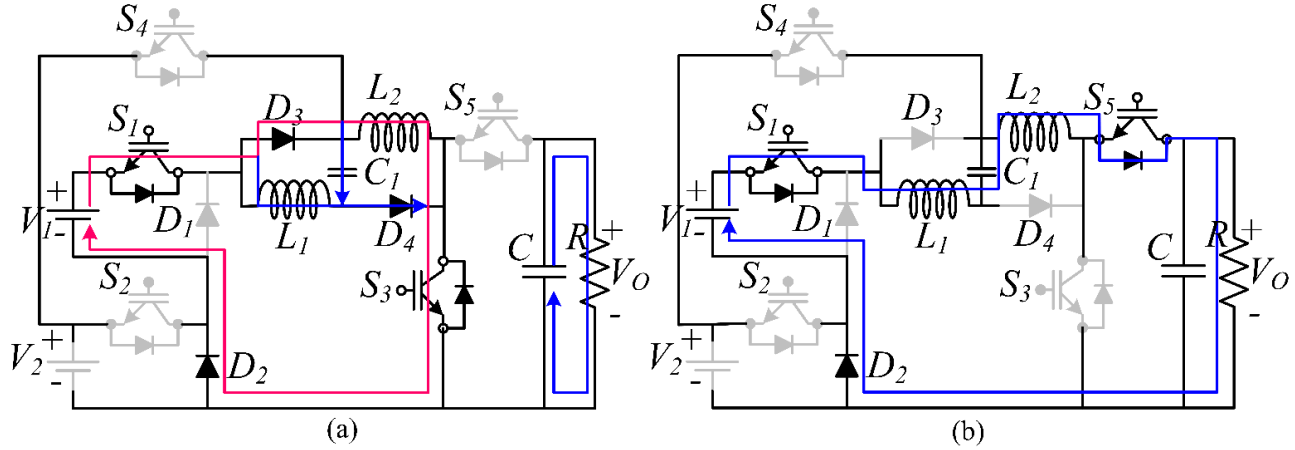


Fig. 5. Current path in V_2-failure case: (a) Mode-1 and (b) Mode-2.

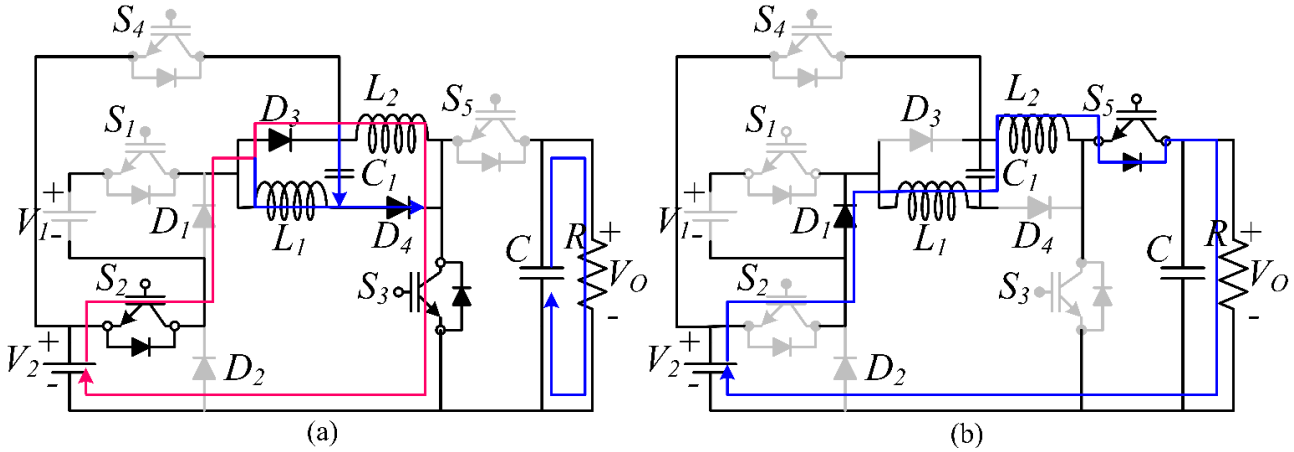


Fig. 6. Current path in V_1-failure case: (a) Mode-1 and (b) Mode-2.

III. SMALL-SIGNAL MODELING

The converter's transfer function is developed from small-signal analysis, as described in [28]. The dynamic equations of the converter are as follows in eq. [9-16],

$$\begin{aligned} \dot{x}(t) &= Bx(t) + Cu(t) \\ y(t) &= Dx(t) + Eu(t) \end{aligned} \tag{9}$$

u(t)=input matrix, y(t)=output matrix and x(t)=state matrix. In a complete switching cycle, the state and output equations are expressed as follows:

$$\dot{x}(t) = B_n x(t) + C_n u(t), y(t) = D_n x(t) + E_n u(t) \tag{10}$$

$$\dot{x}(t) = dB_1 x(t) + (1 - d)B_2 x(t) + dC_1 u(t) + (1 - d)C_2 u(t) \tag{11}$$

$$y(t) = dD_1 x(t) + (1 - d)D_2 x(t) + dE_1 u(t) + (1 - d)E_2 u(t) \tag{12}$$

The state equation in matrix form is as follows.

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_C(t) \\ v_{C1}(t) \end{bmatrix} = A\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_C(t) \\ v_{C1}(t) \end{bmatrix} + BV_{DC} \tag{13}$$

$$B=\begin{bmatrix} 0 & 0 & 0 & -\left(\frac{1-d_1-d_2-d_3}{L_1+L_2}\right) \\ 0 & 0 & 0 & -\left(\frac{1-d_1-d_2-d_3}{L_1+L_2}\right) \\ 0 & 0 & 0 & 0 \\ -\left(\frac{1-d_1-d_2-d_3}{(L_1+L_2)C}\right) & -\left(\frac{1-d_1-d_2-d_3}{(L_1+L_2)C}\right) & 0 & -\left(\frac{1-d_1-d_2-d_3}{(L_1+L_2)RC}\right) \end{bmatrix} \quad (14)$$

$$C=\begin{bmatrix} \frac{V_1d_1+(V_1+V_2)d_2+V_2d_3}{L_1}+\frac{V_{C1}(1-d_1-d_2-d_3)}{L_1+L_2} \\ \frac{V_1d_1+(V_1+V_2)d_2+V_2d_3}{L_2}+\frac{V_{C1}(1-d_1-d_2-d_3)}{L_1+L_2} \\ V_1d_1+(V_1+V_2)d_2+V_2d_3+V_{C1}(1-d_1-d_2-d_3) \\ 0 \end{bmatrix} \quad (15)$$

$$D=\begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \quad (16)$$

The regulation of the 'V_0' is achieved by adjusting the duty ratio, as shown in eq. (17) and (18).

$$\hat{v}_0(s)=G_{vd}\hat{d}(s) \quad (17)$$

$$\frac{\hat{v}_0(s)}{\hat{d}(s)}=\frac{\begin{bmatrix} s^3RC+S^2\frac{(L_1+L_2)}{RC}+SR^2C(L_1+L_2) \\ \left(\frac{V_1d_1+(V_1+V_2)d_2-V_{CV}(1-d_1-d_2-d_3)}{L_1+L_2}\right) \end{bmatrix}}{\begin{bmatrix} s^4RC(L_1+L_2)+s^3\frac{(L_1+L_2)}{RC}+s^2\left(\frac{1}{RC}\right)-s\left(\frac{(L_1+L_2)^2}{R}+\frac{C}{R}\right) \\ (1-d_1-d_2-d_3)^2+(RC)(L_1+L_2)+\frac{(1-d_1-d_2-d_3)^2}{RC} \end{bmatrix}} \quad (18)$$

The frequency response is shown in Fig. 7. From the bode a plot gain margin of 21.7 dB and a phase margin of 3.87^0.

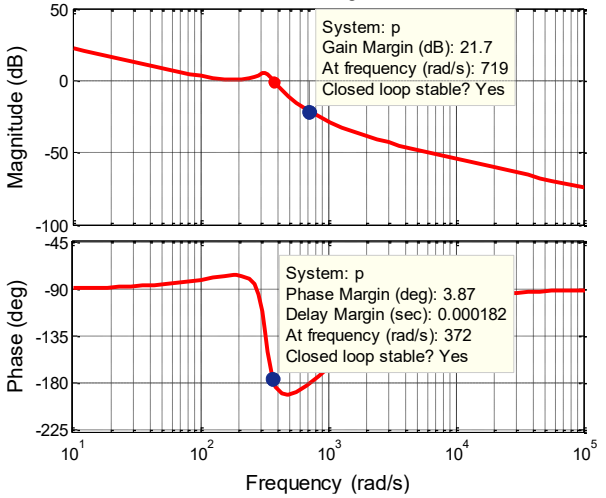


Fig. 7. Bode plot illustrating the frequency response of the system.

IV. Analysis of the Proposed Converter

A. Effect of Parasitic Resistances and Loss Analysis

Fig. 8 shows the converter configuration inclusive of parasitic resistances. Specifically, $r_{S1\text{-}3}$ is the switch on-state resistance, while $r_{D1\text{-}5}$ pertain to the diode forward resistances of $D_{1\text{-}5}$ respectively. Additionally, $r_{L1\text{-}2}$ denotes the equivalent series resistance of the inductors L_1-L_2. r_{C1}, r_C are series resistance of the C_1 and C respectively.

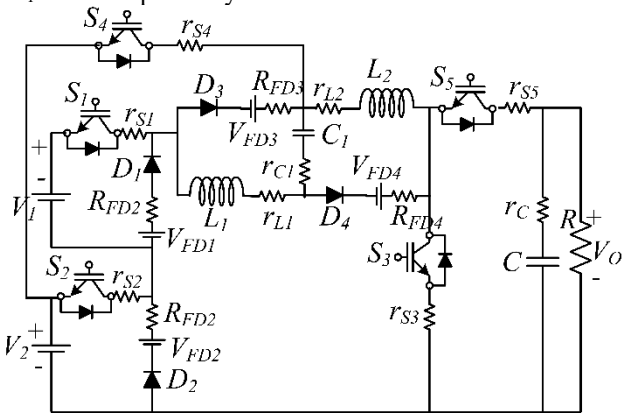


Fig. 8. Equivalent circuit of the proposed configuration including parasitic components.

D. Loss Analysis

The loss analysis is important in optimizing the design of the power converter. Additionally, there is a need to calculate the efficiency [29]. The loss analysis for the proposed structure is described as follows in eq. (19-24). The switch conduction loss (P_{con}):

$$P_{con}=\left(V_{CE\_S}I_{avg\_S}+r_{DS\_(on)}I^2_{rms\_S}\right) \quad (19)$$

$V_{S,}$ represent the collector-emitter saturation voltage, I_{avg_S} denote switch current, I_{rms_S} *is* the rms value of switch current and $r_{DS\_(on)}$ refers to the ON-state resistance of the switch, which is 0.06mΩ.

The switching losses are:

$$P_{SW}=\frac{1}{6}V_SI_sf_S\left(t_{on}+t_{off}\right) \quad (20)$$

where, 't_r' and 't_f' denote the rise and fall times of the switch.

The power dissipation caused by the diode's offset voltage V_D is as follows:

$$P_{V_D}=V_DI_{0max},\quad P_{V_D}=\frac{V_DP_0}{V_0} \quad (21)$$

'V_D' represent the diode forward voltage and I_{0max} is the max load current

The power dissipation caused by the forward resistance r_D is

$$P_{r_D}=r_DI^2_{Drms},\quad I_{Drms}=\frac{I_{0max}}{\sqrt{(1-D_{max})}},\quad P_{r_D}=\frac{r_DP_0}{(1-D)R_L} \quad (22)$$

r_D denote the forward resistances of the diode, I_{rms_D} *is* the rms value of diode current and load resistance is R_L

The inductor loss:

$$\begin{aligned} P_L&=P_{cu}+P_{core} \\ P_L&=r_LI^2_{rms}+kB^{\alpha}_{\max}f^{\beta}V \end{aligned} \quad (23)$$

where: P_{core} represents core losses, P_{cu} denotes copper losses, Irms is the RMS current through the inductor, r_L is the equivalent series resistance, k, α, β are Steinmetz coefficients, B_{max} refers to the maximum flux density in the core (T), f is the switching frequency (Hz), and V is the core volume (m^3).

The capacitor loss:

$$P_{rC}=\frac{r_C(d_1+d_2+d_3)P_0}{(1-d_1-d_2-d_3)R_L} \quad (24)$$

The complete power dissipation in the suggested converter is in Eq. (25).

$$P_{loss} = P_{con} + P_{SW} + P_{V_D} + P_{r_D} + P_{rL} + P_{rC} \quad (25)$$

$$\eta = \frac{P_0}{P_0 + P_{loss}} \quad (26)$$

E. Calculation of Voltage Stress

The voltage experienced by the switches (S_1-S_3, S_5) and (D_1-D_4) in the suggested configuration while operating in the buck-boost mode, as specified in eq. (27), is detailed in reference [29].

$$V_{S_1} = V_{D_1} = V_1, V_{S_2} = V_{D_2} = V_2$$
$$V_{D_3} = V_{D_4} = \frac{V_0}{2}, V_{S_3} = V_{S_5} = V_0 \quad (27)$$

F. Converter Parameters Design

This subsection provides an elaboration on the design of the components employed in the converter. However, detailed deception and design procedure as follows in [29]. The parameter details are presented in Table I.

The design of inductance parameter is in eq. (28):

$$L_{1min} = L_{2min} = \frac{2}{27}\frac{R_{Lmax}}{f_s} \quad (28)$$

Inductor ripple current is in eq. (29)

$$\Delta i_{L_1 max} = \Delta i_{L_2 max} = \frac{D_{min}(1 - D_{min})V_0}{f_s L} \quad (29)$$

The determination of the capacitance value in eq. (30):

$$C_{min} = \frac{D_{max} V_0}{V_{cpp} R_{Lmax} f_s} \quad (30)$$

Where, D_{max} = Maximum duty cycle, R_{Lmax} = load resistance, V_{cpp}=capacitor ripple voltage and ripple voltage (V_r) is 1% V_0.

$$V_{cpp} = \frac{V_r}{2} \quad (31)$$

TABLE I
SPECIFICATIONS OF THE PROPOSED CONVERTER

Parameter	Simulation	Experimental
V_1, V_2	20, 10 V	20, 10 V
L_1, L_2	4, 4 mH	4, 4 mH
f_S	10 kHz	10 kHz
C_1, C	360, 470 uF	360, 470 uF
V_0	135 V	135 V
I_0	1.85 A	1.85 A

G. Comparative Analysis

A comparative analysis of the proposed converter and other recently introduced converters is provided in Table II.

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH EXISTING MISO CONVERTER

Reference	S/D/L/C	Total components	Operation mode	Facility to integrate to inputs	Bidirectional operation	Common ground	Source fault-tolerant	Output voltage	Max. Voltage Stress
[5]	2/4/2/5	13	Boost	Yes	No	No	No	$V_0 = \frac{2(U_{in1}+U_{in2})}{(1-D)}$	$\frac{U_{in1}}{(1-D)}$
[9]	2/4/2/4	12	Boost	Yes	No	No	No	$V_0 = \frac{V_{in}(2-d+d^2)}{(1-d)^2}$	$\frac{V_O}{(2-d+d^2)}$
[19]	2/1/4/2	9	Boost	Yes	No	Yes	No	$V_0 = \frac{(1-d_1)V_{in1}}{(1-2d_1)}$	$\frac{V_{in}}{(1-2D)}$
[20]	4/1/2/2	10	Boost	Yes	No	Yes	No	$V_0 = \frac{d_1+d_2+d_3}{(1-d_1+d_2+d_3)} \times \frac{V_1(d_1+d_3)+V_2(d_2+d_3)}{1-d_1-d_2-d_3}$ $(V_1(d_1+d_3)+V_2(d_2+d_3))$	
[21]	3/5/2/1	11	Boost	Yes	No	Yes	No	$V_0 = \frac{V[2d(1-k)+k(1+d_m)]}{(1-d_m)}$	V_0
[22]	2/8/2/6	18	Boost	Yes	No	Yes	No	$V_0 = \frac{2V_{in2}}{(1-d_2)} + \frac{2V_{in1}}{(1-d_1)}$	$\frac{V_{in1}}{(1-D_{S1})}$
PRO.	5/4/2/2	13	Boost, Buck, Buck-Boost	Yes	Yes	Yes	Yes	Eq. (5)	V_0

The comparison covers factors such as the number of power semiconductor devices, inductors, capacitors, and operational conditions. Although the total component count of the proposed converter is higher than those in [9], [19–21], it is lower than in [5] and [22]. However, the converters in these references lack bidirectional operation, are restricted to boost mode, and provide low voltage gain. In contrast, the proposed converter supports boost, buck, and buck-boost modes, offers bidirectional functionality, source fault-tolerant capability and has a common ground between the source and load, which results in low EMI. Additionally, it can be expanded to accommodate N-inputs and achieve ultra-high voltage gain.

V. RESULTS AND DISCUSSIONS

A. Validation through Simulation

The performance of the converter is validated using MATLAB/Simulink, with detailed results presented in Table I. The input voltages are set as V_1 = 20 V and V_2 = 10 V, with a switching frequency of 10 kHz and duty cycles of d_1 = 30%, d_2 = 30%, and d_3 = 10%. The proposed converter is tested under boost, buck-boost, and buck operating modes. Fig. 9(a) illustrates the output voltage (V_O), inductor currents (i_{L1} and i_{L2}), and voltage across capacitor (V_{C1}) in buck-boost mode, where the output voltage reaches 135.3 V, aligning with theoretical predictions. The converter's performance in boost and buck modes is further demonstrated in Fig. 9(b) and 9(c), respectively.

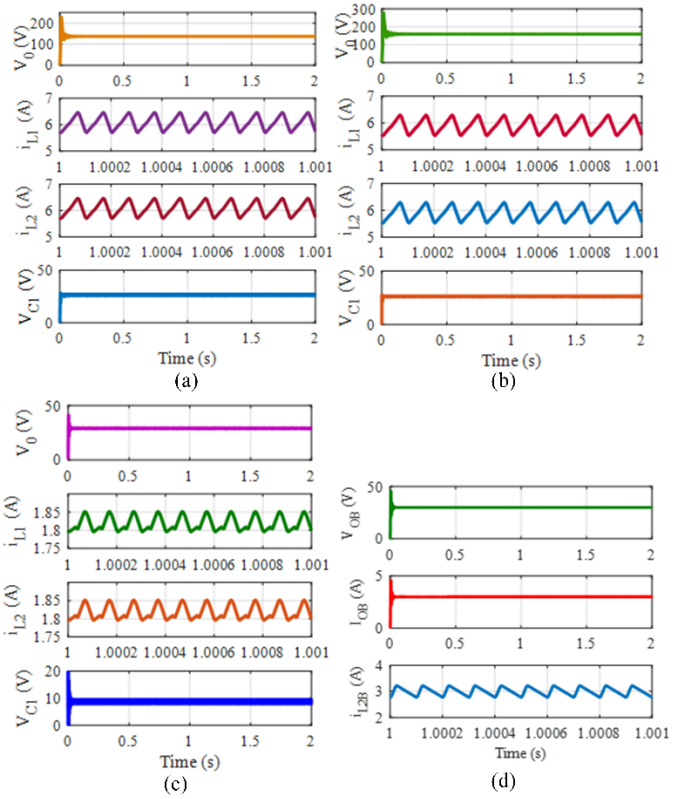


Fig. 9. Simulation results of output voltage (V_O), inductor currents (i_{L1} and i_{L2}), capacitor voltage (V_{C1}) of the proposed converter operating in different modes: (a) buck-boost mode, (b) boost mode, (c) buck mode and (d) output voltage (V_{OB}), load current (I_{OB}) and inductor current (i_{L2B}) in bidirectional mode.

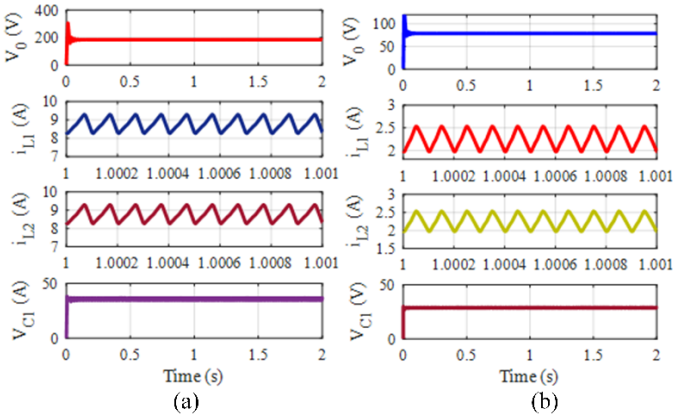


Fig. 10. Simulation result of output voltage (V_O), inductor currents (i_{L1} and i_{L2}), capacitor voltage (V_{C1}) in buck-boost mode at different set of input voltages and duty ratio: (a) different input voltages and (b) different duty ratios.

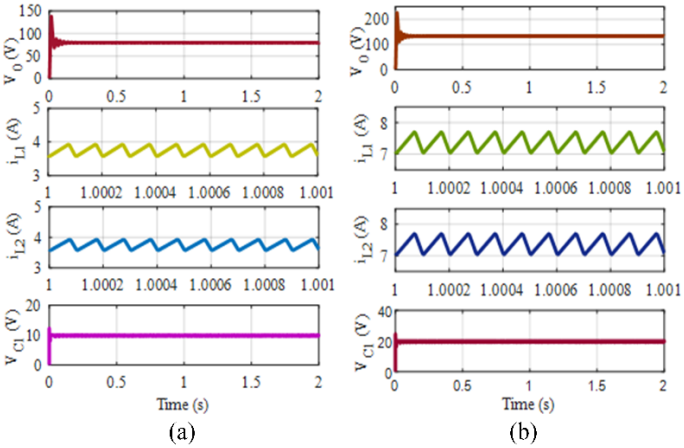


Fig. 11. Simulation result of output voltage (V_O), inductor currents (i_{L1} and i_{L2}), capacitor voltage (V_{C1}) in buck-boost mode in: (a) V_1 in out of work and (b) V_2 in out of work.

Additionally, the bidirectional capability of the converter is evaluated in buck mode, where the output (V_0=135 V) considers as the input, and source (V_2) acts as the load and it control with 20% duty ratio. The corresponding output voltage (V_{OB}), load current (I_{OB}) and inductor current (i_{L2B}) results are depicted in Fig. 9(d). Further verification is conducted at different input voltage settings (V_1 = 25 V, V_2 = 15 V) with duty cycles of (d_1 = 30%, d_2 = 30%, and d_3 = 10%) with results displayed in Fig. 10(a). Another test scenario with V_1 = 20 V, V_2 = 10 V, d_1 = 20%, d_2 = 20%, and d_3 = 10% is presented in Fig. 10(b). The results confirm alignment with theoretical values, demonstrating the converter's ability to operate under varying input voltages and duty cycles effectively. The proposed converter has also been verified under source failure conditions. The results in Fig. 11(a) show the case where V_1 is out of operation and V_2 is working, while the results for V_2 being out of operation and V1 is working is shown in Fig. 11(b). As seen in Fig. 11, even under failure conditions, the proposed converter continues to supply energy to the load.

B. Validation through Experimental

A 250 W laboratory prototype has been developed. Gate pulses are generated using a DSP (TMS320F28379D) controller board with an integrated DSP processor. These pulses are then amplified according to the required turn-on voltages for the IGBTs using gate driver circuits. The circuit specifications used for experimental validation are listed in Table I. The key components of the proposed converter include IGBT switches (GT30J121), with their anti-parallel diodes serving as switching diodes, gate driver circuits (TLP250), tapped inductors (L_1 and L_2) rated at 4 mH, and electrolytic capacitors ((C_1=360 µF/100V (EGPA101ELL361ML30S) and C=470 µF/350V (E92X351VSN471MR50T)). The converter is tested in buck-boost mode with input voltages specified in Table I, i.e. V_1=20 V, V_2=10 V, d_1=30%, d_2=30%, d_3=10%, f=10VkHz, and R=74 ohm. The corresponding results are presented in Fig. 12-17. Fig. 12 illustrates the waveform of the load voltage and inductor currents. The measured load voltage of 132.8 V closely aligns with theoretical calculations and simulation results. Additionally, Fig. 13-16 depict the voltage stress waveforms for the switches (S_1-S_3, S_5) and diodes (D_1-D_4) during buck-boost operation. The Fig. 13-16 illustrates the maximum voltage levels experienced by switches and diodes during operation, confirming that both components are subjected to voltage stresses within their safe operating limits. To regulate the output voltage under dynamic load variations, a closed-loop control system is implemented using a PID controller in real-time. The PID gains are manually tuned using the Ziegler–Nichols method, yielding final values of Kp=0.00481, Ki=1.527, and Kd=0.

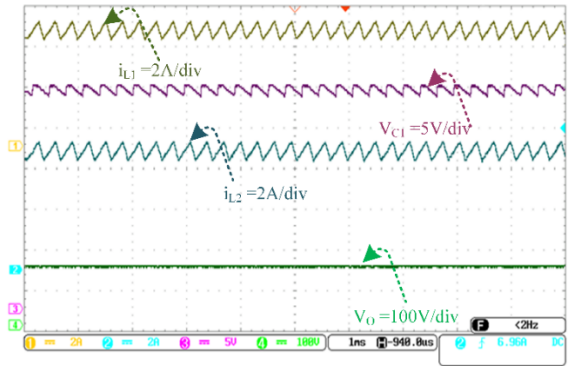


Fig. 12. Experimental waveforms of output voltage (V_O), inductor currents (i_{L1}, i_{L2}), and capacitor voltage (V_{C1}).

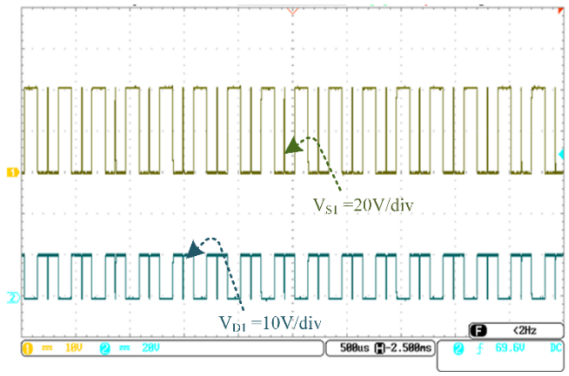


Fig. 13. Experimental voltage stress waveforms of switch (S_1) and diode (D_1).

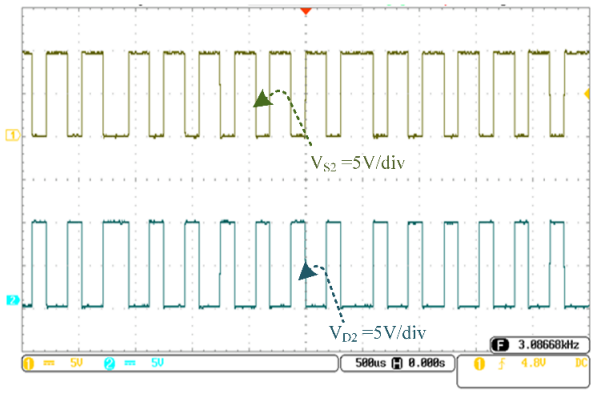


Fig. 14. Experimental voltage waveforms showing the stress across switch (S_2) and diode (D_2).

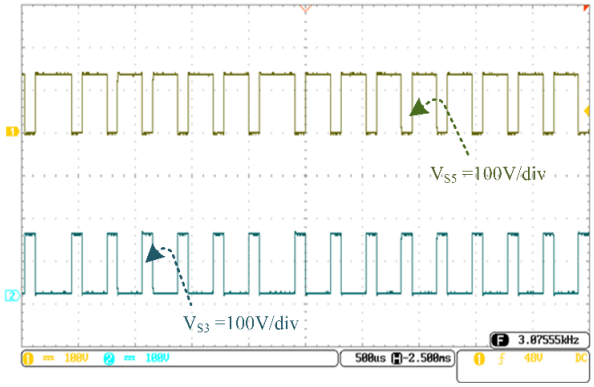


Fig. 15. Experimental voltage waveforms depicting the voltage stress across switches (S_3) and (S_5).

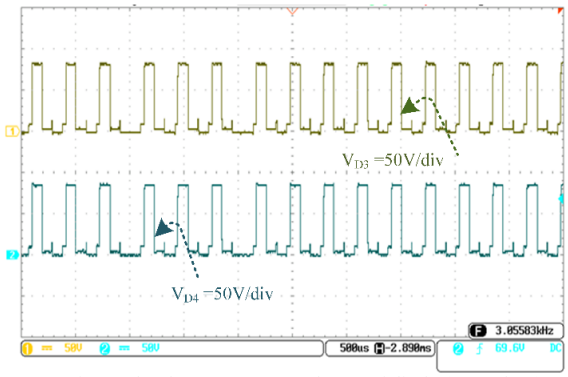


Fig. 16. Experimental voltage stress waveforms of diode (D_3 and D_4).

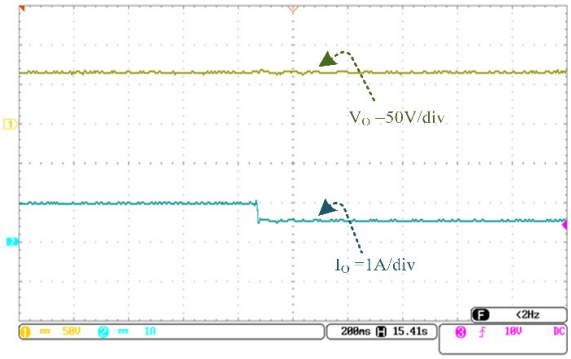
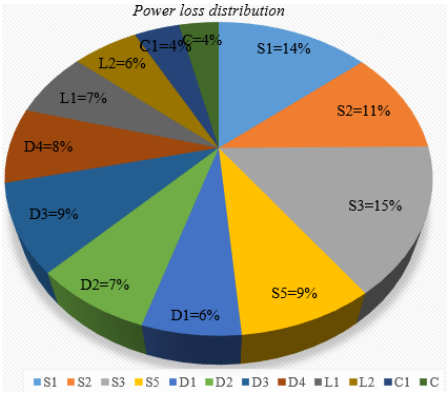
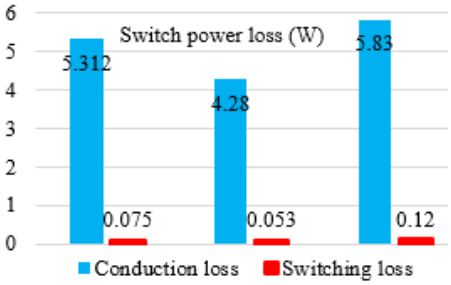


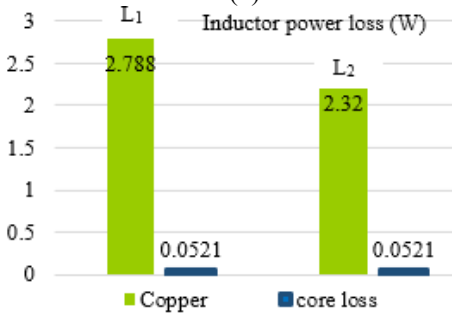
Fig. 17. Experimental transient response of the converter to a step change in load.



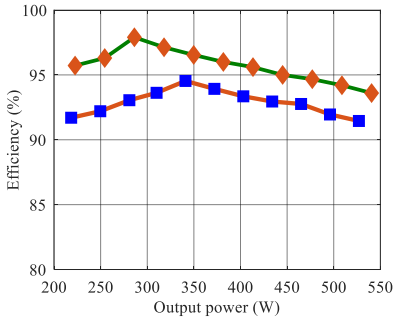
(a)



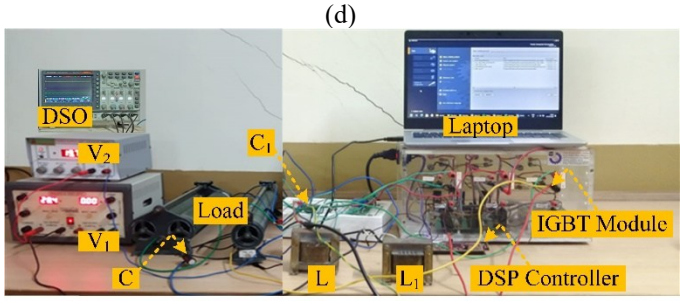
(b)



(c)



(d)



(e)

Fig. 18. (a) Power loss across each component, (b) Efficiency vs output power, (c) Switch power losses, (d) Inductor power losses and (e) Experimental photo in laboratory.

The proposed converter is evaluated under transient conditions, specifically during a sudden reduction in load. It maintains a stable output even when the load is abruptly reduced by 20% from its nominal value, as shown in Fig. 17. The power dissipation for different circuit components is illustrated in Fig. 18(a), while Fig. 18(b) and 18(c) display power losses in the switches and inductors, respectively. The efficiency of the converter is observed to be above 92.37% at rated power, as depicted in Fig. 18(d), while Fig. 18(e) presents the efficiency versus output power characteristics.

VI. CONCLUSION

This study presents a dual-input single-output converter with a switched-inductor network, designed to achieve high step-up voltage for DC microgrids and electric vehicle powertrains. The paper provides a detailed analysis of the circuit design, operational principles, and theoretical evaluation, along with a concise synthesis of the proposed topology. The design is scalable for ultra-high voltage gain and supports an N-input configuration, offering source fault tolerance and bidirectional operation. The converter's performance is verified in different mode of operation through MATLAB simulations, with the results closely matching the theoretical analysis. Additionally, experimental validation using a 250W laboratory prototype demonstrates the converter's ability to achieve enhanced output voltage with dual inputs, further confirming the theoretical findings.

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