Design and Analysis of an Improved Gain Single Inductor Dual Switch DC-DC Converter with Reduced Duty Ratio and Minimal Voltage Stress

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***Abstract*— This paper proposes an Improved Gain Single Inductor Dual Switch Converter (IGSIDSC) for the grid integration of solar and fuel cells, which achieves high voltage gain at reduced duty ratio and with less component count. The proposed converter is designed to operate with a duty ratio less than 50% to ensures reduced losses and less component stress. This salient feature makes the proposed converter unique among the other converters reported so far. By reducing voltage stress on switches and diodes, the design permits the use of lower-rated components and reduces the cost. The common ground configuration helps to reduce dv/dt issue. The IGSIDSC is analyzed in steady state with consideration of parasitic resistance for all components of the converter. Further, the simulation results are validated through experimental investigation using the prototype developed in laboratory for the power rating of 200 W. Also, the investigations on steady state performance and dynamic behavior of the experimental prototype effectively demonstrate the successful operation of the IGSIDSC.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9396

***Index Terms*— High-gain DC-DC converter, Non-isolated converters, Reduced voltage stress, Switched capacitor.**

I. Introduction

THE 2030 agenda adopted by United Nations has highlighted the need for affordable and clean energy (SDG-7) which mandates the reduction of fossil fuel usage and increases the demand for renewable energy sources, particularly in power sector [1]. This surge in demand can be satisfied by technologies such as PV and fuel cells. These sources typically generate DC power at lower voltage levels [2]-[4]. To integrate these renewable sources into the existing AC grid, a reliable power conditioning system is required which consists of both DC-DC converter and inverter stages. Therefore, a DC-DC converter with boost operation is must to integrate PV and fuel cell sources with the existing three-phase grid. For example, to achieve a three-phase grid voltage of 400 V at 50 Hz, the inverter DC-bus input voltage must be at least 600 V [5]-[8]. Conventional boost converters are having inadequate voltage gain and significant voltage stress, which reduce the efficiency at higher duty ratios values [9]-[10]. Hence, a boost converter with high gain at a lower duty ratio is necessary to overcome the above-mentioned drawbacks. Fig.1 shows the typical application of high gain DC-DC converter.

In this context, many literatures have reported different high gain DC-DC converter topologies [11]-[36], but each has their own demerits, such as more component count, common ground issue, and reduced efficiency. Moreover, due to high duty ratio, the converter switches and diodes will face high voltage and current stress, which affects the overall performance.

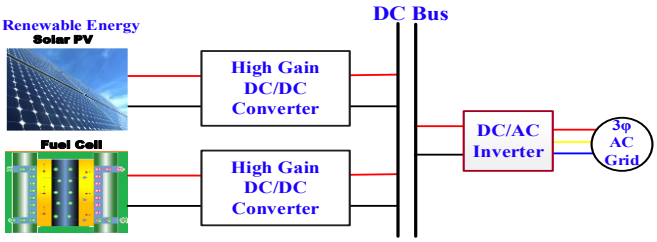

Fig. 1. Typical application diagram of high gain DC-DC converter.

Literature [11]-[16] described the converters which can produce 650 V from 48 V input at a higher duty ratio. In [11] an active switched-inductor and quasi-Z-source network-based converter is reported with 75.82% duty ratio. Similarly, [12] demonstrated a voltage multiplier cell-based converter with a 72.49% duty ratio, and [13] described an active switched-inductor and switched-capacitor based converter with a 68.11% duty ratio. The topologies reported in [11]-[13] utilised 14 components. Further, [14] and [15] combine a quadratic boost converter with a voltage-multiplier cell to achieve 650 V output, where the first one operates at a duty ratio of 67.4%, and utilized 16 components, and the next design achieves same output voltage at 64.73% duty ratio by using 20 components. In [16] uses a zeta-boost converter and an active quad switched inductor-based converter for a 63.32% duty ratio with 18 components. It is to be noticed from [11]-[16], that the required gain is attained only beyond 60% duty ratio. But, the high duty ratio operation of the above converters at high-frequency causes inductor core saturation and increased voltage stress.

Converters in references [17]–[28] achieve the same gain with a slightly lower duty ratio as the aforementioned literature. In [17], a hybrid high voltage gain converter is designed, and a voltage-multiplier cell-based converter is employed in [18], where both of them operate with a duty ratio of 58.74% and require 14 components. In [19], a quadratic boost converter with a switched-capacitor network is reported which operates at 57.7 % duty ratio. The converters reported in [20]-[22] operate with a duty ratio of 56.48%, with 16 components. A modified-voltage-multiplier-cell via a switched-inductor converter [23]

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operates with a 55.69% duty ratio using 16 components. By employing 14 components, converters in [24]-[26] have a duty ratio of 53.48%. Also, the literature [27] proposes a switched capacitor converter with a duty ratio of 52.21%, and [28] employs an extended capacitor-diode network-based converter with 51.31% duty ratio with 14 components. From the above literature, it can be realized that the higher gain is achieved when the duty ratio ranging between 50% to 60%, which leads to increased component stress.

Similarly, literature introduces converters with improved gain at lower duty ratios [29]–[36]. A quadratic boost converter operating with a duty ratio of 49.22% with 14 components is proposed in [29]. A converter with ultra-gain is presented in [30] operate with a 48.38% duty ratio using 16 components. The above-mentioned converters in [29]-[30] suffer with increased voltage stress. In [31], a hybrid-Z-source converter with 16 components operates at 43.12% duty cycle. It experiences voltage stress across its power devices exceeding 50% of the output voltage. In [32], a quasi-Z-source converter is employed, with a duty cycle of 42.61% and utilizes 16 components. It experiences voltage stress across its power switches of about 50% of the output voltage. In [33], a symmetrical switched capacitor Z-source converter is explained, and [34] reported a Z-network plus switched-capacitor converter. Both operate at a duty cycle of 42.03% with 14 components. The voltage stress on the switches in these converters is slightly below 50% of the output voltage. The Quasi-Z-Source converters are reported in [35] and [36] with 16 components and 14 components respectively. Both operate at 41% duty ratio and their power devices experience voltage stress of 0.41 times the output voltage.

It is clear from the Table I, that most of the high gain DC-DC Converters are facing the issue of high voltage stress across the switches. In addition to that the converters presented in literature [11]-[13],[15]-[18],[20]-[24],[28],[30]-[33],[35], and [36], do not have common ground, which leads to dv/dt problems and produces unreliable output. It is evident from the literature that higher gains are attained by making the converter to operate at a higher duty ratio, which increases device stress and core saturation. To address these issues, an IGSIDSC is presented in this work, which integrates the single inductor, dual switch-based structure [37]-[38] and the passive switched-capacitor network. The proposed structure achieves high gain with a minimal operating duty ratio which reduces the voltage stress on switches and diodes and eventually permits the use of lower-rated components. In particular, the single-inductor configuration, along with the reduced component count, helps to minimize the converter size and cost. The lower duty ratio operation avoids core saturation issues and enhances efficiency by minimizing conduction and switching losses. The common ground configuration reduces dv/dt issues, ensuring stable operation. These design advantages enable the proposed converter to overcome the limitations of conventional topologies. Further, to enhance the overall performance of the proposed converter, SiC devices are utilized for the prototype development. The paper is organized as follows: The IGSIDSC operation, along with mathematical derivations, is explained in section II. Performance evaluation, comparison review, small signal model, simulation and experimental validation, and conclusion are given in sections III, IV, V, and VI, respectively.

II. Description of the Proposed High Gain Converter

The proposed converter is depicted in Fig. 2, which has single inductor, two MOSFETs (S_1 & S_2), six diodes (D_1-D_6), and five capacitors (C_1-C_5). This IGSIDSC structure takes advantage of the utilization of reactive elements for energy recycling, resulting in improved voltage gain with a low duty ratio. Moreover, it offers advantages such as minimal voltage stress on the device and utilization of common ground. Both the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM), which are explained below, are used to examine the steady-state behavior of this converter.

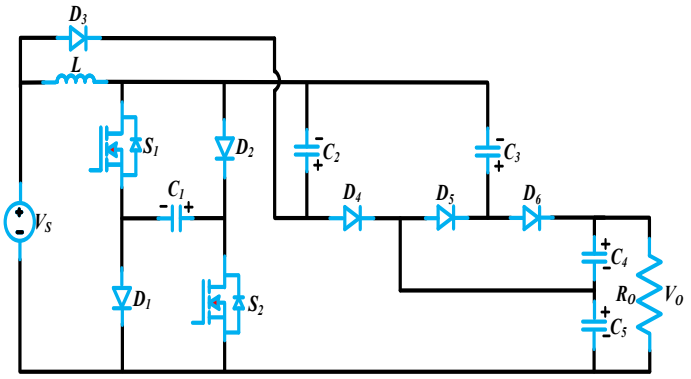


Fig. 2. Proposed topology of the improved gain single inductor dual switch converter (IGSIDSC).

A. CCM Operation

Based on the states of MOSFETs CCM in explained in two different operating states and then analytical waveform are discussed.

1) State – 1: During this state, MOSFETs S_1 and S_2 are activated, while diodes D_3 and D_5 are conducting, which is depicted in Fig. 3 as an equivalent circuit. The inductor receives energy from the input (V_s) and capacitor (V_{C1}) through the path V_S^+-L-S_1-C_1-S_2-V_S^-. Simultaneously, capacitor C_2 is charged from the input (V_s) and capacitor (V_{C1}) through the path V_S^+-D_3-C_2-S_1-C_1-S_2-V_S^-. The capacitor C_3 is charged from the capacitors (V_{C1}) and (V_{C5}) through the path C_5^+-D_5-C_3-S_1-C_1-S_2- C_5^-. The capacitors C_4 and C_5 supply the load through the path C_4^+-R_O-C_5-C_4^-. The remaining diodes are OFF during this state. Due to the energization of inductor, the inductor voltage is positive, and the inductor current increases, as depicted in Fig. 5 (a). The following equations represent the voltage and current for this state.

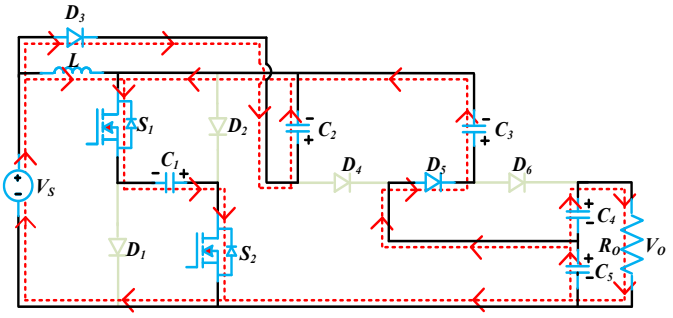


Fig. 3. Equivalent circuit of state 1 operation for the IGSIDSC.

TABLE I
SUMMARIZED LITERATURE SURVEY

Reference No.	Converter Type	DR (%) @ 650 V	N_T	Key Issues
[11]	Active switched-inductor and quasi-Z-source	75.82		
[12]	Voltage multiplier cell-based	72.49	14	High duty ratio, increased voltage stress, no common ground, and core saturation.
[13]	Active switched-inductor and switched-capacitor	68.11		
[14]	Quadratic boost with voltage multiplier	67.40	16	High duty ratio, increased component count, high voltage stress, and core saturation.
[15]	Quadratic boost with voltage multiplier	64.73	20	High duty ratio, increased voltage stress, increased component count, no common ground, and core saturation.
[16]	Zeta-boost with active quad switched-inductor	63.32	18	High duty ratio, increased voltage stress, increased component count, no common ground, and core saturation.
[17]-[18]	Hybrid topology, voltage multiplier	58.74	14	Moderate duty ratio, high voltage stress, and no common ground.
[19]	Boost converter with a Luo and voltage doubler	57.7	16	Moderate duty ratio, high voltage stress, and increased component count.
[20]-[22]	Various (quadratic boost, voltage multiplier)	56.48	16	Moderate duty ratio, high voltage stress, increased component count, and no common ground.
[23]	A modified voltage multiplier cell with switched inductor	55.69	16	
[24]	Quadratic boost converter	53.48	14	Moderate duty ratio, high voltage stress, and no common ground.
[25]-[26]	Quadratic boost converter			Moderate duty ratio, and high voltage stress.
[27]	Switched capacitor	52.21	14	Moderate duty ratio, and high voltage stress.
[28]	Extended capacitor-diode network	51.31	14	Moderate duty ratio, and no common ground.
[29]	Quadratic boost	49.22	14	Moderate duty ratio, and high voltage stress.
[30]	Ultra-gain converter	48.38	16	Moderate duty ratio, more component count, and no common ground.
[31]	Hybrid-Z-source	43.12	16	Voltage stress across power devices exceeds 50% of the output voltage, increased component count and a lack of common ground.
[32]	Quasi-Z-source	42.61	16	Switch voltage stress is 50% of the output voltage, diode voltage stress is equal to the output voltage, increased component count and no common ground.
[33]	Symmetrical switched capacitor Z-network	42.03	14	Voltage stress is slightly below half of the output voltage, and no common ground.
[34]	Z-network plus switched capacitor			Voltage stress is slightly below half of the output voltage.
[35]	Quasi-Z-source	41	16	Voltage stress is 41% of output voltage, no common ground, and increased component count.
[36]	Quasi-Z-source		14	Voltage stress is 41% of output voltage, and no common ground.

DR – Duty Ratio, N_T-Total Number of Components

$$V_L = V_S + V_{C1};\ V_L = V_{C2};\ V_L = V_S + V_{C3} - V_{C5};$$
$$i_{C1} = i_{S1} = i_{S2} = i_S + i_{D5} = i_L + i_{D3} + i_{D5};\ i_{C2} = i_{D3}; \quad (1)$$
$$i_{C3} = i_{D5};\ i_{C4} = i_o;\ i_{C5} = i_{D5} + i_o$$

2) State – 2: During this state, the two MOSFETs are deactivated, and diodes D_1, D_2, D_4, and D_6 are conducting, as depicted in Fig. 4 as an equivalent circuit. The capacitor C_1 is charged by the input (V_s) and inductor, along the path V_S^+-L-D_2-C_1-D_1-V_S^-. Simultaneously, the capacitor C_5 is charged from the input (V_s), inductor, and capacitor (V_{C2}) following the path V_S^+-L-C_2-D_4-C_5-V_S^-. The capacitors C_4 and C_5 are charged and load supplied from the input (V_s), inductor, and capacitor (V_{C3}) through the paths V_S^+-L-C_3-D_6-C_4-C_5-V_S^- and V_S^+-L-C_3-D_6-R_O-V_S^-. The remaining diodes are OFF during this state. Due to the de-energization of inductor, the inductor voltage is negative, and the inductor current decreases, as depicted in Fig. 5 (a). The following equations represent the voltage and current for this state.

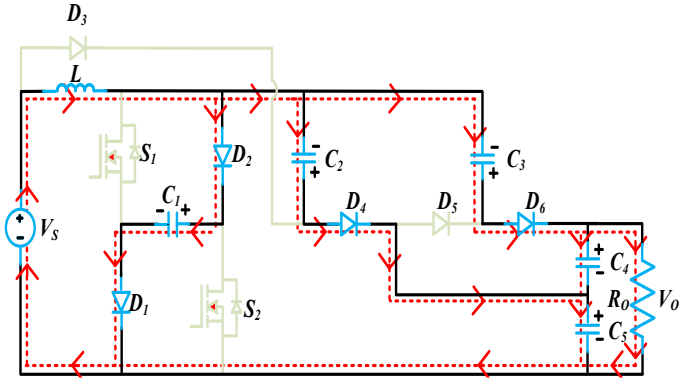


Fig. 4. Equivalent circuit of state 2 operation for the IGSIDSC.

$$V_L = V_{C1} - V_S;\ V_L = V_{C5} - V_{C2} - V_S;$$
$$V_L = V_O - V_{C3} - V_S;\ V_L = V_{C4} + V_{C5} - V_{C3} - V_S \quad (2)$$
$$i_{C1} = i_{D1} = i_{D2};\ i_{C2} = i_{D4};\ i_{C3} = i_{D6};$$
$$i_{C4} = i_{D6} - i_o;\ i_{C5} = i_{D4} + i_{D6} - i_o$$

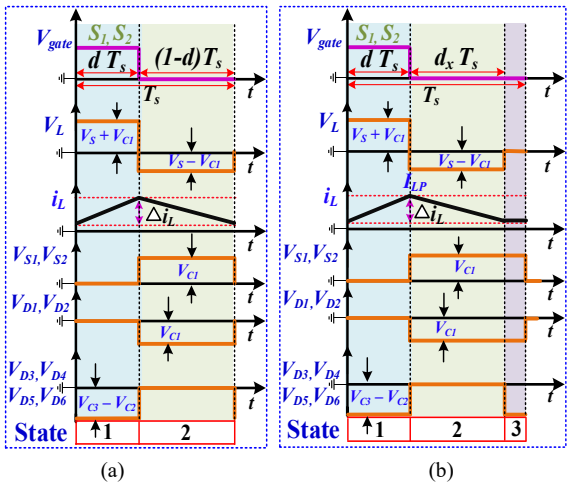


Fig. 5. Analytical waveforms of the IGSIDSC converter in (a) CCM and (b) DCM, showing gate pulse, inductor voltage, inductor current, switch voltage stress, and diode voltage stress.

The voltages of five capacitors and the voltage gain (M_V) of the IGSIDSC are calculated using (1) and (2), presented below.

$$V_{C1} = \frac{V_S}{1-2d};\ V_{C2} = \frac{2V_S(1-d)}{1-2d};\ V_{C3} = \frac{2V_S(d^2-3d+2)}{2d^2-3d+1};$$
$$V_{C4} = \frac{2V_S}{1-2d};\ V_{C5} = \frac{V_S(2d^2-5d+3)}{2d^2-3d+1} \quad (3)$$

$$M_V = \frac{V_o}{V_S} = \frac{2d^2-7d+5}{2d^2-3d+1} \quad (4)$$

It is inferred from (3)-(4) that, the operational duty ratio of the IGSIDSC ranges from $0 < d < 0.5$. The duty ratio of the IGSIDSC is determined with (4) and symbolized by (5).

$$d = \left(\frac{(3M_V - 7) - \sqrt{M_V^2 + 6M_V + 9}}{4(M_V - 1)} \right) \quad (5)$$

B. DCM Operation

Based on the inductor current, DCM is explained in three different operating states. The first two state operations are similar to CCM, and then analytical waveforms are discussed.

1) State – 1: The peak current I_{LP1} of an inductor is expressed as given in (6).

$$I_{Lp1} = \frac{V_S + V_{C1}}{L} d\,T_s \quad (6)$$

2) State – 2: The peak current I_{LP2} of an inductor is expressed as in (7).

$$I_{Lp2} = \frac{V_S - V_{C1}}{L} d_x\,T_s \quad (7)$$

3) State – 3: In this state, the inductors hold zero current at the end of $d_x T_S$ and is shown in Fig. 5(b). Fig. 6 illustrates the equivalent circuit of the state 3 operation. By employing (6) and (7), the expression for d_x is obtained as follows,

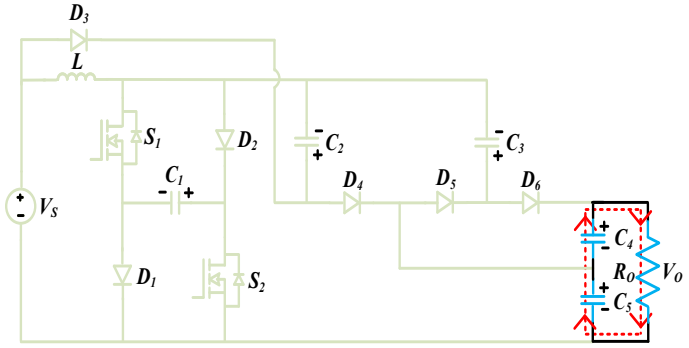


Fig. 6. Equivalent circuit of state 3 operation for the IGSIDSC.

$$d_x = \frac{(V_S + V_{C1})\,d}{V_{C1} - V_S} \quad (8)$$

Where d_x – Discharging duty cycle.

From Fig. 5(b), the average inductor current I_{LA} is expressed as in (9).

$$I_{LA} = \frac{V_S(1-d)\,d\,T_s}{(1-2d)\,L} \quad (9)$$

The voltage gain of the IGSIDSC in DCM, by using power balance principle, M_{DCM} is obtained as in (10).

$$M_{DCM} = \frac{V_o}{V_S} = 0.5 + 0.5\sqrt{1 + \frac{4(1-d)\,d}{(1-2d)\,\tau_L}} \quad (10)$$

The inductor time constant $\tau_L = Lf_s/R_o$. Here, f_s is the switching frequency and R_o is the load resistance. The inductor current is neither discontinuous nor continuous during the boundary condition mode (BCM) of operation. By considering the gain of IGSIDSC during CCM and DCM as equal at BCM, the time constant of inductor τ_{BL} at BCM is given as,

$$\tau_{BL} = \frac{0.25(1-d)^3(1-2d)d}{5-12d+9d^2-2d^3} \tag{11}$$

Fig. 7 depicts the CCM and DCM boundary condition of the IGSIDSC based on the duty ratio. It is evident that when τ_L exceeds τ_{BL}, the IGSIDSC operates in CCM.

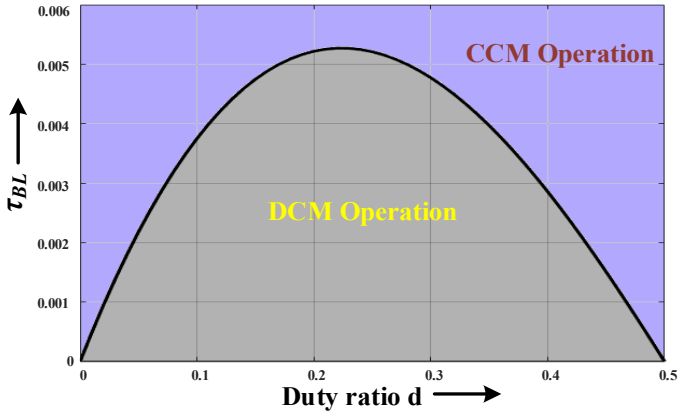


Fig. 7. Inductor time constant versus duty ratio for the CCM and DCM boundary condition in the IGSIDSC converter.

C. Selections of Inductor and Capacitors

The expression for inductor L is derived from state 1:

$$L \geq \frac{2V_o\, d\,(1-d)^2}{(2d^2-7d+5)*f_s*\Delta i_{Lr}} \tag{12}$$

The inductance value can be calculated using parameters like duty ratio (d), output voltage (V_o), switching frequency (f_S), and inductor current ripple (Δi_{Lr}). Accordingly, an appropriate inductor can be selected through (12).

The capacitor values for C_1, C_2, C_3, C_4, and C_5 are determined through state 1, wherein ΔV_{Cr1}, ΔV_{Cr2}, ΔV_{Cr3}, ΔV_{Cr4}, and ΔV_{Cr5} represent the ripple voltages across the capacitors.

$$\begin{aligned} C_1 &\geq \frac{V_o(2d^3-5d^2+2d+1)}{(2d^2-3d+1)*f_s*\Delta v_{Cr1}*R_O} \\ C_2 &\geq \frac{V_o}{f_s*\Delta v_{Cr2}*R_O}; C_3 \geq \frac{V_0}{f_s*\Delta v_{Cr3}*R_O} \\ C_4 &\geq \frac{V_o\, d}{f_s*\Delta v_{Cr4}*R_O}; C_5 \geq \frac{V_o(1+d)}{f_s*\Delta v_{Cr5}*R_O} \end{aligned} \tag{13}$$

The capacitance value is dependent on factors such as duty ratio (d), output voltage (V_o), switching frequency (f_S), output resistance (R_O), and capacitor voltage ripple (Δv_{cr}). Therefore, (13) can be utilized to calculate the suitable values for C_1, C_2, C_3, C_4, and C_5.

III. Performance Evaluation

This section delves into the stress analysis and performance evaluation of the IGSIDSC, by taking the parasitic resistance into account.

A. Stress Analysis

The voltage stress on the MOSFETs and diodes in the deactivated condition can be determined as follows:

$$V_{S1}, V_{S2}, V_{D1}, V_{D2} = \frac{V_S}{1-2d}; V_{D3}, V_{D4}, V_{D5}, V_{D6} = \frac{2V_S}{1-2d} \tag{14}$$

The converter source current is determined using the power balancing principle, and the resulting current is denoted as I_S, which is described as follows:

$$I_S = \frac{2d^2-7d+5}{2d^2-3d+1} I_o \tag{15}$$

The inductor current I_L, switch current stress, and diode current stress can be determined based on (1), (2), and (15) and it is given as follows:

$$\begin{aligned} I_L &= \frac{(2d^3-9d^2+8d-1)}{(2d^2-3d+1)d} I_o; I_{S1P} = I_{S2P} = \frac{(2d^3-5d^2+2d+1)}{(2d^2-3d+1)d} I_o \\ I_{D1P} &= I_{D2P} = \frac{(2d^3-5d^2+2d+1)}{-2d^3+5d^2-4d+1} I_o \\ I_{D3P} &= I_{D5P} = \frac{1}{d} I_o; I_{D4P} = I_{D6P} = \frac{1}{1-d} I_o \end{aligned} \tag{16}$$

Based on the abovementioned analysis, the average current of the MOSFETs and diodes are determined as follows.

$$\begin{aligned} I_{S1A} &= I_{S2A} = I_{D1A} = I_{D2A} = \frac{2d^3-5d^2+2d+1}{2d^2-3d+1} I_o \\ I_{D3A} &= I_{D4A} = I_{D5A} = I_{D6A} = I_o \end{aligned} \tag{17}$$

Furthermore, the RMS currents of the MOSFETs and diodes are computed as follows:

$$\begin{aligned} I_{S1R} &= I_{S2R} = \frac{(2d^3-5d^2+2d+1)}{(2d^2-3d+1)\sqrt{d}} I_o \\ I_{D1R} &= I_{D2R} = \frac{(2d^3-5d^2+2d+1)}{(2d^2-3d+1)(1-d)^{0.5}} I_o \\ I_{D3R} &= I_{D5R} = \frac{1}{\sqrt{d}} I_o; I_{D4R} = I_{D6R} = \frac{1}{\sqrt{1-d}} I_o \end{aligned} \tag{18}$$

The rms current of the capacitors are as follows:

$$\begin{aligned} I_{C1R} &= \frac{(2d^3-5d^2+2d+1)}{(2d^2-3d+1)(1-d)^{0.5}\sqrt{d}} I_o; I_{C5R} = \frac{1+d}{\sqrt{d(1-d)}} I_o \\ I_{C2R} &= I_{C3R} = \frac{1}{\sqrt{d(1-d)}} I_o; I_{C4R} = \sqrt{\frac{d}{1-d}} I_o \end{aligned} \tag{19}$$

B. Performance Analysis with Parasitic Resistance

This investigation aims to discuss the impact of parasitic resistance of IGSIDSC components on voltage gain and efficiency. Fig. 8 illustrates circuit diagram of the IGSIDSC converter with parasitic elements. For this investigation, an inductor (L) with a winding resistance (R_L) of 15 mΩ is

considered. The parasitic resistances of capacitors C_1-C_5 are labeled (R_C) and have a value of 10 mΩ each. The parasitic resistance (R_S) of MOSFETs is specified as 55 mΩ, and the on/off switching time is 75 ns. Additionally, the internal resistance and forward voltage drop of the diodes are specified as R_d = 50 mΩ and V_{FD} = 0.79 V, respectively. In real-world high-power applications, parasitic resistances lead to increased I^2R losses, affecting efficiency and thermal management. To effectively mitigate these effects, it is essential to select components with low parasitic resistance and to implement efficient cooling solutions to handle higher power levels.

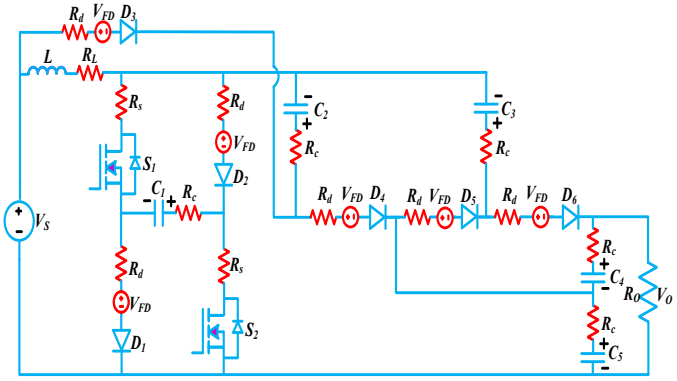


Fig. 8. Circuit diagram of the IGSIDSC converter with parasitic elements.

The voltage gain of the IGSIDSC with parasitic elements is obtained as,

$$\frac{V_0}{V_S}=\frac{(2d^2-7d+5)-\frac{V_{FD}}{V_S}E_4}{(1-3d+2d^2)+\frac{R_L}{R_O}E_1+\frac{R_C}{R_O}E_2+\frac{R_d}{R_O}E_3+\frac{R_S}{R_O}E_5} \tag{20}$$

Where $E_1=4(2d^3-9d^2+8d-1)/(1-2d)d$;

$E_2=(-4d^4+9d^2-10d+5)/(2d^2-3d+1)d$;

$E_3=2(4d^4-14d^3+12d^2-3d+1)/(2d^2-3d+1)d$;

$E_4=8(d^2-2d+1)$ and

$E_5=4(-2d^4+7d^3-7d^2+d+1)/(2d^2-3d+1)d$

Utilizing (4) and (20), the theoretical voltage gains are plotted for various load conditions in Fig.9. along with the experimental voltage gain. The plot proves that at high load conditions, particularly when the duty ratio exceeds 0.4, the outcome of parasitic elements on the voltage gain becomes notably significant. Conversely, when the duty ratio falls below 0.4, the parasitic element effect is reduced.

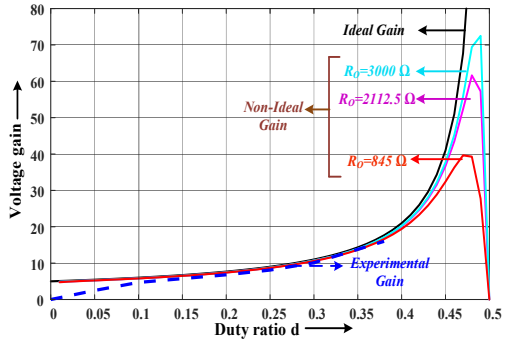


Fig. 9. Ideal, non-ideal, and experimental voltage gain versus duty ratio of the IGSIDSC converter.

The voltage gain of the laboratory prototype is observed by varying duty ratio up to 0.38, The gain obtained from the experimental prototype closely matches the theoretical gain, confirming the validity of the proposed converter topology.

To determine the efficiency of the converter, the losses for each component are given as follows:

For the IGSIDSC, the total switch losses encompass both conduction and switching losses are computed as:

$$P_{S,CL}=\frac{2I_0^2(4d^6-20d^5+33d^4-16d^3-6d^2+4d+1)}{4d^5-12d^4+13d^3-6d^2+d}R_s$$
$$P_{S,SL}=\frac{V_S I_o f_s (t_{on}+t_{off})(2d^3-5d^2+2d+1)}{-4d^3+8d^2-5d+1} \tag{21}$$

where t_{on} is equal to rise time and turn-on delay time, and t_{off} is equal to fall time and turn-off delay time.

The total diode losses encompass both conduction and forward voltage drop losses:

$$P_{D,CL}=\frac{2I_0^2(4d^7-20d^6+33d^5-12d^4-18d^3+17d^2-5d+1)}{-4d^6+16d^5-25d^4+19d^3-7d^2+d}R_d$$
$$P_{D,V_{FD}L}=\frac{2I_0(2d^3-d^2-4d+3)}{2d^2-3d+1}V_{FD} \tag{22}$$

The loss of an inductor is calculated as follows:

$$P_{LL}=\frac{I_0^2(2d^3-9d^2+8d-1)^2}{4d^6-12d^5+13d^4-6d^3+d^2}R_L \tag{23}$$

Also, the capacitor loss is calculated as follows:

$$P_{CL}=\frac{I_0^2(12d^6-36d^5+47d^4-38d^3+23d^2-12d+4)}{-4d^6+16d^5-25d^4+19d^3-7d^2+d}R_C \tag{24}$$

From the losses of each component calculated using (21) to (24), the efficiency of the IGSIDSC can be computed as follows:

$$\eta=\frac{P_0}{P_0+P_{S,CL}+P_{S,SL}+P_{D,CL}+P_{D,V_{FD}L}+P_{LL}+P_{CL}}\times 100 \tag{25}$$

The analysis in Fig. 10 represents the loss distribution profile of the IGSIDSC calculated using (21–25) for a 200 W output power with 48 V input, 650 V output, and 50 kHz switching frequency.

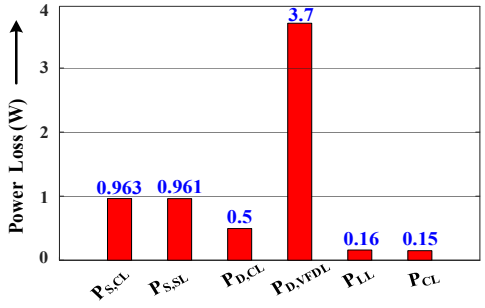


Fig. 10. Power loss distribution across various elements.

It indicates that the majority of losses occurs due to the diode forward voltage drop, which is approximately 57.51% of the total losses. Since, operating duty ratio of the converter is minimum, the conduction losses of the MOSFET and diode remain low. Hence, the IGSIDSC analytical efficiency is 96.88% at 200 W.

IV. Comparison Review

In this section, the comparison analysis of IGSIDSC with existing converters based on the component count, voltage gain, duty ratio, maximum voltage stress, common ground, and efficiency is carried out and it is presented in Table II. The relation between voltage gain and duty ratio plot is depicted in Fig. 11 (a), which shows that the IGSIDSC achieves the highest voltage gain for all ranges of duty ratio (< 0.5) among existing converters.

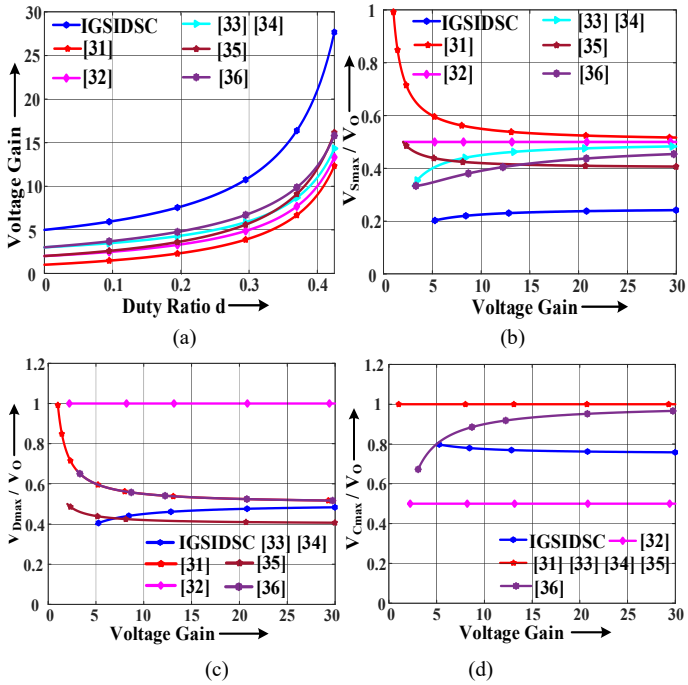


Fig. 11. Comparison review of the IGSIDSC and existing converter (a) Voltage gain versus duty ratio (b) Maximum switch voltage stress (V_{Smax}/V_O) versus voltage gain (c) Maximum diode voltage stress (V_{Dmax}/V_O) versus voltage gain (d) Maximum capacitor voltage stress (V_{Cmax}/V_O) versus voltage gain.

From the Table II, it can be seen that for the gain of 13.54, the IGSIDSC operates at duty ratio of 34.06%. It is to be noted that the MOSFETs and two diodes are having voltage stress as approximately 23% of the output voltage. Also, the four diodes have voltage stress as approximately 46.3% of the output voltage, and the maximum voltage stress on the capacitor is less than the output voltage.

According to the analysis, the IGSIDSC has a minimum operational duty ratio, which eventually decreases the voltage stress on switches and diodes and hence it permits the use of lower-rated components. Additionally, using a single inductor, the IGSIDSC size is smaller, resulting in reduced costs and achieving high efficiency.

V. Small Signal Model

This section presents the development of the small-signal model for the IGSIDSC using the state-space averaging method. The state-space model of the converter has been developed as denoted in (26). In this context, the state variable x represents the inductor current (i_L) and capacitor voltage (v_{C1} - v_{C5}). The input variable u is the source voltage (V_S), and the output variable y is the output voltage (V_o). The matrix A_j, B_j, and C_j represents the system, input, and output matrices, respectively. In order to avoid invalid states, the component equivalent series resistance is assumed by the loop resistance "r" and is included in the analysis. The duty ratio d is considered as the control variable to perform the closed loop operation.

$$\dot{x}(t) = A_j x(t) + B_j u(t);\ y(t) = C_j x(t) \tag{26}$$

The state-space model specified in (27) represents state 1, where the MOSFETs S_1 and S_2 are activated, while in state 2, the MOSFETs S_1 and S_2 are deactivated and it is represented as (28). The average state-space model of the IGSIDSC, which results from the combination of states 1 and 2, as shown in (29).

TABLE II
Comparison Review Of IGSIDSC and Existing Converter

Topology	[31]	[32]	[33]	[34]	[35]	[36]	IGSIDSC
N_S/ N_D/ N_C/ N_L /N_T	1/4/7/4/16	2/4/6/4/16	1/4/6/3/14	1/5/6/2/14	1/5/7/3/16	2/4/5/3/14	2/6/5/1/14
Voltage Gain V_O/V_s	$\frac{1+2d}{1-2d}$	$\frac{2}{1-2d}$	$\frac{3-2d}{1-2d}$	$\frac{3-2d}{1-2d}$	$\frac{2+d}{1-2d}$	$\frac{3-3d-2d^2}{1-3d+2d^2}$	$\frac{2d^2-7d+5}{2d^2-3d+1}$
Maximum Voltage Stress on Switch V_{Smax}/V_O	$\frac{1}{1+2d}$	$\frac{1}{2}$	$\frac{1}{3-2d}$	$\frac{1}{3-2d}$	$\frac{1}{2+d}$	$\frac{1-d}{3-3d-2d^2}$	$\frac{1-d}{2d^2-7d+5}$
Maximum Voltage Stress on Diode V_{Dmax}/V_O	$\frac{1}{1+2d}$	1	$\frac{1}{3-2d}$	$\frac{1}{3-2d}$	$\frac{1}{2+d}$	$\frac{2-3d}{3-3d-2d^2}$	$\frac{2(1-d)}{2d^2-7d+5}$
Maximum Voltage Stress on Capacitor V_{Cmax}/V_O	1	$\frac{1}{2}$	1	1	1	$\frac{2-4d^2}{3-3d-2d^2}$	$\frac{2d^2-6d+4}{2d^2-7d+5}$
Common Ground	No	No	No	Yes	No	No	Yes
DR (%) @ 650 V	43.12	42.61	42.03	42.03	41.1	41.03	34.06
Analytical ɳ (%)	95.43%	93.36%	96.12%	92.8%	90.4%	94.62%	96.88%
Output Power V_s/V_O	200 W 48/650 V	200 W 48/650 V	200 W 48/650 V	200 W 48/650 V	200 W 24/360 V	200 W 48/650 V	200 W 48/650 V

N_S-Number of Switches, N_D-Number of Diodes, N_C-Number of Capacitors, N_L-Number of Inductors, N_T-Total Number of Components, DR-Duty Ratio

$$\dot{x}(t) = A_1\, x(t) + B_1\, u(t);\; y(t) = C_1\, x(t) \tag{27}$$

$$A_1 = \begin{bmatrix} 0 & \frac{1}{L} & 0 & 0 & 0 & 0 \\ -\frac{1}{C_1} & -\frac{2}{C_1 r} & \frac{1}{C_1 r} & \frac{1}{C_1 r} & 0 & -\frac{1}{C_1 r} \\ 0 & \frac{1}{C_2 r} & -\frac{1}{C_2 r} & 0 & 0 & 0 \\ 0 & \frac{1}{C_3 r} & 0 & -\frac{1}{C_3 r} & 0 & \frac{1}{C_3 r} \\ 0 & 0 & 0 & 0 & -\frac{1}{C_4 R} & -\frac{1}{C_4 R} \\ 0 & -\frac{1}{C_5 r} & 0 & \frac{1}{C_5 r} & -\frac{1}{C_5 R} & -\frac{(R+r)}{C_5 r R} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{C_1 r} & \frac{1}{C_2 r} & 0 & 0 & 0 \end{bmatrix}^T \quad C_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

$$\dot{x}(t) = A_2\, x(t) + B_2\, u(t);\; y(t) = C_2\, x(t) \tag{28}$$

$$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} & 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & -\frac{2}{C_1 r} & -\frac{1}{C_1 r} & -\frac{1}{C_1 r} & \frac{1}{C_1 r} & \frac{2}{C_1 r} \\ 0 & -\frac{1}{C_2 r} & -\frac{1}{C_2 r} & 0 & 0 & \frac{1}{C_2 r} \\ 0 & -\frac{1}{C_3 r} & 0 & -\frac{1}{C_3 r} & \frac{1}{C_3 r} & \frac{1}{C_3 r} \\ 0 & \frac{1}{C_4 r} & 0 & \frac{1}{C_4 r} & -\frac{(R+r)}{C_4 r R} & -\frac{(R+r)}{C_4 r R} \\ 0 & \frac{2}{C_5 r} & \frac{1}{C_5 r} & \frac{1}{C_5 r} & -\frac{(R+r)}{C_5 r R} & -\frac{(2R+r)}{C_5 r R} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad C_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

$$\dot{x}(t) = A_{av}\, x(t) + B_{av}\, u(t);\; y(t) = C_{av}\, x(t) \tag{29}$$

$$A_{av} = \begin{bmatrix} 0 & \frac{2d-1}{L} & 0 & 0 & 0 & 0 \\ \frac{1-2d}{C_1} & -\frac{2}{C_1 r} & \frac{2d-1}{C_1 r} & \frac{2d-1}{C_1 r} & \frac{1-d}{C_1 r} & \frac{2-3d}{C_1 r} \\ 0 & \frac{2d-1}{C_2 r} & -\frac{1}{C_2 r} & 0 & 0 & \frac{1-d}{C_2 r} \\ 0 & \frac{2d-1}{C_3 r} & 0 & -\frac{1}{C_3 r} & \frac{1-d}{C_3 r} & \frac{1}{C_3 r} \\ 0 & \frac{1-d}{C_4 r} & 0 & \frac{1-d}{C_4 r} & \frac{R(d-1)-r}{C_4 r R} & \frac{R(d-1)-r}{C_4 r R} \\ 0 & \frac{2-3d}{C_5 r} & \frac{1-d}{C_5 r} & \frac{1}{C_5 r} & \frac{R(d-1)-r}{C_5 r R} & \frac{R(d-2)-r}{C_5 r R} \end{bmatrix}$$

$$B_{av} = \begin{bmatrix} \frac{1}{L} & -\frac{d}{C_1 r} & \frac{d}{C_2 r} & 0 & 0 & 0 \end{bmatrix}^T \quad C_{av} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

As given in (29), the state variables, input variable, output variable, and control variable are expressed in terms of small signal disturbances as follows:

$$i_L = I_L + \hat{i}_L; v_{C1} = V_{C1} + \hat{v}_{C1}; v_{C2} = V_{C2} + \hat{v}_{C2}; v_{C3} = V_{C3} + \hat{v}_{C3};$$
$$v_{C4} = V_{C4} + \hat{v}_{C4}; v_{C5} = V_{C5} + \hat{v}_{C5}; v_S = V_S + \hat{v}_s; v_o = V_o + \hat{v}_o;$$

and $d = D + \hat{d}$. The resulting small-signal model is derived in (30). The transfer functions, output to input voltage $(\hat{v}_0/\hat{v}_S)$, and output voltage to control variable ($\hat{v}_0/\hat{d}$) are given in (31) and (32), respectively.

The transfer function of the proposed converter is validated through the procedure explained in [39]. In order to validate the transfer function described in (32), the bode plot of transfer function is compared against the bode plot of circuit simulation as shown in Fig. 12. From the bode plot, the gain margin is observed as -72.17 dB, and the phase margin is observed as -87.28° for the derived transfer function ($\hat{v}_0/\hat{d}$). Similarly, the circuit simulation results in a gain margin of -73.2 dB and a phase margin of -89.93°. The closeness of these margin values validates the derived transfer function.

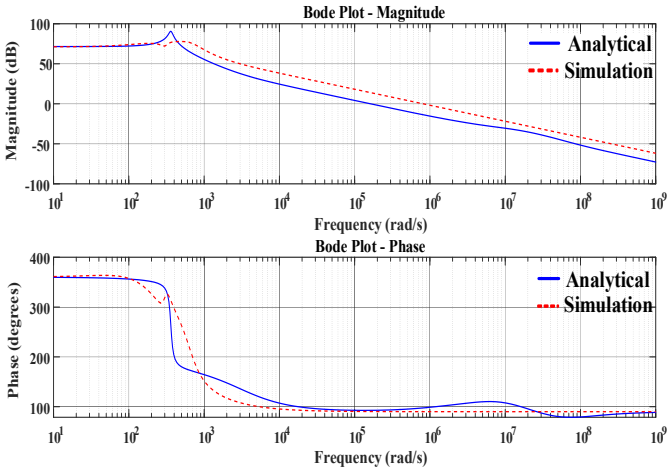


Fig. 12. Transfer Function validation using bode plot.

To further improve the dynamic performance of the proposed system, a PI controller is designed based on the derived small-signal model. The Fig. 13 shows the closed loop control system of the IGSIDSC with PI controller. The actual output voltage (V_{oact}) is compared with the desired output voltage (V_{oref}) to produce the error signal 'e'. This error signal is given to the PI controller to produce the desired duty ratio for the IGSIDSC. The tuned values of the proportional gain (K_p) and integral gain (K_i) are found to be $1.6*10^{-6}$ and 0.65, respectively.

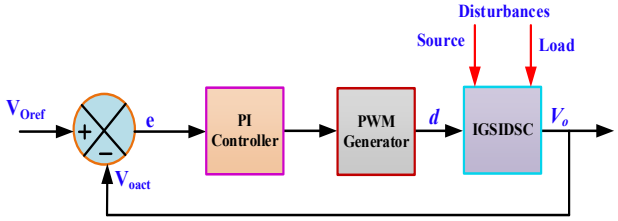


Fig. 13. Closed loop control strategy of the IGSIDSC converter with a PI controller.

The gains of PI controller are calculated through the Ziegler–Nichols method [40]. These parameter values are crucial in governing the converter behavior, ensuring that the system attains the regulated output value.

$$
\begin{cases}
\begin{bmatrix} \dot{\hat{i}}_L \\ \dot{\hat{v}}_{C1} \\ \dot{\hat{v}}_{C2} \\ \dot{\hat{v}}_{C3} \\ \dot{\hat{v}}_{C4} \\ \dot{\hat{v}}_{C5} \end{bmatrix} = \begin{bmatrix} 0 & \frac{2d-1}{L} & 0 & 0 & 0 & 0 \\ \frac{1-2d}{C_1} & -\frac{2}{C_1 r} & \frac{2d-1}{C_1 r} & \frac{2d-1}{C_1 r} & \frac{1-d}{C_1 r} & \frac{2-3d}{C_1 r} \\ 0 & \frac{2d-1}{C_2 r} & -\frac{1}{C_2 r} & 0 & 0 & \frac{1-d}{C_2 r} \\ 0 & \frac{2d-1}{C_3 r} & 0 & -\frac{1}{C_3 r} & \frac{1-d}{C_3 r} & \frac{1}{C_3 r} \\ 0 & \frac{1-d}{C_4 r} & 0 & \frac{1-d}{C_4 r} & \frac{R(d-1)-r}{C_4 r R} & \frac{R(d-1)-r}{C_4 r R} \\ 0 & \frac{2-3d}{C_5 r} & \frac{1-d}{C_5 r} & \frac{1}{C_5 r} & \frac{R(d-1)-r}{C_5 r R} & \frac{R(d-2)-r}{C_5 r R} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{C3} \\ \hat{v}_{C4} \\ \hat{v}_{C5} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ -\frac{d}{C_1 r} \\ \frac{d}{C_2 r} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_S + \\
\begin{bmatrix} 0 & \frac{2d-1}{L} & 0 & 0 & 0 & 0 \\ \frac{1-2d}{C_1} & -\frac{2}{C_1 r} & \frac{2d-1}{C_1 r} & \frac{2d-1}{C_1 r} & \frac{1-d}{C_1 r} & \frac{2-3d}{C_1 r} \\ 0 & \frac{2d-1}{C_2 r} & -\frac{1}{C_2 r} & 0 & 0 & \frac{1-d}{C_2 r} \\ 0 & \frac{2d-1}{C_3 r} & 0 & -\frac{1}{C_3 r} & \frac{1-d}{C_3 r} & \frac{1}{C_3 r} \\ 0 & \frac{1-d}{C_4 r} & 0 & \frac{1-d}{C_4 r} & \frac{R(d-1)-r}{C_4 r R} & \frac{R(d-1)-r}{C_4 r R} \\ 0 & \frac{2-3d}{C_5 r} & \frac{1-d}{C_5 r} & \frac{1}{C_5 r} & \frac{R(d-1)-r}{C_5 r R} & \frac{R(d-2)-r}{C_5 r R} \end{bmatrix} \begin{bmatrix} I_L \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{1}{L} \\ -\frac{d}{C_1 r} \\ \frac{d}{C_2 r} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_S \hat{d} \\
\hat{v}_O = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L & \hat{v}_{C1} & \hat{v}_{C2} & \hat{v}_{C3} & \hat{v}_{C4} & \hat{v}_{C5} \end{bmatrix}^T
\end{cases} \tag{30}
$$

$$
\frac{\hat{v}_0}{\hat{v}_S} = \frac{-3.332\times10^{11}\,s^4 - 5.925\times10^{17}\,s^3 - 2.522\times10^{23}\,s^2 + 1.14\times10^{25}\,s + 1.389\times10^{30}}{s^6 + 6.32\times10^6\,s^5 + 1.147\times10^{13}\,s^4 + 7.179\times10^{18}\,s^3 + 9.589\times10^{23}\,s^2 + 4.018\times10^{25}\,s + 1.026\times10^{29}} \tag{31}
$$

$$
\frac{\hat{v}_0}{\hat{d}} = \frac{-2.304\times10^5\,s^5 - 2.058\times10^{12}\,s^4 - 3.164\times10^{18}\,s^3 - 1.435\times10^{24}\,s^2 - 1.525\times10^{29}\,s + 3.875\times10^{32}}{s^6 + 6.32\times10^6\,s^5 + 1.147\times10^{13}\,s^4 + 7.179\times10^{18}\,s^3 + 9.589\times10^{23}\,s^2 + 4.018\times10^{25}\,s + 1.026\times10^{29}} \tag{32}
$$

VI. Simulation and Experimental Validation

The hardware setup of the IGSIDSC is illustrated in Fig. 14, and its specification is listed in Table III. To endorse the performance of the IGSIDSC, a laboratory prototype for the power rating of 200 W is developed. The developed prototype has a source voltage of 48 V, which operates with a 34.06% duty ratio to achieve 650 V of output voltage as per the theoretical calculation. The SiC devices are used for the implementation of the prototype to improve the converter performance. Here, the programmable DC source IT6000C will supply the power to the IGSIDSC. The switching pulse of 50 kHz is generated using LAUNCHXL-F28379D and it is fed to the gate driver HCPL3101 to drive the MOSFET SCTW35N65G2VAG. The proposed converter has been simulated in PSIM platform and the results are presented in Fig. 15(a) - Fig. 15(e), and the experimental results are depicted in Fig. 16(a)- Fig. 16(e). Both simulation and experimental investigations were carried out for the same specifications.

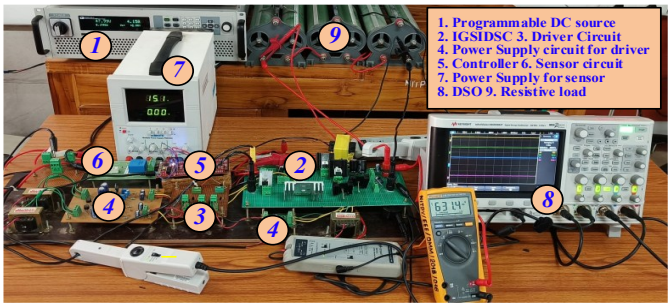
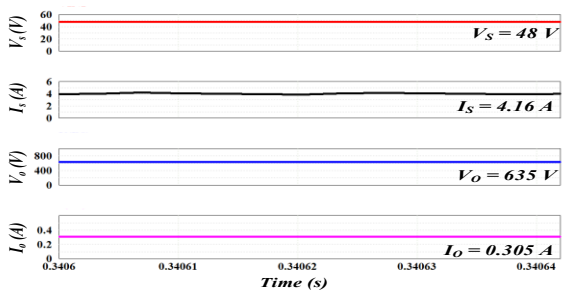


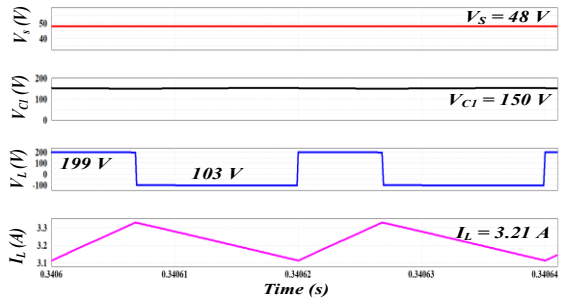
Fig. 14. Hardware prototype of the IGSIDSC converter for experimental validation.

TABLE III
SPECIFICATION OF THE COMPONENTS

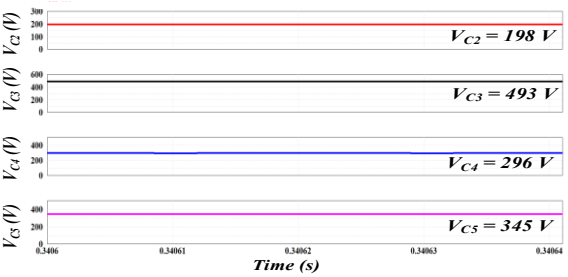
Components	Rating/Part Number
V_S, V_O, P_O and f_s	48 V, 650 V, 200 W & 50 kHz
Inductor & Capacitors	5 mH & 10 µF
MOSFETs	SCTW35N65G2VAG
Diodes	IDH10G65C6
Load (R_O)	2112.5 Ω



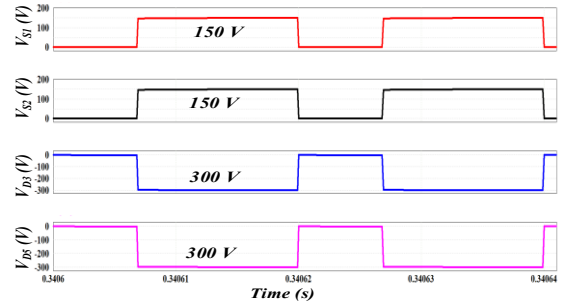
(a) Source voltage (V_S), source current (I_S), output voltage (Vo), and output current (Io).



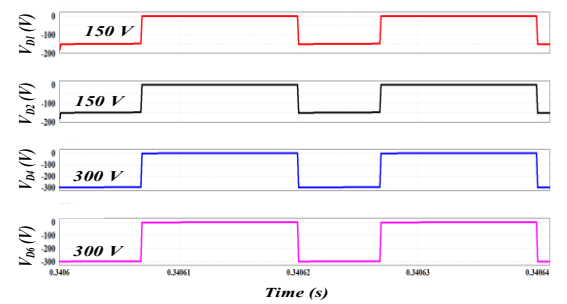
(b) Source voltage (V_S), capacitor voltage (V_{C1}), inductor voltage (V_L), and inductor current (I_L).



(c) Capacitor voltages (V_{C2}, V_{C3}, V_{C4}, and V_{C5}).

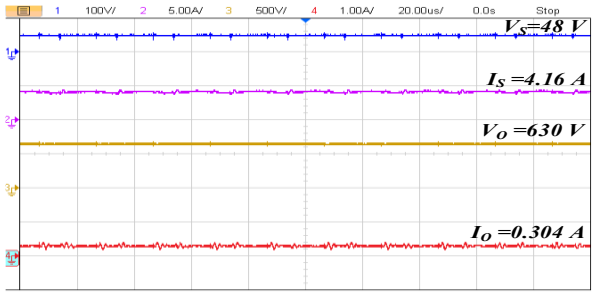


(d) Voltage stress on switches (V_{S1}, V_{S2}), and diodes (V_{D3}, V_{D5}).

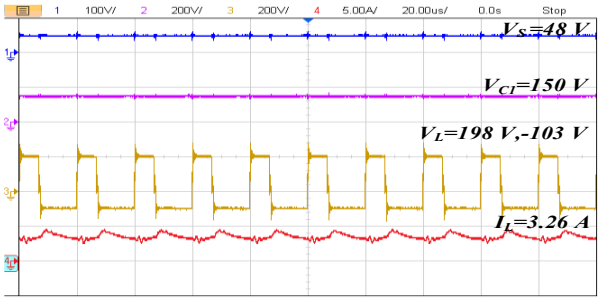


(e) Voltage stress on diodes (V_{D1}, V_{D2}, V_{D4}, V_{D6}).

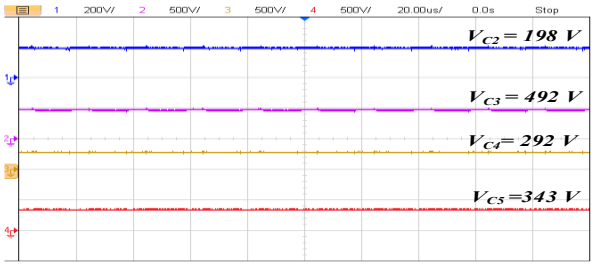
Fig. 15. Simulation steady-state results for the IGSIDSC converter.



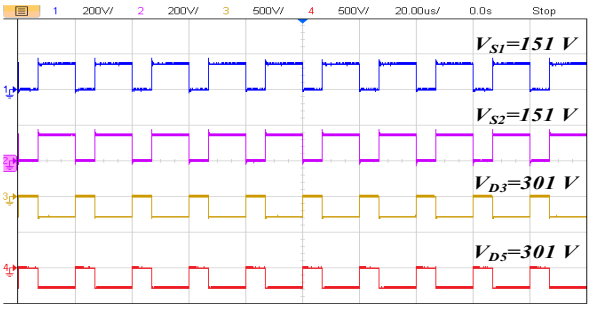
(a) Source voltage (V_S), source current (I_S), output voltage (Vo), and output current (Io).



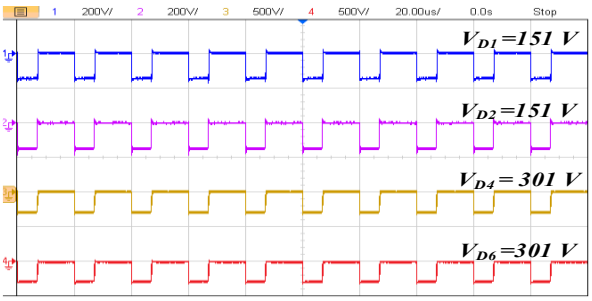
(b) Source voltage (V_S), capacitor voltage (V_{C1}), inductor voltage (V_L), and inductor current (I_L).



(c) Capacitor voltages (V_{C2}, V_{C3}, V_{C4}, and V_{C5}).



(d) Voltage stress on switches (V_{S1}, V_{S2}), and diodes (V_{D3}, V_{D5}).



(e) Voltage stress on diodes (V_{D1}, V_{D2}, V_{D4}, V_{D6}).

Fig. 16. Experimental steady-state results for the IGSIDSC converter.

The IGSIDSC prototype delivers an output of 630 V and 0.304 A from an input of 48 V and 4.16 A, with a duty ratio of 34.06%, as portrayed in Fig. 16(a). Due to effect of parasitic resistance, the converter produces an output of 630 V instead of 650 V, when it is operated at theoretically calculated duty ratio of 34.06%. This results in an efficiency of 95.91% for the IGSIDSC. In Fig. 16(b) illustrates the source voltage (V_S), capacitor voltage (V_{C1}), inductor voltage (V_L), and inductor current (I_L). The inductor is energized with a voltage of 198 V (V_S+V_{C1}) and de-energized with a voltage of -103 V (V_S-V_{C1}), with an average current of 3.26 A. The remaining capacitor voltages V_{C2}, V_{C3}, V_{C4} and V_{C5} are 198 V, 492 V, 290 V, and 340 V, respectively, as portrayed in Fig. 16(c). The output voltage is the sum of capacitor voltages V_{C4} and V_{C5}. Also, in Fig. 16(d), the voltage stress across V_{S1}, V_{S2}, V_{D3} and V_{D5} are depicted. MOSFETs S_1 and S_2 have a voltage stress of 151 V, i.e., V_0/4.3, and diodes D_3 and D_5 have voltage stress of 301 V, i.e., V_0/2.16, respectively. In Fig. 16(e), diodes D_1 and D_2 have voltage stress of 151 V, i.e., V_0/4.3, diodes D_4 and D_6 have voltage stress of 301 V, i.e., V_0/2.16, respectively. It is obvious from Figs. 15 – 16, both simulation and experimental results are closely matching each other and this validates the proposed IGSIDSC. All the devices experience lower voltage stress across them, which is much lesser than the output voltage. It is evident from the experimental waveform that the IGSIDSC achieves high voltage gain with a minimal duty ratio and fewer component counts. A significant benefit of the IGSIDSC is the reduced voltage stress.

The plot illustrated in Fig. 17 (a) compares the analytical efficiency calculated using (21–25) and experimental efficiency of the IGSIDSC for various power ratings. It shows that the analytical and experimental efficiency are closely matching at the 200 W power rating. Similarly, Fig. 17 (b) depicts the analytical and experimental efficiency of the proposed converter for different input voltages at 200 W. The plot reveals that the analytical and experimental efficiencies are closely matching.

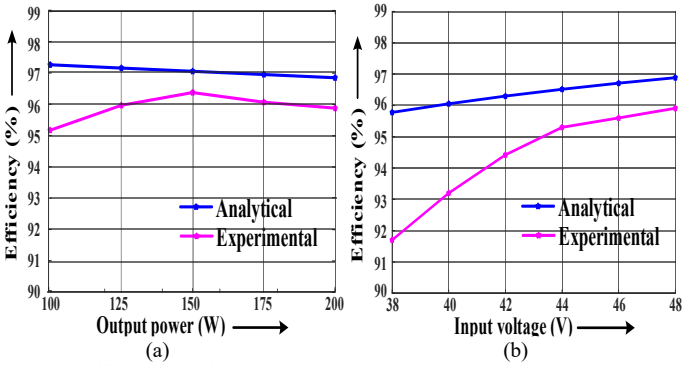
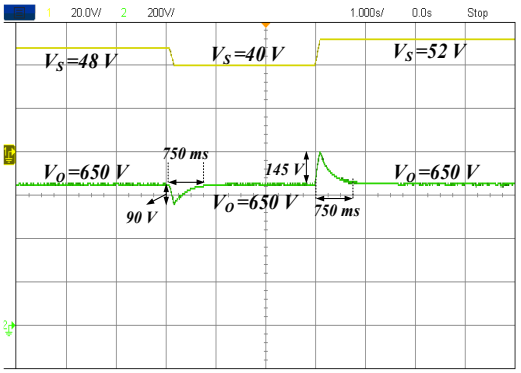
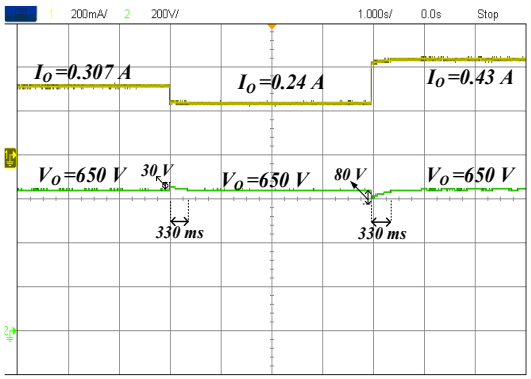


Fig. 17. Efficiency analysis of the IGSIDSC converter: (a) Comparison of analytical and experimental efficiency across various power ratings; (b) Comparison of analytical and experimental efficiency at different input voltages.

To evaluate the dynamic performance of the system in regulating the output voltage under source side and load side disturbances, an experimental investigation has been carried out by changing the input from 48 V to 40 V and then to 52 V. During transitions from 48 V to 40 V and from 40 V to 52 V, a voltage dip of 90 V and a rise of 145 V were observed respectively. In both cases, the output voltage settles to the targeted voltage of 650 V after 750 ms.



(a) Output voltage (V_o) regulation under a step change in input voltage (V_s).



(b) Output voltage (V_o) regulation under a step change in load current (I_o).

Fig.18. Experimental dynamic results for the IGSIDSC converter.

Similarly, in order to introduce load disturbance, the load resistance is changed to vary the load current from 0.307 A to 0.24 A and then to 0.43 A. During these load changes a voltage rise of 30 V and a dip of 80 V were observed respectively. In both cases, the output voltage settles to the targeted voltage of 650 V after 330 ms. Despite the disturbance on the source side and load side, the controller effectively maintains the output voltage at 650 V, as depicted in Fig. 18.

These experimental observations highlight the successful implementation and performance of the designed controller in mitigating disturbances both on the source and load sides, ensuring reliable and stable output voltage regulation.

VII. Conclusion

An Improved Gain Single Inductor Dual Switch Converter (IGSIDSC) is designed and demonstrated in this work. By strategically improving gain, the operating duty-ratio is reduced and voltage stress across the devices is minimized, which helped to address the common concerns found in existing high gain converters. The focus on minimizing the operational duty ratio ensures reduced stress on the switches and diodes, thereby enhancing overall performance. Utilization of SiC devices with a single inductor reduces size and improves efficiency. The proposed IGSIDSC is simulated in PSIM platform and their results are validated through investigations on a 200 W laboratory prototype. The prototype gives an output of 630 V from 48 V input for theoretically determined duty ratio of

34.06%, with 95.91% efficiency. Further, steady-state analysis, investigation on parasitic effects, and analysis of small-signal models are carried out to validate the performance of the IGSIDSC. In addition to that, the transient responses during load and source side disturbances are experimentally investigated. And the common ground feature enhances reliability and makes the IGSIDSC suitable for various applications, including PV and fuel cell systems, etc. Overall, the IGSIDSC reported in this paper demonstrates a significant advancement in high gain converter operation, offering solutions with substantial advantages like high gain, reduced duty ratio, minimized voltage stress, common ground utilization, and less component count over existing converters.

VIII. APPENDIX -I

Voltage gain derivation of proposed IGSIDSC

A. Calculation of voltage gain in CCM

The vol-sec balance approach for inductor L (From 1 & 2), the equation (33) - (37) has been formulated.

$$(V_S + V_{C1})\, d = (V_{C1} - V_S)(1-d) \tag{33}$$

$$V_{C2}\, d = (V_{C1} - V_S)\,(1-d) \tag{34}$$

$$(V_S + V_{C1})\, d = (V_{C5} - V_{C2} - V_S)\,(1-d) \tag{35}$$

$$(V_{C3} - V_{C5} - V_S)\, d = (V_{C1} - V_S)\,(1-d) \tag{36}$$

$$(V_S + V_{C1})\, d = (V_o - V_{C3} - V_S)\,(1-d) \tag{37}$$

The voltages of five capacitors and the voltage gain (M_V) of the IGSIDSC are calculated using (33) - (37), presented below.

$$V_{C1} = \frac{V_S}{1-2d}; V_{C2} = \frac{2V_S(1-d)}{1-2d}; V_{C3} = \frac{2V_S(d^2-3d+2)}{2d^2-3d+1};$$
$$V_{C4} = \frac{2V_S}{1-2d}; V_{C5} = \frac{V_S(2d^2-5d+3)}{2d^2-3d+1} \tag{38}$$

$$M_V = \frac{V_o}{V_S} = \frac{2d^2-7d+5}{2d^2-3d+1} \tag{39}$$

B. Calculation of voltage gain in DCM

DCM gain is derived using power balance method

$$P_{in} = P_{out} \tag{40}$$

$$V_S * I_S = \frac{V_o^2}{R} \tag{41}$$

$$V_S * (I_{LA} + I_{D3A}) = \frac{V_o^2}{R} \tag{42}$$

From the analytical waveform in Fig.5(b), inductor average current is given below:

$$I_{Lavg} = \frac{1}{2}(d + d_x) I_{LP} \tag{43}$$

By employing (6) and (7), the expression for D_x is obtained as follows,

$$d_x = \frac{(V_S + V_{C1})\, d}{V_{C1} - V_S} \tag{44}$$

Substitute (6) & (44) in (43), the expression for I_{LA} is obtained as follows,

$$I_{LA} = \frac{V_S(1-d)\, d\, T}{(1-2d)\, L} \tag{45}$$

Substitute (17) & (45) in (42), The voltage gain (M_{DCM}) of the IGSIDSC is obtained

$$M_{DCM} = \frac{V_o}{V_S} = 0.5 + 0.5\sqrt{1 + \frac{4(1-d)\, d}{(1-2d)\tau_L}} \tag{46}$$

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