A New Solution based on Multi-objective Algorithm for Multi-application Mappings for Many-Core Systems

M. A. Almeida, I. F. Gallon, and E. C. Pedrino

***Abstract*— Mapping multiple applications onto intra-chip communication structures, such as Network-on-Chip (NoC), commonly used in the context of manycore systems, is a problem classified as NP-hard. This is due to the need for the simultaneous optimization of performance, reliability, and energy efficiency metrics. For instance, it is essential to account for heat dissipation effects throughout the system, while also ensuring fault tolerance and proper load balancing. While there is still a limited number of works in the literature addressing the allocation of multi-applications in NoCs, many studies focus on the mapping of single applications. Therefore, this paper proposes a multi-objective mapping model that targets performance metrics and heat distribution for multi-application scenarios in manycores with NoCs, aiming to contribute to this area. The results obtained are compared with a state-of-the-art algorithm for this scenario, showing promising improvements, with more than 30% reduction in latency and 38% increase in fault tolerance when all applications are considered.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9346

***Index Terms*—many-core, network-on-chip, task mapping, metrics.**

I. Introduction

TECHNOLOGICAL advances in the manufacture of ICs (Integrated Circuits) have enabled the integration of a greater number of components onto a single chip. This progress has led to the construction of devices with an increasing number of processing cores, especially in embedded systems. For some years now, multicore and manycore devices have been utilizing lower operating frequencies [1]–[3] because the performance demands can no longer be met by increasing the frequency of single-core operation alone [4]–[7]. Another challenge in this scenario is the distribution of mono-application or multi-application tasks among these cores, which is not trivial to solve in practice. Depending on the arrangement chosen, latency and/or power distribution throughout the chip may be compromised. In manycore devices, the basic principle used to address this problem involves dividing applications into smaller tasks that can be efficiently allocated to different cores for parallel execution [8], [9]. This approach allows for better synchronization control, memory management, and reliability in executing parallel code [10], [11]. Therefore, mapping application tasks in these systems involves establishing a communication scheme between them, aiming to optimize hardware variables such as energy consumption, computational performance, voltage, frequency, and others, as exemplified in [12]. However, the optimization involving two or more objectives in multi-applications for NoC mapping can be further explored.

Furthermore, as stated in [13]–[15], to optimize communication delays and energy consumption, tasks should be mapped to the same core or close to each other. These optimizations are necessary to meet the constraints of each application. Thus, there is a need to develop more efficient mapping methodologies that can provide optimal mappings satisfying the demands of different applications. This problem is classified as NP-hard [13], so heuristics based on application domain knowledge must be employed to find an optimized solution.

Current strategies for task distribution in systems with many cores depend on the number of applications to be executed. In scenarios with fixed or variable workloads, improvements to task distribution in these architectures are made during the design or execution phase, respectively. These architectures can be uniform (with identical cores) or heterogeneous (with different cores). During runtime distribution, one core manages tasks such as scheduling, resource control, configuration, and migration. This distribution can be centralized, distributed, or a combination of both [8], [16], [17]. Distributions made during the design phase are best suited for static workloads, where a predefined set of applications with known computing and communication behaviors are considered. Dynamic changes to applications while running [18], [19] are not supported on these systems.

In [24] combine the benefits of evolution-based search with a learning-based local search to quickly determine the PE and communication link placement to optimize multiple objectives (e.g., latency, throughput, and energy) in 3D NoC-enabled manycore heterogeneous systems. It is a promising technique that can be benchmarked in future work.

[25] is a proposed technique that uses an ML-based model to extract relevant information from research data and incorporate it into the research process. This results in a more robust model with a higher convergence rate and solution quality.

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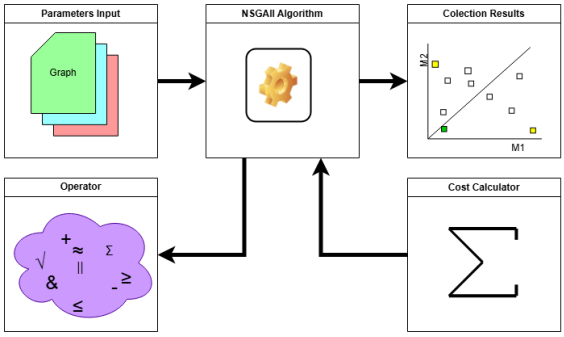

Fig. 1. Block Diagram of the Proposed Model.

In Fen Ge et al. [20], an efficient method called multi-phase is presented, which is used to solve the mapping of many applications in two phases. This work is one of the few in the literature to explore this idea, as most others only deal with mapping mono-applications. The multi-phase algorithm first allocates the best areas for mapping each of the given applications, and then maps these areas to optimized regions of the NoC (Network on Chip). However, the heat distribution throughout the chip, given by this solution, is not optimal, as it does not consider finding idle cores between the mapped tasks. Additionally, the optimization presented occurs in two steps using an evolutionary algorithm, making it less flexible if the user decides to work with other metrics in this scenario. Therefore, the motivation of this article is to propose an alternative and flexible solution, regarding the use of metrics in this context, to the work of Fen Ge et al. [20]. Through a multi-objective optimization algorithm, it is possible to simultaneously improve performance in executing multi-application tasks and achieve better energy distribution throughout the chip. This approach aims to solve the problem encountered by [20].

II. Solution Structure and Problem Presentation

As observed, the problem of mapping multiple applications onto a NoC to balance various objectives including fault tolerance, computational load, latency, communication load, and energy requirements—while optimizing more than one of these requirements simultaneously, remains largely unexplored. Therefore, this paper presents a proposal to map multiple applications with multiple objectives onto a 2D NoC.

In Fig. 1, an overview of the proposal is presented. The system is composed of a Parameter Entry module, which defines execution configurations and organizes the graphs to be used by the PlatEMO [21] optimizer, in which an NSGAII Algorithm [22], [23] module performs the optimization of the simultaneous metrics desired by the user who, in this work, these will be the latency and fault tolerance metrics. The Cost Calculation module calculates the costs of each individual in the population offered by the algorithm, the Operator module performs the task of diversifying the population and, finally, the Results Generation module presents the set of solutions obtained.

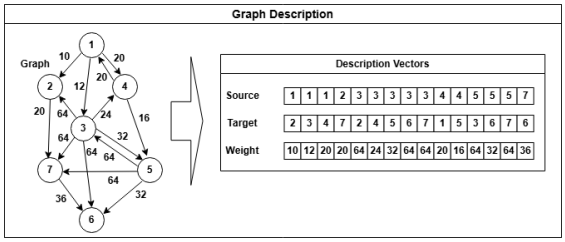

Fig. 2. Conversion of a graph into 3 vectors. Source- source node, Target- destination node, Weigth- Bandwidth occupation of the arc.

A. Parameter Input

1) Parameters: The system needs some parameters for its execution, so it is necessary to provide several application graphs in which you want to find the best arrangement for optimizing the intended metrics, as already mentioned above, and also, the user needs to specify the grid size of the Study NoC.

2) Graphs: Graphs are provided through a set of vectors that describe the origin and destination of each arc of a given graph, their respective communication weight, where the number of positions in each vector is equal to the number of arcs in each graph. Each application is represented by a graph and each graph is represented by a set of three vectors. Fig. 2 illustrates how the graph is represented. The Source vector contains a sequence of tasks and the value of each position represents the origin task of the arc. In the Target vector, each position represents the target task and the Weight vector is the weight of the arc. Thus, in the three vectors, each position represents an arc, for example, in position 1 we have the starting point of an arc in the Source vector, the end point of this same arc in the Target vector, and the communication weight of this arc in Weight.

3) NoC Mapping: The way to represent an application in the NoC structure can be seen in Fig. 3 , and occurs through a pair Task, PE, where Task is the identification of the task, and PE is the processor.

4) Compound Graph: The graphs are joined into a single graph that is used in optimization, as seen in Fig. 4 and algorithm1, the vectors are joined into a sequence, and the tasks receive a new numbering, which allows the algorithm to treat all applications as a single chromosome (individual).

Algorithm 1 Create Graph Vectors.

$S \leftarrow (S_1, S_2, \ldots, S_n)$
$T \leftarrow (T_1, T_2, \ldots, T_n)$
$W \leftarrow (W_1, W_2, \ldots, W_n)$
return Create vectors with all applications.

B. NSGAII Agorithm

The NSGAII Algorithm [22], [23] is used as the optimization algorithm for the proposed metrics. In this work, the implementation of this algorithm provided by PlatEMO was used as a base. To use this tool, the proposed chromosome was adapted to it, allowing the description of new customized

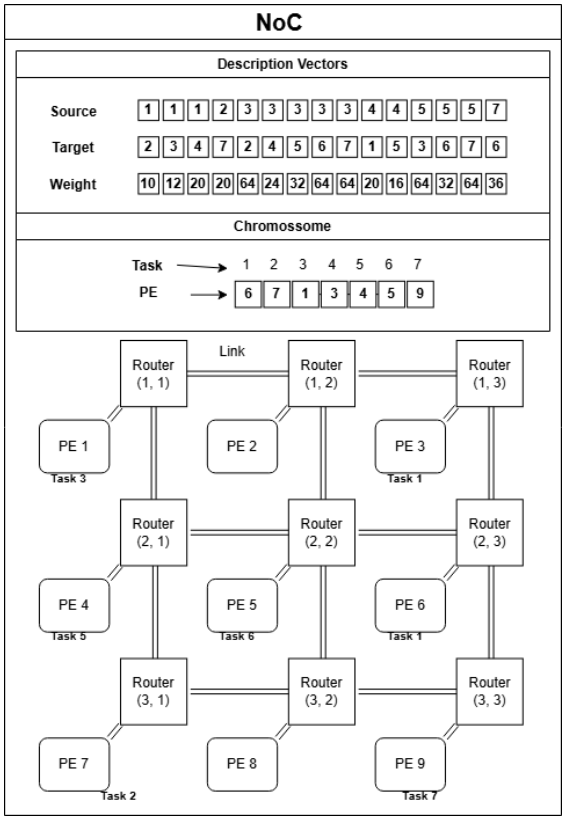

Fig. 3. Conversion of the chromosome into a NoC mapping.

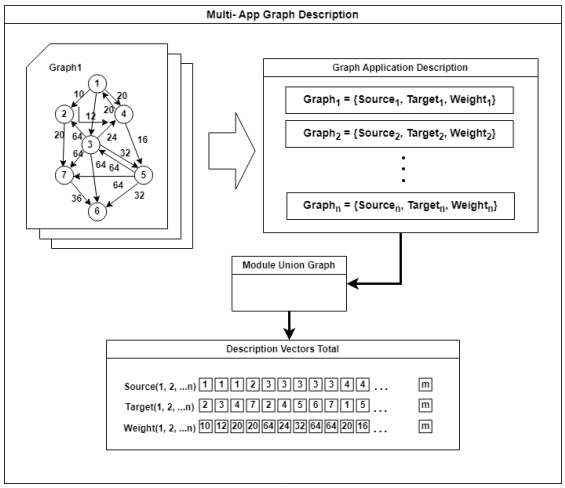

Fig. 4. Conversion of application graphs into a single vector.

solutions regarding the generation of the initial population, genetic operators, and involved cost calculations. More details on this can be found in the PlatEMO Manual. The choice of NSGAII was based on its availability in the tool, its nature as a multi-objective algorithm, ease of configuration and its good performance in initial tests, when compared with NSGAIII, MOPSO and MOEA/D.

C. Cost Calculator

This module receives the algorithm's population and calculates the cost for each expected objective. For the communication cost, the cost between tasks of the same arc is summed, and the communication cost between two tasks is calculated by the cost given by the graph multiplied by the number of routers needed to go from the source task ($source_i$) to the destination task ($target_i$) see(1). The fault tolerance and performance metrics studied are presented below, where r is the number of rows of the NoC and c is the number of columns and $nearestIdle$ is the closest node see(2).

$$Perf = \sum_{i=0}^{c-1} distance[source_i, target_i] - 1 \quad (1)$$

$$Ftol = \sum_{i=0}^{r-1} \sum_{j=0}^{c-1} distance[(r, c), nearestIdle] - 1 \quad (2)$$

D. Genetic Operators

The genetic operators used in PlatEMO receive the population, given by the chromosome description mentioned above, and perform the diversity operation, altering the population and searching for new solutions. They first execute a crossover between individuals and then a permutation.

In this phase, the results found, containing the best solutions, are saved in a database on the computer.

III. Experimental Analysis

To verify and validate the new multi-application mapping approach (Multi-Objective), a test similar to the one proposed in [20] is used as a reference (Multi-Phase). Benchmark graphs are used with 12, 16, 20 and 25 tasks, being App 12, App 16, App 20 and App 25 respectively (MPEG4, VOPD, WIFIRX and VCE), benchmark with graphs known in the literature executed simultaneously on a corresponding number of cores in a 9x9 NoC platform, where this process is repeated 100 times.

The proposal is evaluated considering the set of all applications for latency and fault tolerance metrics. In Table I, the methods (Multi-Objective and Multi-Phase) are compared for latency and fault tolerance metrics. Fig. 5 demonstrated, empirically, that the Multi-Objective proposal has a lower total latency than the Multi-Phase proposal. In Fig. 6, the total fault tolerance is much lower than in the Multi-Phase method. The proposed method achieves better results by fully utilizing the available area without being constrained by the geometry of the grid formed by task allocation. It also optimizes two metrics—latency and fault tolerance—while the Multi-Phase method is limited to a rectangular geometry and focuses on a single metric, latency.

In Figs. 8 (best latency - current proposal), 9 (best fault tolerance - current proposal), 10 (balanced latency and fault tolerance - current proposal), it is possible to visualize the results of the application maps generated in each case, for each approach, according to the Pareto curve given in Figs. 7 - A, B and C respectively, generated by the current proposal. The reader should note that the graph is not to scale. In Fig. 11, (compared map - Multi-Phase) the map for the Multi-Phase method is presented for optimizing the latency metric. All the maps are in a 9X9 NoC.

TABLE I
COMPARISON BETWEEN MULTI-OBJECTIVE AND MULTI-PHASE, LATENCY AND FAULT TOLERANCE

Method	Objective	Min	Q1	Q3	Max
Multi-Objective	Latência	8400	**14000**	20290	37800
Multi-Objective	FT	2611	**2724**	2866	3002
Multi-Phase	Latência	11200	25200	39200	75600
Multi-Phase	FT	3604	4260	4260	4260

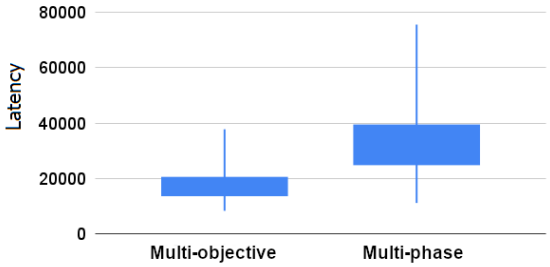

Fig. 5. Comparison chart of Latency obtained in both methods.

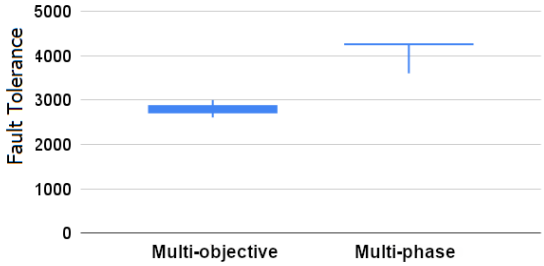

Fig. 6. Comparison chart of Fault Tolerance obtained in both methods.

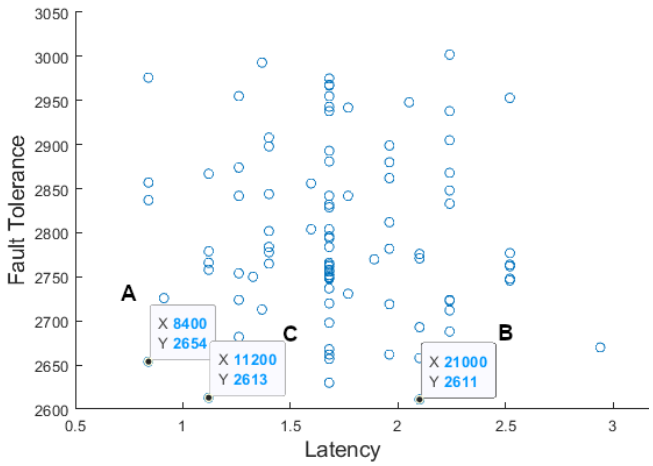

Fig. 7. Multi Objective Results. A-Improved Latency, B-Improved Fault Tolerance and C-Improved General (Latency and Fault Tolerance).

IV. CONCLUSION

In this proposal, a multi-objective optimization solution for generating multi-application maps on manycore architectures was presented and compared with the multi-application mapping proposal multiphase presented by Fen Ge et al. [20]. The Multi-Objective proposal demonstrates efficiency

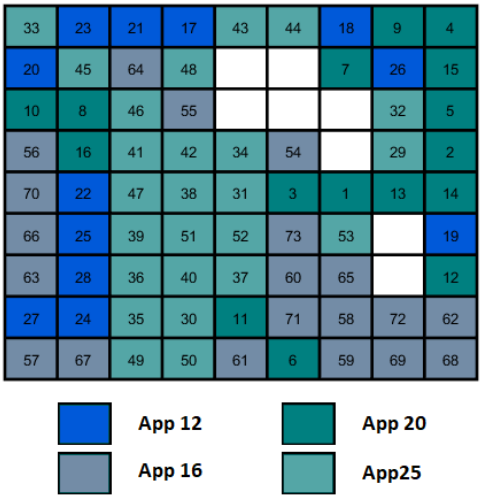

Fig. 8. A- Mapping Representation in NoC for Multi-Objective Improved Latency.

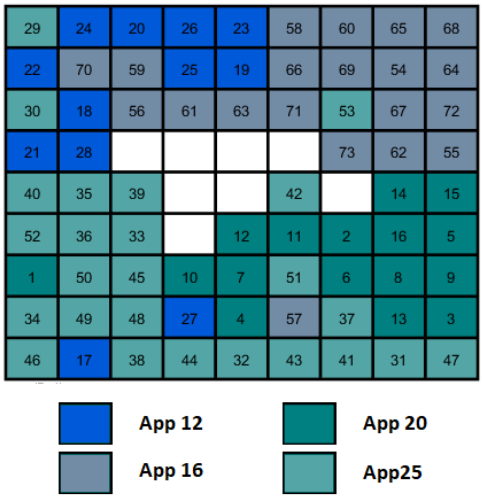

Fig. 9. B- Mapping Representation in NoC for Multi Objective Improved Fault Tolerance.

in achieving balanced results between the chosen metrics, performing a more effective mapping in the use of the NoC, better exploiting the available area, with improvements of over 30% in latency and 38% in fault tolerance. Additionally, it executes more quickly by optimizing all applications at once, thus better exploring the distribution of tasks in the NoC, without restricting areas or blocking processors. Furthermore, individual applications may have better latency values with the [20] proposal, but this does not guarantee better latency in the Noc when all are used. In this work, only one optimization algorithm, NSGAII, is used to evaluate the performance of a multi-objective algorithm compared to a single-objective algorithm in mapping tasks in a NoC. Therefore, an evaluation of other algorithms is necessary. In future works, Multi-objective optimization algorithms will be compared for mapping tasks in NoC across multiple applications.

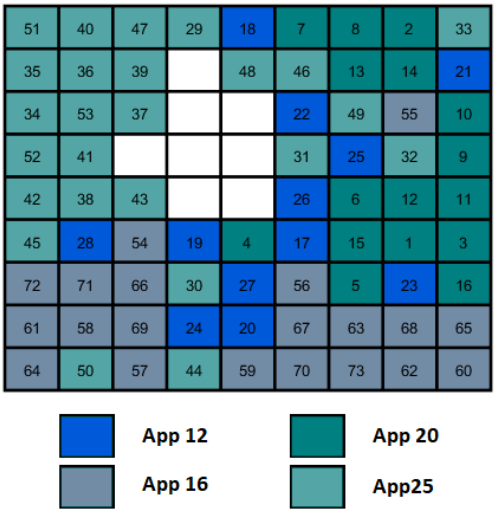

Fig. 10. C- Mapping Representation in NoC for Multi Objective Improved General (Latency and Fault Tolerance).

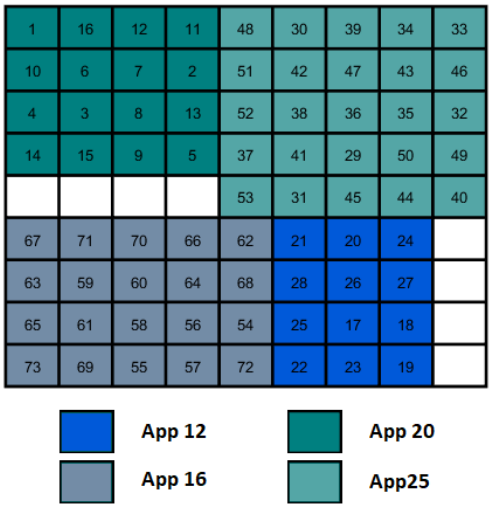

Fig. 11. Representation of Mapping in NoC for the Multi-Phase Solution.

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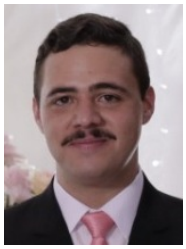

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