Design of a Transformerless DC Regulator with Reduced Redundant Power Processing for a Residential DC Microgrid

Iván Reyes, Saúl Méndez, Jorge Morales, Claudia Rivera, and Dora Castro

***Abstract*—The current energy requirements of the residential, industrial, and commercial sectors are met by direct current (DC) electronic loads. Distributed generation (DG) systems which use photovoltaic systems, domestic wind generators, and grid integration, require maximizing energy transfer efficiency in these systems. The DC/DC converters integrated as interfaces between different sources of DG systems have the funtion to optimize the energy transferred to the DC bus. This paper proposes integrating a Quadratic Buck converter with reduced power processing as an interface between DG system sources and the DC bus. The design and operation of the converter in continuous conduction mode, as well as its average and linear models, are presented. The analysis of the reduced redundant power processing in the converter is also provided, along with the design of the DC bus voltage regulator.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9240

***Index Terms*—DC/DC, Power electronics, R^2P^2, Transformerless DC, DC microgrid, Quadratic Buck converter.**

I. Introduction

DC MICROGRIDS have garnered interest as an efficient and innovative solution for integrating storage systems, renewable energy generators, and DC loads [1]–[3]. The rise in the use of DC loads, such as LED lighting, computers, and household appliances, has made DC microgrids essential for future energy systems [4], [5]. These systems incorporate power electronic converters as interfaces between distributed generation (DG) sources and the DC bus [6], [7]. To ensure stable operation, these converters require adaptive regulation systems capable of responding to the varying demands of the load connected to the DC bus [8]. Conventional converters, such as Buck, Boost, and Buck-Boost, are widely used in these applications due to their simplicity of implementation and operation [9]. However, high conversion gains requires that these converters to operate at high duty ratios. This imposes a restriction on the switching frequency and generates higher energy stress levels due to the extended turn-on intervals of the semiconductors [10]. Single-stage power processing causes magnetic elements and semiconductors to handle high current levels, affecting power density and efficiency [11]. In applications requiring voltage reduction and current boosting, Buck converters are used because of their advantages, such as ease of implementation and minimal phase dynamics relative to the output voltage variable [12]. However, Buck converters have high current levels in the inductor, which increases conduction losses. Another disadvantage is the discontinuous current at the converter input, which is unsuitable for distributed generation sources like PV panels, wind turbines, and fuel cells [13]–[15]. An LC filter can be incorporated as a solution to this issue. Residential DC microgrids incorporate DC/DC converters to regulate a direct current bus with standard voltages of $12/24/48\ V$ [16]–[18]. Fig. 1 shows the classic schematic of a DC microgrid incorporating renewable energy sources, backup the interconnection to the grid and a battery bank.

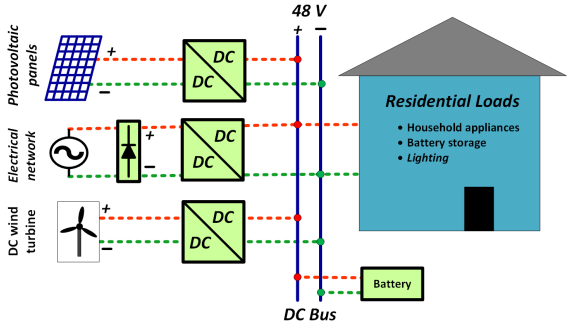

Fig. 1. Classic structure of a DC microgrid for residential loads.

High current levels applications pose a significant challenge from an efficiency standpoint because increased conduction losses directly affect overall efficiency. Some trends suggest using traditional non-isolated Buck converters enhanced with switched capacitive or inductive cells [19]. These topologies achieve higher voltage conversion ratios than the conventional Buck structure [20], [21]. Another alternative is cascaded quadratic Buck structures, which operate with low semiconductor stress and within the range of $0.4 < D < 0.7$. However, a drawback of these structures is that process the power supplied by the source twice before reaching the load, thereby reducing overall efficiency. Some step-down converters use zero voltage switching (ZVS) and zero current switching

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Iván Alfonso Reyes-Portillo, and D. Castro are with the Polytechnic University of San Luis Potosí, San Luis Potosí, México (e-mails: ivan.reyes@upslp.edu.mx, and dora.castro@upslp.edu.mx).

S. Méndez, and J. Morales are with Autonomous University of San Luis Potosí, San Luis Potosí (e-mails: saul.mendez@uaslp.mx, and jmorales@uaslp.mx).

C. Romero is with National Institute of Astrophysics, Optics and Electronics, Puebla, México (e-mail: c.a.riveraromero@inaoe.mx).

(ZCS) techniques to enhance efficiency. Nonetheless, these methods compromise the simplicity of circuit design and are restricted to a specific operating frequency to maintain the resonant effect of soft switching. In [22], [23] discuss various topologies derived from the Buck configuration, which offer simpler structures at the expense of conversion capability. Standard DG source voltages range from 120 V to 380 V, and for high conversion ratios, high gain converters are required [2], [9]. This paper proposes the design of a Quadratic Buck converter with Reduced Redundant Power Processing (R^2P^2) as an interface between distributed generation (DG) sources and the bus of a DC microgrid. This proposal aims to achieve a high current/voltage transformation ratio, improve power density, and attain higher efficiency compared to cascaded structures. The rest of the paper is organized as follows: In Section II, the proposed R^2P^2 based converter and the analysis of its performance are presented. In addition, an analysis of the power processing reduction through the k-factor, along with its average and linear model, is presented. In Section III, the dynamic analysis based on the linear model and the design of the voltage regulation scheme are discussed. Section IV presents the experimental tests that to verify the theoretical results, and Section V provides the final comments.

II. Quadratic Buck Converter with R^2P^2

This paper proposes integrating a Quadratic Buck converter with reduced power processing as an interface between the distributed generation (DG) sources and the bus of a DC microgrid, as shown in Fig. 2. The topology has two modes of operation: Continuous Conduction Mode (CCM), where the currents in the inductors never reach zero, and Discontinuous Conduction Mode (DCM), where the current in the inductors reaches zero for a interval of time. In this work, only CCM will be analyzed.

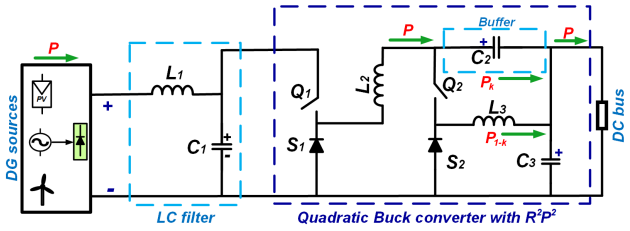

Fig. 2. Quadratic Buck converter with R^2P^2 powered by DG sources.

The topology in CCM (Continuous Conduction Mode) has two states of operation: the "ON Mode," which occurs when switches Q_1 and Q_2 are turned on, while diodes S_1 and S_2 do not conduct current, and the "OFF Mode," which occurs when switches Q_1 and Q_2 are turned off, while diodes S_1 and S_2 are turned on. Fig. 3 shows the electrical networks corresponding to the two operating states of the converter. The inductor L_1 and capacitor C_1 operate as a filter to eliminate discontinuous current being drawn from the DC source, and also help mitigate the effects of electromagnetic interference (EMI) present in the coupling between the control stage and the power stage. In addition, by selecting a frequency of 50 kHz, EMI is minimized compared to higher frequencies, which simplifies the necessary filtering and complies with electromagnetic compatibility (EMC) standards.

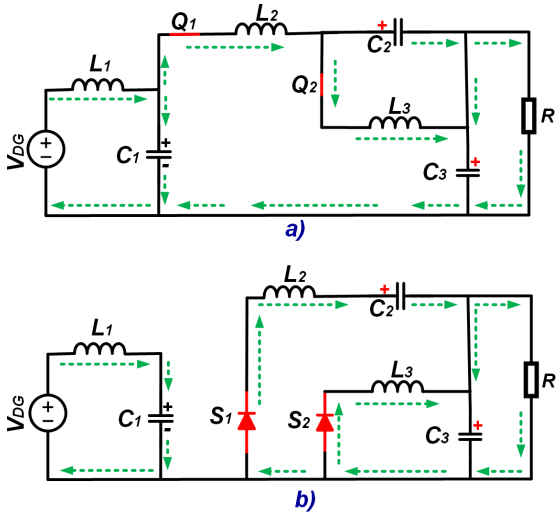

Fig. 3. Electrical networks corresponding to the operating states of the proposed converter in CCM, a) ON state and b) OFF state.

This converter was proposed with an LC filter for PV applications in [24], and belongs to the family of R^2P^2 step-down converters proposed in [25]. Through a steady-state analysis, it is possible to determine the average voltage/current values in the reactive elements (capacitors and inductors) of the R^2P^2 quadratic Buck converter in terms of the source voltage V_{DG}, the nominal duty ratio (D), and load (R). This analysis is valid only for CCM and considers ideal elements.

$$V_{C_1} = V_{DG} \tag{1}$$

$$V_{C_2} = V_{DG}D(1-D) \tag{2}$$

$$V_{C_3} = V_{DG}D^2 \tag{3}$$

$$I_{L_1} = \frac{V_{DG}D^4}{R} \tag{4}$$

$$I_{L_2} = \frac{V_{DG}D^3}{R} \tag{5}$$

$$I_{L_3} = \frac{V_{DG}D^2}{R} \tag{6}$$

The gain (M) in voltage of the converter is given by:

$$M = \frac{V_o}{V_{DG}} = D^2 \tag{7}$$

The following expressions establish the value of the capacitors required for the converter to operate in CCM. It is important to consider the percentage of the voltage ripple (ΔV) according to the requirements of the load.

$$C_1\Delta V_{C_1} = \frac{V_{DG}D^4(1-D)}{f_sR} \tag{8}$$

$$C_2\Delta V_{C_2} = \frac{V_{DG}D^3(1-D)}{f_sR} \tag{9}$$

$$C_3\Delta V_{C_3} = \frac{V_{DG}D^3(1-D)}{f_sR} \tag{10}$$

The following expressions define the value of the inductors:

$$L_1 \Delta I_{L_1} = \frac{V_{DG} D^4 (1-D)}{8 f_s^2 C_1} \tag{11}$$

$$L_2 \Delta I_{L_2} = \frac{V_{DG} D (1-D)}{f_s} \tag{12}$$

$$L_3 \Delta I_{L_3} = \frac{V_{DG} D (1-D)}{f_s} \tag{13}$$

The size of the current ripple in L_1 depends on the value of the capacitor C_1.

A. The k-factor

The R^2P^2 converters reduce the amount of power processed by the DC/DC stage. In some cases, part of this power is processed directly to the load, which enhances efficiency and minimizes overall power losses. The internal division of the rated power within the converter is represented by a factor k. The proposed converter belongs to the I-IIIB structures, and its efficiency is determined by:

$$\eta_T = \eta_1 \eta_2 + (1-k)\eta_2 (1-\eta_1) \tag{14}$$

where η_1 and η_2 are the efficiencies of each basic converter, and $k \in (0,1)$ is the fraction of buffer processed power [26]. For the theoretical calculation of k, the following equations are proposed:

$$k = \frac{P_k}{P_o} \tag{15}$$

where P_k is the power processed by the buffer element and P_o is the output power. The analysis of energy processing in the buffer using "Volt-Ampere (VA) modeling" was proposed in [26], [27] and used in R^2P^2 structures in [28]. This method assumes that the input and output powers are approximately ($P_{in} \approx P_o$), meaning it does not account for losses due to parasitic resistances. Fig. 4 shows the input/output power areas in relation to the average voltage/current values.

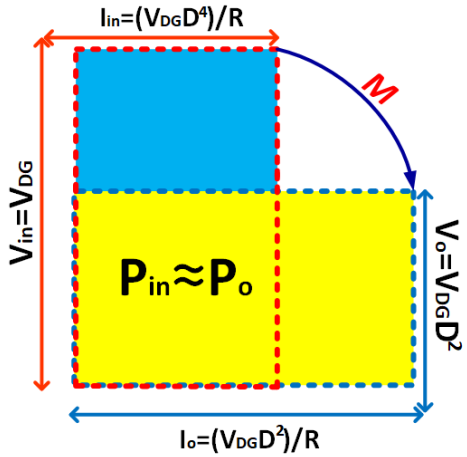

Fig. 4. VA area of the input/output power of the Quadratic Buck converter with R^2P^2.

The power P_k is processed by the capacitor C_2. Equation (16) allows to calculate the power P_k processed in C_2.

$$P_k = I_{C_2}^{+} \cdot V_{C_2} \tag{16}$$

where $I_{C_2}^{+}$ is the average positive current present in capacitor C_2. The positive current in C_2 occurs during the "OFF state" of the converter within a span of the switching period. Equation (17) expresses the average positive current present in capacitor C_2.

$$I_{C_2}^{+} = I_{L_2} \cdot (1-D) = \frac{V_{DG} D^3 \cdot (1-D)}{R} \tag{17}$$

The power processed by the buffer is given by:

$$P_k = V_{DG} D (1-D) \cdot \frac{V_{DG} D^3 \cdot (1-D)}{R} = P_o (1-D)^2 \tag{18}$$

The power processed by the switches S_2 and Q_2 is defined by:

$$P_{SQ} = P_{(1-k)} = P_o (2-D) D \tag{19}$$

The fraction of power transferred by the buffer C_2 is directly related to the k-factor proposed in Equation (20).

$$k = \frac{P_k}{P_o} = \frac{P_o (1-D)^2}{P_o} = (1-D)^2 \tag{20}$$

The Fig. 5 shows the areas of power processed by the buffer element (P_k) and the power processed during the switching of S_2 and Q_2, which is represented by $P_{(1-K)}$.

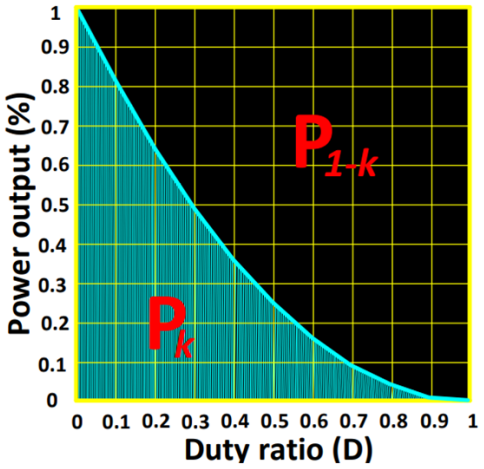

Fig. 5. VA area of power processed by the Buffer (P_k) and the power processed by the S_2 and Q_2.

The proposed converter can process more direct power through the buffer when the duty ratio is less than 0.5. However, a disadvantage is that it increases the stress on the switches by higher peak current in the transistors and longer conduction times in the diodes. Table I presents the comparison of different step-down converter structures with high transformation ratio, considering the number of components, gain, current and voltage stress, and reported efficiency.

B. Converter Modeling

The modeling of the converter was carried out using the state-space technique, analyzing the different electrical networks shown in Fig. 4. This modeling does not consider the

TABLE I
COMPARISON OF STEP-DOWN CONVERTERS

Converter	Proposed	Ref [11]	Ref [12]	Ref [13]	Ref [19]	Ref [20]
Capacitors	3	2	1	2	4	6
Inductors	3	2	1	2	4	3
Switches / Diodes	2 / 2	2 / 2	1 / 1	2 / 2	4 / 0	2 / 1
M (V_o/V_{in})	D^2	D^2	D	$\frac{D^2}{(1-D)^2}$	$\frac{DN_2}{N_1-2N_2}$	$\frac{D}{1-2N}$
Stress (I_Q)	$Q_1=\frac{V_{in}D^4}{R}$	$Q_1=\frac{V_{in}D^4}{R}$	$Q=\frac{V_{in}D^2}{R}$	$Q_1=\frac{V_{in}D^4}{R(1-D)^4}$	X	$Q_1=\frac{1+2N}{(N)I_{aps}}$
current	$Q_2=\frac{V_{in}D^3}{R}$	$Q_2=\frac{V_{in}D^3}{R}$	X	$Q_2=\frac{V_{in}D^3}{R(1-D)^3}$	X	$Q_2=\frac{V_{in}D}{(1+2N)R}$
Stress (V_Q)	$Q_1=V_{in}(1-D)$	$Q_1=V_{in}(1-D)$	$Q=V_{in}(1-D)$	$Q_1=\frac{V_{in}D}{(1-D)}$	$Q_{1,2}=V_{in}\frac{DN_2}{N_1-2N_2}$	$Q_1=\frac{V_{in}D}{1+2N}$
voltage	$Q_2=V_{in}D(1-D)$	$Q_2=V_{in}D(1-D)$	X	$Q_2=\frac{V_{in}D^2}{(1-D)^2}$	$Q_{3,4}=V_{in}\frac{DN_2}{N_1-N_2}$	$Q_2=NV_o$
(I_{in}) continues	Yes	No	No	No	No	No
Power / Efficiency	325 W / 93.04%	50 W/ 82%	220 W / 91.7%	100 W / 91.83%	33 W / 94.8%	120 W / 94%

parasitic resistances present in the electronic devices. The state variables are chosen as follows: $x_1 = I_{L_1}$, $x_2 = I_{L_2}$, $x_3 = I_{L_3}$, $x_4 = V_{C_1}$, $x_5 = V_{C_2}$, $x_6 = V_{C_3}$. These state variables correspond to the currents in the inductors and the voltages in the capacitors. Once the expressions for a switching period have been obtained, a unified model can be derived using a function $q(t)$ where $q(t) = 1$ when the "ON state" is present and $q(t) = 0$ when the "OFF state" is present. Subsequently, averaging $q(t)$ over a switching period results in $<q(t)> = d$, which allows us to obtain an average model, given by:

$$\dot{x}_1 = \frac{V_{DG}}{L_1} - \frac{x_4}{L_1} \tag{21}$$

$$\dot{x}_2 = \frac{x_4 d}{L_2} - \frac{x_5}{L_2} - \frac{x_6}{L_2} \tag{22}$$

$$\dot{x}_3 = \frac{x_5 d}{L_3} - \frac{x_6(1-d)}{L_3} \tag{23}$$

$$\dot{x}_4 = \frac{x_1}{C_1} - \frac{x_2 d}{C_1} \tag{24}$$

$$\dot{x}_5 = \frac{x_2}{C_2} - \frac{x_3 d}{C_2} \tag{25}$$

$$\dot{x}_6 = \frac{x_2}{C_3} + \frac{x_3(1-d)}{C_3} - \frac{x_6}{C_3 R} \tag{26}$$

and expressed in the form $\dot{x} = A(x) + B(x)u$:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \\ \dot{x}_5 \\ \dot{x}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{d}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{d}{L_3} & -\frac{(1-d)}{L_3} \\ \frac{1}{C_1} & -\frac{d}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & -\frac{d}{C_2} & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & \frac{(1-d)}{C_3} & 0 & 0 & -\frac{1}{C_3 R} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{GD} \tag{27}$$

To obtain a linear representation around the operating point of the system, the variables are perturbed with small AC signals, such that $d = D + \widetilde{d}$, $V_{DG} = V_{DG} + \widetilde{v}_{DG}$, $x = X + \widetilde{x}$, resulting in:

$$\dot{\widetilde{x}}_1 = \frac{\widetilde{v}_{DG}}{L_1} - \frac{\widetilde{x}_4}{L_1} \tag{28}$$

$$\dot{\widetilde{x}}_2 = \frac{\widetilde{x}_4 D}{L_2} - \frac{\widetilde{x}_5}{L_2} - \frac{\widetilde{x}_6}{L_2} + \frac{V_{GD}\widetilde{d}}{L_2} \tag{29}$$

$$\dot{\widetilde{x}}_3 = \frac{\widetilde{x}_5 D}{L_3} - \frac{\widetilde{x}_6(1-D)}{L_3} - \frac{D V_{DG}\widetilde{d}}{L_3} \tag{30}$$

$$\dot{\widetilde{x}}_4 = \frac{\widetilde{x}_1}{C_1} - \frac{\widetilde{x}_2 D}{C_1} - \frac{D^3 V_{GD}\widetilde{d}}{C_1 R} \tag{31}$$

$$\dot{\widetilde{x}}_5 = \frac{\widetilde{x}_2}{C_2} - \frac{\widetilde{x}_3 D}{C_2} - \frac{D^2 V_{GD}\widetilde{d}}{C_2 R} \tag{32}$$

$$\dot{\widetilde{x}}_6 = \frac{\widetilde{x}_2}{C_3} + \frac{\widetilde{x}_3(1-D)}{C_3} - \frac{\widetilde{x}_6}{C_3 R} - \frac{D^2 V_{GD}\widetilde{d}}{C_3 R} \tag{33}$$

This is a typical technique for linearizing at the operating point in DC/DC converters, known as the small-signal model, and can be expressed in the form $\dot{\widetilde{x}} = A\widetilde{x} + B\widetilde{u}$.

$$\begin{bmatrix} \dot{\widetilde{x}}_1 \\ \dot{\widetilde{x}}_2 \\ \dot{\widetilde{x}}_3 \\ \dot{\widetilde{x}}_4 \\ \dot{\widetilde{x}}_5 \\ \dot{\widetilde{x}}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{D}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{D}{L_3} & -\frac{(1-D)}{L_3} \\ \frac{1}{C_1} & -\frac{D}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & -\frac{D}{C_2} & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & \frac{(1-D)}{C_3} & 0 & 0 & -\frac{1}{C_3 R} \end{bmatrix} \begin{bmatrix} \widetilde{x}_1 \\ \widetilde{x}_2 \\ \widetilde{x}_3 \\ \widetilde{x}_4 \\ \widetilde{x}_5 \\ \widetilde{x}_6 \end{bmatrix} + \tag{34}$$

$$\begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{V_{DG}}{L_2} \\ 0 & -\frac{D V_{DG}}{L_3} \\ 0 & -\frac{D^3 V_{DG}}{C_1 R} \\ 0 & -\frac{D^2 V_{DG}}{C_2 R} \\ 0 & -\frac{D^2 V_{DG}}{C_3 R} \end{bmatrix} \begin{bmatrix} \widetilde{v}_{DG} \\ \widetilde{d} \end{bmatrix} \tag{35}$$

C. Model Validation

The Quadratic Buck converter with R^2P^2 was designed considering the PV panels and the rectified grid voltage, which is approximately 120 V. Table II describes the design parameters and devices used to perform a validation analysis between the switching model and an average model.

TABLE II
DESIGN PARAMETERS

Symbol	*Parameter*	*Value*
V_{DG}	*Input voltage*	120 V
P_o	*Ouput power*	325 W
V_o	*Ouput voltage*	48 V
I_o	*Ouput current*	6.78 A
f_s	*Switching frequency*	50 kHz
L_1, L_2, L_3	*Inductors*	66 μH, 1.35 mH, 1.12 mH
C_1, C_2, C_3	*Capacitors*	10 μF
D	*Duty ratio*	63.3%
Q_1, Q_2	*Mosfet´s*	*C20N60CFD*
S_1, S_2	*Diodes*	*TO-220-L*

Model validation is carried out by comparing the response of the switching model and the averaged model. This comparison is supported by MATLAB and PowerSim software. Fig. 6 shows the voltage/current waveforms of the reactive elements of the proposed converter. The current in L_1 exhibits an oscillating response, caused by the switching frequency and the response of the LC filter. Therefore, it is not recommended to use this variable for control design. The validation of the obtained linear model in (35) was performed by analyzing the dynamic behavior of the system using the transfer function (36).

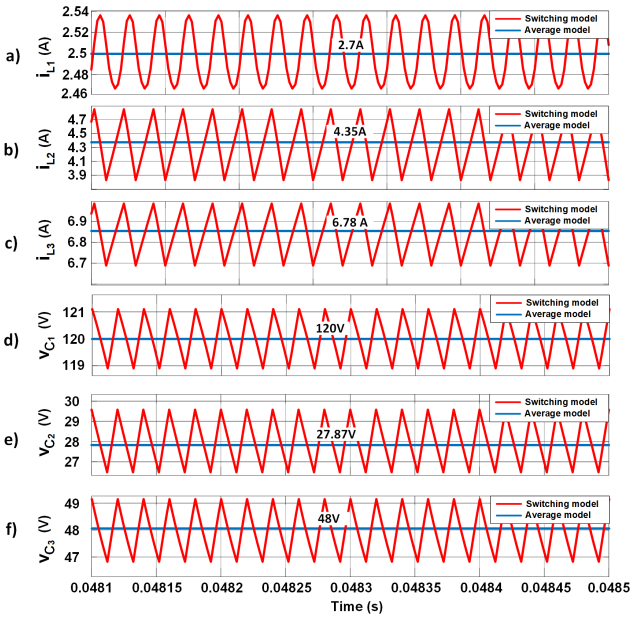

Fig. 6. Waveforms of current and voltage for the average model and the switching model: (a) current in inductor i_{L1}, (b) current in inductor i_{L2}, (c) current in inductor i_{L3}, (d) voltage on capacitor v_{C1}, (e) voltage on capacitor v_{C2} and (f) voltage on capacitor v_{C6}.

$$\frac{\widetilde{V}_{C_3}(s)}{\widetilde{d}(s)} = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (36)$$

The transfer function is related to the output voltage and duty ratio. Table III shows the values of the coefficients of (36).

TABLE III
TRANSFER FUNCTION COEFFICIENTS

Numerator	Denominator
a_5= *-6.584*$\times 10^5$	b_5= *1.299*$\times 10^4$
a_4= *4.385*$\times 10^{10}$	b_4= *7.934*$\times 10^9$
a_3= *- 4.368*$\times 10^{15}$	b_3= *1.0194*$\times 10^{14}$
a_2= *1.051*$\times 10^{20}$	b_2= *1.517*$\times 10^{18}$
a_1= *-1.861*$\times 10^{23}$	b_1= *1.117*$\times 10^{22}$
a_0= *8.607*$\times 10^{27}$	b_0= *4.972*$\times 10^{25}$

The frequency response of the transfer function (36) was obtained and compared with the frequency response of the switched model using the PowerSIM simulator, as shown in Fig. 7. The Quadratic Buck converter with R^2P^2 is a sixth-order system that exhibits non-minimum phase dynamics, as shown in the pole/zero pattern of the transfer function in Fig. 8. Hence, it is important to select a controller that ensures adequate voltage regulation at the output.

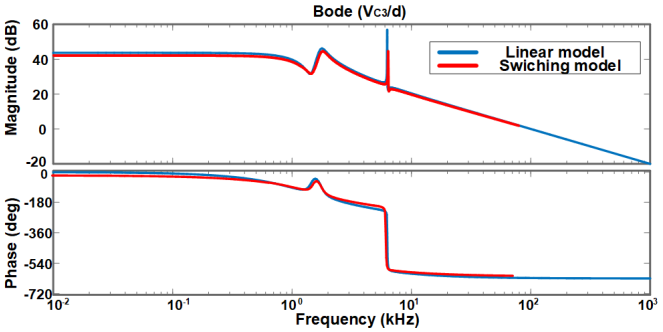

Fig. 7. Frequency response of the linear model and the switching model.

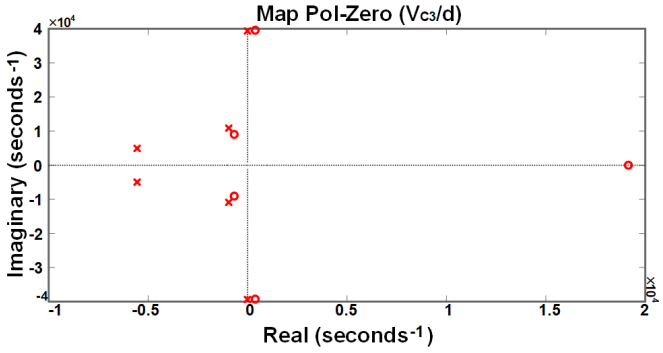

Fig. 8. Mapping of poles and zeros of the transfer function (36).

III. CONTROLLER DESIGN

The control design of high-order DC/DC converters, such as the Quadratic Buck converter with R^2P^2, presents challenges due to the system's complexity and dynamics. Selecting the appropriate controller is crucial to ensuring stability, improving dynamic performance, and maintaining adequate output

voltage regulation. To ensure adequate regulation at the system output, a closed-loop scheme based on a type III compensator with an extra pole at the origin is proposed (Fig. 9), aimed at improving the system ability to follow reference signals and reject low-frequency disturbances. This is especially crucial in microgrids, where it is important to maintain a regulated voltage despite load variations.

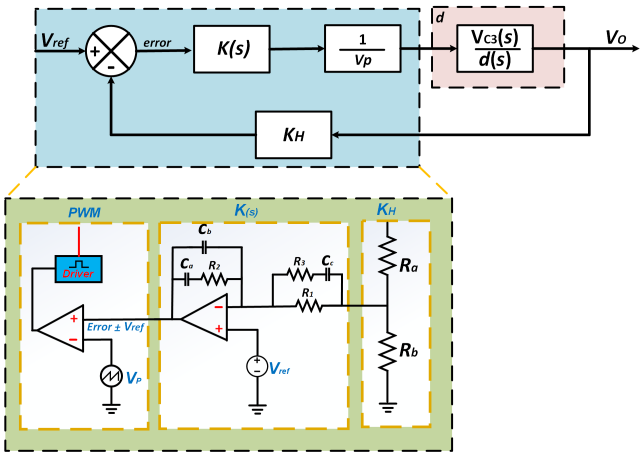

Fig. 9. Control scheme for output voltage regulation based on a type III compensator.

Based on Fig. 9, K_H is the sensor gain, $K(s)$ is the proposed controller, and V_p is the peak voltage of the triangular signal. Equation (37) presents the transfer function of the type III compensator [29].

$$K(s) = \frac{K\left[\frac{s}{w_z}+1\right]^2}{s\left[\frac{s}{w_p}+1\right]^2} \tag{37}$$

where the location of the zeros, the poles and the constant gain K are given by:

$$w_z = \frac{1}{C_b R_2} = \frac{1}{C_c(R_1+R_3)} \tag{38}$$

$$w_p = \frac{1}{C_{ab} R_2} = \frac{1}{C_c R_3} \tag{39}$$

$$K = \frac{1}{R_1(C_a+C_b)} \tag{40}$$

The proposed controller contains three poles and two zeros. With the use of the type III compensator, a zero steady state error is guaranteed. Additionally, the two zeros and two poles allow for precise phase margin adjustment, enhancing the system's ability to reject high-frequency disturbances effectively [29]. In [30], the methodology for obtaining the phase-specific contribution of the controller is presented. Equation (41), determines the maximum phase occurring at the geometric mean ω_m of ω_z and ω_p.

$$\phi_v(\omega_m) = 2tan^{-1}\frac{\omega_p-\omega_z}{2\sqrt{\omega_p\omega_z}} \tag{41}$$

The objective of the controller is to compensate for the phase of the natural dynamics of the converter. Therefore, the zeros were placed at a frequency of 500 Hz and the poles at 5 kHz to ensure the maximum phase contribution of the controller between the first complex pole pairs. The controller gain is proposed to be $K = 215$, so that the loop gain at the position of the resonant peak caused by the second pair of complex poles equals 0. A reference voltage of $V_{ref} = 3\ V$ and a regulated output of $V_o = 48\ V$ were selected. Based on this, the values for the voltage divider used to sense the output were set to $R_b = 7.5\ k\Omega$ and $R_a = 500\ \Omega$. Table IV presents the values of the elements that constitute the controller.

TABLE IV
TYPE III COMPENSATOR PARAMETERS

Symbol	*Parameter*	*Value*
R_a	*Sensing resistance*	500 Ω
R_b	*Sensing resistance*	7.5 Ω
R_1	*Compensator resistancer*	10 kΩ
R_2	*Compensator resistance*	762 Ω
R_3	*Compensator resistance*	1.1 kΩ
C_a	*Compensator capacitor*	46 nF
C_b	*Compensator capacitor*	417 nF
C_c	*Compensator capacitor*	29 nF

Fig. 10 shows the frequency response of the loop-gain, defined as the product of the controller and the plant. This loop-gain exhibits a gain margin of 9.41 dB and a phase margin of 71.2 degrees, ensuring closed-loop stability. Additionally, the frequency response of controller is shown. The Nyquist diagram of the loop gain is shown in Fig. 11. According to the Nyquist criterion, since the contour does not encircle the critical point $(-1, 0)$, the closed-loop system is stable.

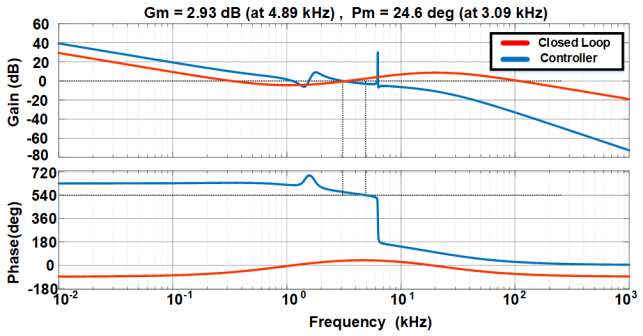

Fig. 10. Frequency response of the loop-gain and controller.

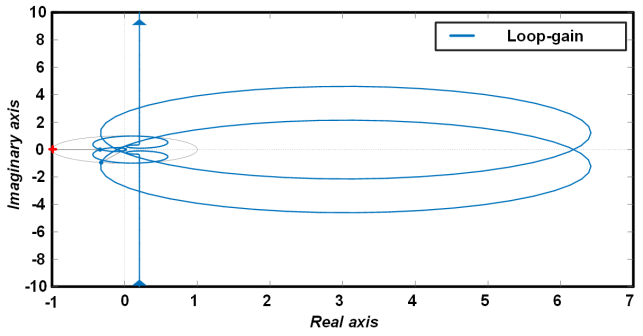

Fig. 11. Nyquist diagram of the loop-gain.

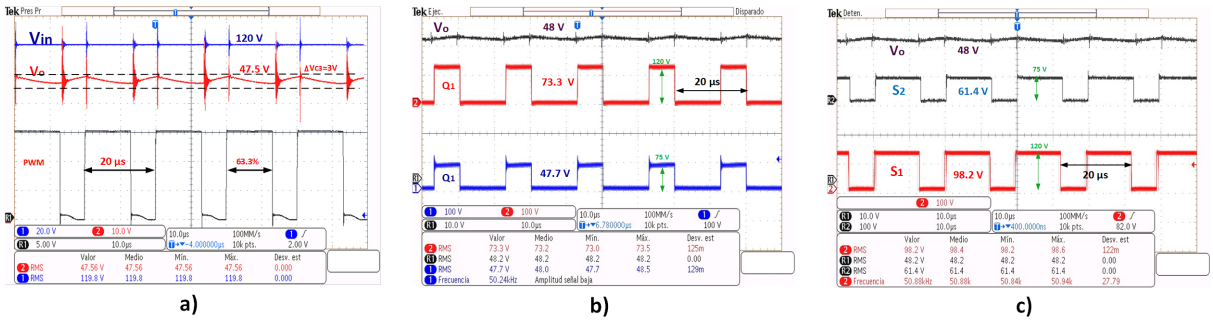

Fig. 12. Voltage waveforms on the converter, a) input/output voltages in comparison with the duty ratio, b) mosfets voltages in comparison with output voltage, and c) diodes voltages in comparison with output voltage.

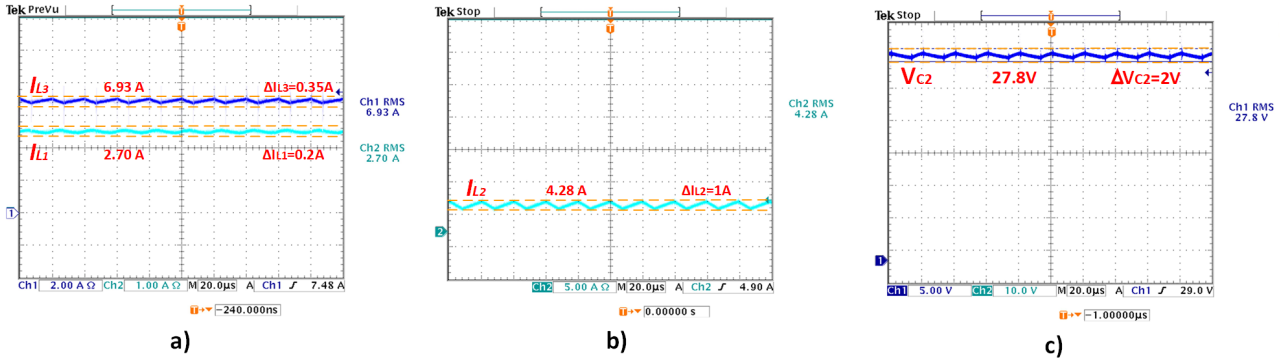

Fig. 13. Voltage/current waveforms on the reactive elements of the converter, a) current in inductors L_1 and L_3, b) current in inductor L_2, and c) voltage on capacitor C_2.

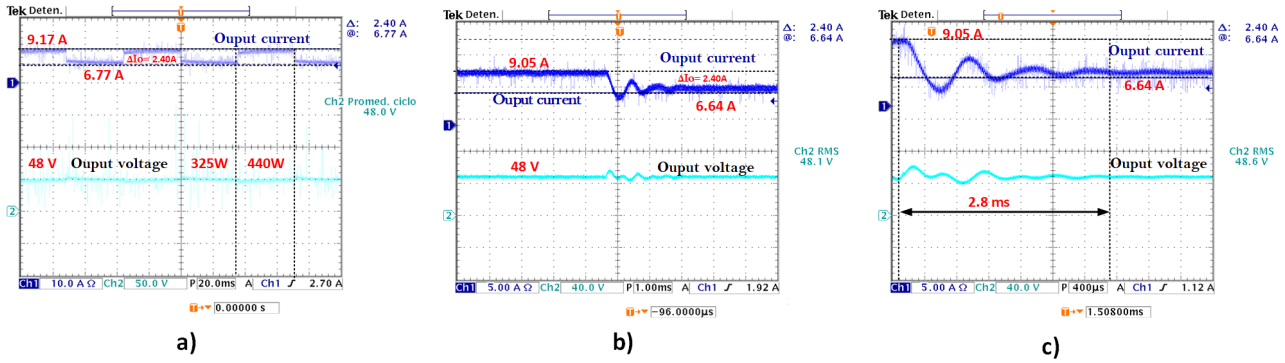

Fig. 14. Closed-loop converter output voltage/current waveforms, a) load change from 6.77 A to 9.17 A, b) dynamic response of output voltage to load variation, and c) output voltage stabilization time at 48 V during load changes.

IV. Experimental Results

To validate the simulation results and compare the efficiency of the system in open-loop and closed-loop configurations, a functional prototype of the Quadratic Buck converter with R^2P^2 was built. Fig. 15 shows the functional prototype, which includes the filter stage, the converter, and the control system. It was designed to operate at 325 W, using the parameters listed in Table II. Fig. 12 a) shows the input and output voltage waveforms of the converter, as well as the duty ratio that allows for the determination of the converter quadratic gain. Fig. 12 b) and c) show the voltages at the switches.

Fig. 13 shows the voltage and current waveforms in the open-loop converter to analyze the ripples proposed in Equa-

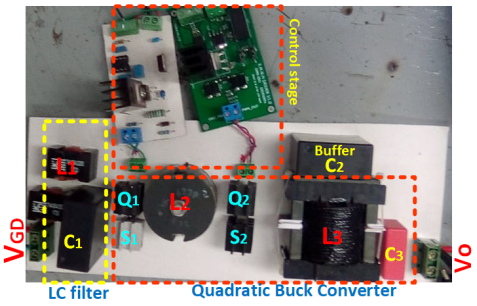

Fig. 15. Prototype of the Quadratic Buck converter with R^2P^2.

tions (8-13). Fig. 13 a) and b) shows the current waveforms for inductors L_1, L_2 and L_3. These currents in the averaged model are similar to the input and output currents of the system. The current ripple for inductor L_1 is $0.2\ A$, in L_2 it is $1\ A$ and in L_3 it is $0.35\ A$. The current ripple at L_2 is designed high because it has no impact on the input and output of the system and thereby improving the power density by reducing the inductor size. Fig. 13 c) shows the voltage across C_2, which serves to process the redundant power in the proposed converter. The voltage stress on C_2 is $27.8\ V$ with a ripple of $2\ V$. The controller was designed to regulate the output voltage to $48\ V$ and operate at a nominal power of $325\ W$. To verify the functionality of the designed controller, the system was subjected to a load change from $6.77\ A$ to $9.17\ A$. The system increased its power by $35\ \%$ relative to the nominal power, as shown in the Fig. 14 a). The Type III controller demonstrated robustness and functionality for controlling high-order systems with complex dynamics, such as the Quadratic Buck converter with reduced redundant power processing. Fig. 14 b) shows the converter load change from $9.05\ A$ to $6.64\ A$ with sampling times of $1\ ms$ and Fig. 14 c) shows that the voltage loop takes $2.4\ ms$ to regulate the output during the load change.

A. *Eficience Analysis*

To evaluate the efficiency of the quadratic Buck converter with R^2P^2, experiments were conducted in both open-loop and closed-loop configurations. In the open-loop case, it was observed that the efficiency depending on the load conditions and the characteristics of the components used. The power conversion efficiency in open loop was $92.38\ \%$ to $94.05\ \%$ at different power ranges (Fig.16).

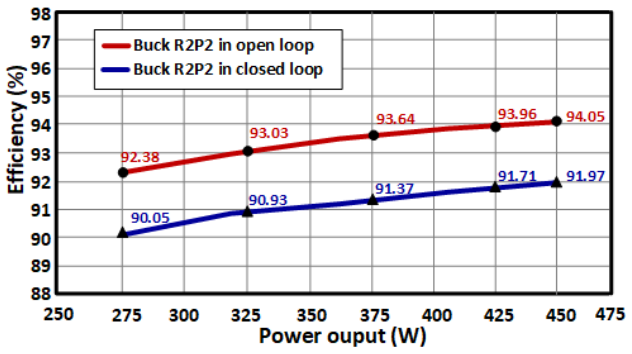

Fig. 16. Efficiency of the Quadratic Buck converter with R^2P^2 in open loop and closed loop.

On the other hand, implementing the converter in closed-loop with a Type III compensator impacted its efficiency. Experimental results showed an average efficiency reduction of $2.3\ \%$ compared to the open-loop configuration, with maximum efficiencies reaching up to $91.97\ \%$. This reduction is attributed to the control requirements for maintaining a constant output voltage of $48\ V$, which dynamically affects the converter's operating parameters and increases power losses in the semiconductor devices as they continuously adjust to stabilize the load. Fig. 17 shows the percentage of overall losses of the converter, being the inductors and transistors, where there is greater power loss. The loss analysis was carried out at the rated power of $325\ W$, where an efficiency of $93.03\ \%$ was obtained.

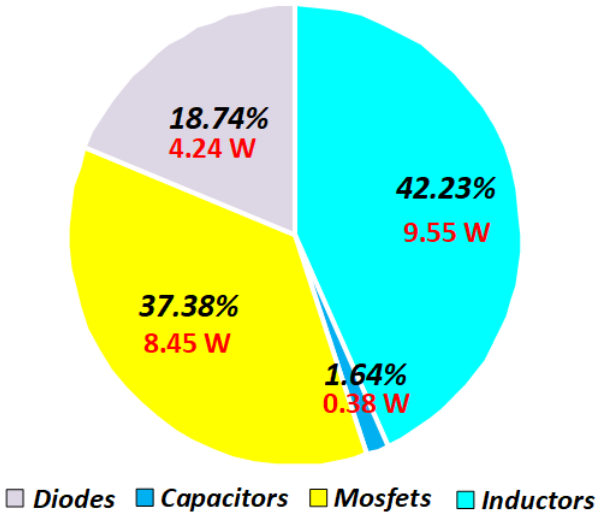

Fig. 17. Analysis of power losses in the converter elements.

V. Final Comments

This article has demonstrated the effectiveness and feasibility of the Quadratic Buck converter with Reduced Redundant Power Processing applied to a residential DC microgrid. The obtained experimental results validate the proposed design, showing significant improvements in system efficiency and stability. The use of the Type III compensator has been crucial in mitigating load variations and ensuring stable and reliable operation, despite being a non-minimum phase system. One of the disadvantages of the control scheme proposed in this work is that it does not protect the converter against over-currents. However, there are strategies, such as the LC filters for transient overcurrents already available in this structure, or a passive current limiter, such as a negative temperature coefficient (NTC) thermistor, which will be analyzed in future works. The VA model was presented to analyze the reduced redundant power processing. The VA modeling allows selecting an appropriate operating point where the system can improve power processing with the help of the k factor without affecting efficiency. Additionally, the linear model was presented, enabling the development of control strategies according to load requirements. The proposal to integrate a Quadratic Buck converter with R^2P^2 aimed to improve efficiency and energy management in DC microgrids, highlighting its potential for future applications in distributed generation systems. In future work, an analysis of the controller's performance will be developed, as well as the comparison of other regulation strategies to offer multiple options for implementation. In addition, a stability analysis when several converters are interconnected to a single closed-loop DC bus.

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Iván Alfonso Reyes Portillo received the degree of Electromechanical Engineer from the Instituto Tecnológico Superior de San Andrés Tuxtla, San Andrés Tuxtla, Veracruz, México in 2016 and the degree of Master of Science in Electronic Engineering from the Centro Nacional de Investigacion Y Desarrollo Tecnológico, Cuernavaca, Morelos, México in 2019. Obtained a Ph.D. in Electrical Engineering from the Universidad Autónoma de San Luis Potosí, San Luis Potosí, México, in 2024. He is currently a professor at Universidad Politécnica de San Luis Potosí in the Academy of Engineering in Systems and Industrial Technologies. His main areas of interest are DC/DC converters, redundant power processing converters, energy storage and renewable energies.

Saúl Rolando Mendez Elizondo received the degree of Biomedical Engineer and the degree of Master´s in Electrical Engineering from the Universidad Autónoma de San Luis Potosi, San Luis Potosí, Mexico, in 2017 and 2020, respectively. He is currently a PhD. student in Electrical Engineering at the Autonomous University of San Luis Potosí.His main areas of interest are DC/DC converters, study of stability in DC microgrids, energy storage and controller design for power electronic systems.

Jorge Alberto Morales Saldaña received the degree of Electrical Engineer and the degrees of Master´s and Ph.D. degrees in Electrical Engineering from the Universidad Autónoma de San Luis Potosi, San Luis Potosí, Mexico, in 1995, 1997 and 1999, respectively. He currently works at the Faculty of Engineering of the same University as a Research Professor. His main areas of interest are the development of high-efficiency switching converters, DC/DC conversion systems and control engineering applied to power electronic systems.

Claudia Angelica Rivera Romero a Computer Engineer graduated from the Universidad Autónoma de Zacatecas in 2006. She obtained her Master's degree in Electrical Engineering from the Universidad de Guanajuato in 2012. She obtained her PhD degree in Electrical Engineering from Universidad Autónoma de San Luis Potosí in 2021. She is currently an associate researcher at the Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), México. Her areas of interest are digital image processing, machine learning and power electronics.

Dora Luz Castro López received the B.S. degree in mechanical engineering from the Universidad Autónoma de Zacatecas (UAZ), Zacatecas, in 2011, and the master's and Ph.D. degrees in mechanical engineering from the Universidad Autónoma de San Luis Potosí (UASLP), San Luis Potosí, México, in 2014 and 2021, respectively. She is currently a professor at Universidad Politécnica de San Luis Potosí in the Academy of Engineering in Systems and Industrial Technologies. His research interests focus on heat transfer in biomedical systems and fluid mechanics applications. In addition, she is interested in the study of heat transfer and thermal design of power electronics systems.