High Step-up DC-DC Converter with Reconfiguration Capability

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***Abstract*—In this paper a high step-up DC-DC converter is proposed with reconfiguration capability that can operate safely without redundancy even if one of its power electronic switches fails. The proposed converter topology provides reduce voltage stress, uniform current sharing among power electronic switches, common grounding features, and also reduces the power handled by the power electronic devices using alternate paths, thereby improves the converter overall efficiency. Further, the control technique used for the converter reduces the transients during the healthy and fault operations. A fuse-MOSFET pair has been used to protect the converter from short-circuit faults. The proposed converter characteristic is analyzed in the continuous current mode (CCM), and its features are discussed in detail for both healthy and fault operation. The proposed converter was designed, fabricated and experimentally tested in a closed loop at 100 W to verify the operation and feasibility of the controller designed for both healthy and fault operation.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9070

***Index Terms*—Common grounding, high step-up converter, reduced voltage stress, uniform current sharing, reconfiguration capability.**

I. Introduction

DC-DC converters are used in handheld gadgets, household appliances, mobile phones, renewable energy systems, electric vehicles, and also varies industrial applications. Many of these applications demand low power loss, high performance, and low cost [1],[2]. However, these converters face reliability challenges due to the failure of power switches, and passive components [3]. Moreover, repairing the converters used in solar photovoltaic systems and wind energy conversion systems is costly and time consuming. Critical equipment used in applications like bio-medical, aerospace, and electric vehicle charging stations needs uninterrupted operation in the event of fault in the converter [4]. Therefore, it is essential to design DC-DC converters that can tolerate faults and deliver partial/full power to the load [5]. Many researchers in both academia and industry have been working on developing efficient and fault tolerant design techniques for high-gain DC-DC converters against power switch short circuit faults and open circuit faults. These faults can affect the performance and efficiency of the converters [6] over the time and may also cause the failure of other components in the converters, such as capacitors, inductors. A method for detecting capacitor faults is proposed to improve reliability of converter in [7]. Various fault tolerant high-gain DC-DC converters proposed for industrial applications contain more than one power switch to achieve high voltage gain, high power density, less voltage stress on components, and reduced size [8]-[15]. To make the converter fault tolerant, redundant components may be used, or the control structure needs to be modified. However, these redundant power switches increase the cost and complexity. A converter that uses a relay or controlled switch to bypass the fault module is proposed in [16]. Converter with an additional switch and TRIAC is connected in parallel to the main switch as a redundant component in [17]. Therefore, switching patterns are reconstructed using novel approaches during the post-fault condition. Converter that uses a phase shift modulation technique for interleaved 3-phase conventional boost DC-DC converters to bypass the fault switch in [18]. This configuration is robust to transients during current imbalance between phases, no additional sensors are required. However its limitations include a narrow focus on open-circuit faults, lower voltage gain, complex control circuit, and poor transient response. A fault-tolerant converter based on cascaded quasi-z sources was proposed in [19]. This converter uses relays to bypass the fault module, which is costly due to additional converter connected in cascade. During post-fault periods, switching patterns are reconfigured. Modular multi-level converter structures proposed in [20] require simple reconfiguration process compared to [19]. A DC-DC dual-switch converter to offer high reliability and work in both buck and boost modes was proposed in [21]. This topology offers reconfiguration capabilities during switch failures, however introduce new current paths that may increase stress on other converter components and voltage gain is not consistent in both healthy and fault operation. An open circuit fault diagnostic and fault tolerant three-level boost converter that uses an extra inductor and TRIAC for fault operation is proposed in [22]. This converter leverages output capacitor voltage and control parameters for achieving maximum power point tracking and employs an additional inductor and TRIAC to maintain half of its rated power delivery during fault. A DC-DC converter that uses several resonant switched-capacitor cells to form a voltage multiplier circuit can offer variable output voltage, with fault tolerance is proposed in [23]. This converter offers variable output voltage by means of redundant module to bypass the faulty components. But this converter produces double the input voltage, require more modules to obtain reference output voltage. Interleaved DC-

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DC converters with fault tolerant capabilities by adjusting multi-phase pule-width modulation control based on an open circuit fault detection algorithm were presented in [24]-[26]. These converters guarantee uninterrupted operation even under switch failure conditions, leveraging the redundancy provided by the additional switches. These converters produce low voltage gain, required more components, and suffers with electromagnetic interference. A highly efficient reconfigurable step-up DC-DC converter with fault tolerant capability was proposed in [27]. This converter produces less voltage gain, non-uniform distribution of current through switches, high input current ripple, less efficient, no common grounding feature and also increased voltage stress.

From the existing literature on fault tolerant DC-DC converters, five important observations have been made. Converter should have common grounding to increase their application range, high voltage gain in both operations without using any additional components, voltage stress should be less than output voltage in both healthy and fault operation, uniform distribution of current among power switches and lastly, reconfiguration time should be as less as possible for continuous power supply without interruption. To address these issues, a fault tolerant converter is proposed, modelled, and experimentally validated for continuous current mode operation in both healthy and fault operation. Experimental results presented demonstrate the superiority of the proposed converter with the existing fault tolerant DC-DC converter topologies reported in the literature.

II. Operation of Proposed Converter

The proposed topology is shown in Fig. 1 consists of two MOSFETs, two fuses, two inductors, three capacitors, and three diodes. This converter uses the voltage lift technique obtained from the combination of two p-type converters to offer high voltage gain, more efficiency, low input current ripple, reduced voltage stress among power switches, reconfiguration capability, and decreases redundancy time. Furthermore, this converter has continuous input current, uniform current flow through switch, fault detection using capacitor voltage compare to voltage across switches and a common grounding which aid in alleviating current stress on the source and electromagnetic interference/leakage current, respectively. This converter is analysed by neglecting the parasitic of capacitors and inductors, capacitance is large enough to maintain constant voltage in one switching cycle, power switches and diodes are ideal, and continuous current mode of operation.

A. Healthy Operation of Proposed Converter:

During normal operation converter operates in two modes in one switching cycle.

1) Mode-1(0 - DT_S): During mode-1, converter switches S_{w1} & S_{w2} and the diode D_2 are turned ON, while the diodes D_1& D_3 are turned OFF. Fig. 2 depicts the Current path in normal operation when switches are ON. The voltage across the inductors (L_1 & L_2) becomes positive and equal to input voltage. Simultaneously, Capacitors C_1 and C_2 discharge

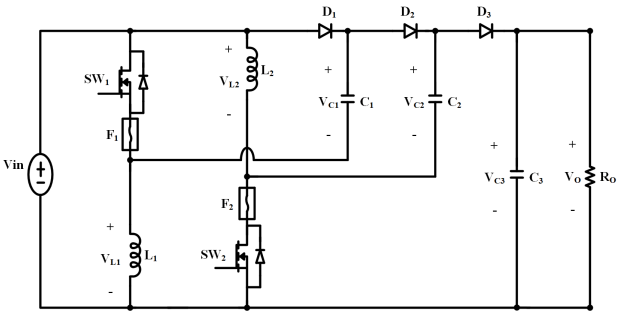


Fig. 1. Proposed converter topology.

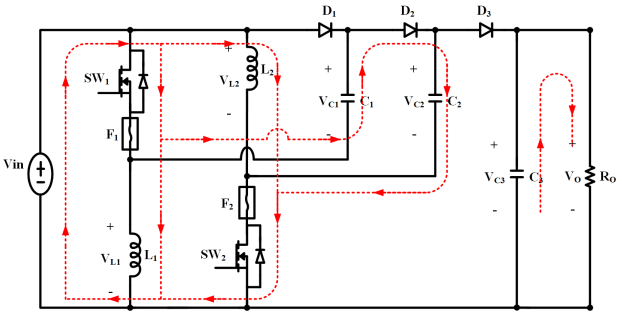


Fig. 2. Current path in normal operation when switches are ON (mode-1).

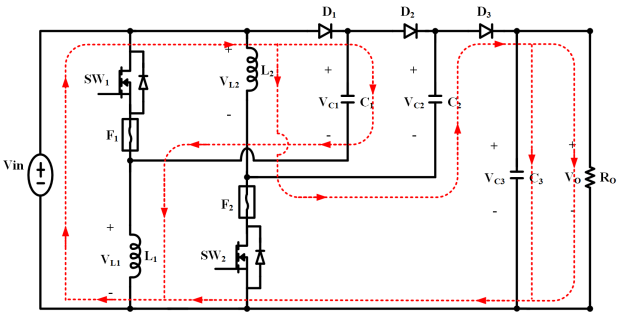


Fig. 3. Current path in normal operation when switches are OFF (mode-2).

and charge in combination to match the input voltage, while capacitor C_3 releases its stored energy to the load. By applying Kirchhoff's voltage law gives

$$\begin{cases} V_{L1} = V_{C2} - V_{C1} = V_{in} \\ V_{L2} = V_{in}, V_O = V_{C3} \end{cases} \quad (1)$$

2) Mode-2(DT_S - T_S): During mode-2, switches S_{w1} & S_{w2} and the diode D_2 are turned OFF, while the diodes D_1& D_3 are turned ON. Fig. 3 depicts the current path in normal operation when switches are OFF. The L_1 & C_1 are connected in series, and also L_2, C_2 & C_3 are connected in series, which is equal to the input voltage. According to the converter operation key, operating waveforms of proposed converter under healthy operation are shown in Fig. 4. By utilizing Kirchhoff's voltage law gives

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_{L2} = V_{in} + V_{C2} - V_{C3} \\ V_O = V_{C3} \end{cases} \quad (2)$$

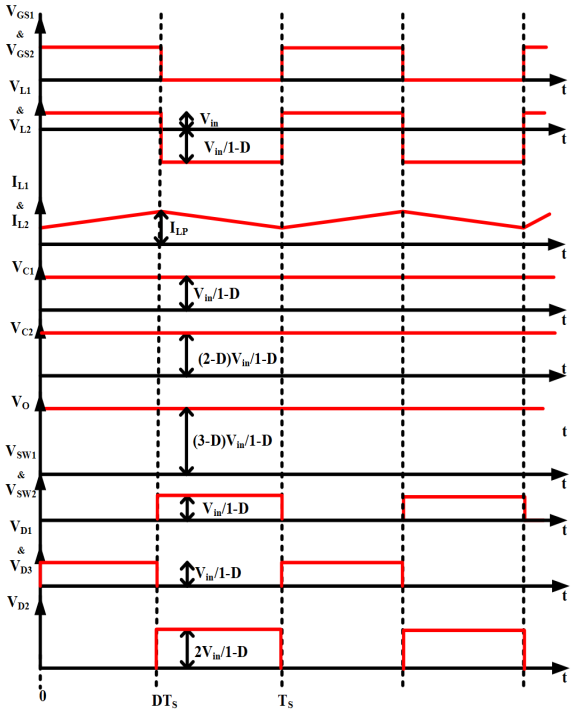


Fig. 4. Operating waveforms of proposed converter during healthy operation.

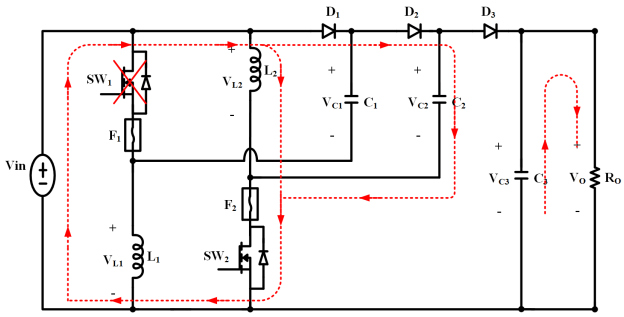


Fig. 5. Current path in mode-1 operation when switch S_{w1} is faulty

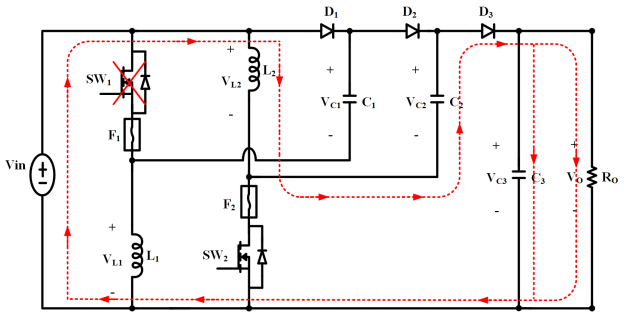


Fig. 6. Current path in mode-2 operation when switch S_{w1} is faulty.

B. Fault Operation of Proposed Converter:

Reconfiguration technique improve the reliability of the converter and its control by detecting and mitigating faults in real-time. In the event of a short circuit fault, the fuse is used to isolate the fault from rest of the circuit. The reconfigurable feature of the fault tolerant converter enables it to function even with one switch. However, when the converter is reconfigured, its characteristics are also modified. The fault tolerant operation of the converter under all possible cases are discussed in detail below.

1) Case-1: Switch S_{w1} is Faulty & Switch S_{w2} is Healthy: In this case, the converter operates in two modes in one switching cycle.

i) Mode-1(0-DT_S): During mode-1, switch S_{w2} and the diode D_2, D_1 are turned ON, while the diode D_3 is turned OFF. Fig. 5 depicts the Current path in mode-1 operation when Switch S_{w1} is faulty. The voltage across the inductor (L_2) becomes positive and equal to the input voltage (V_{in}). while capacitor C_2 is charged to match the input voltage. The energy contained in capacitor C_3 is simultaneously released to the load, and small amount current flow through L_1 and C_1 which can be neglected. By utilizing Kirchhoff's voltage law gives

$$\begin{cases} V_{L2} = V_{in} \\ V_{C2} = V_{in} \\ V_O = V_{C3} \end{cases} \tag{3}$$

ii) Mode-2(DT_S-T_S): During mode-2 operation, the switch S_{w2} and the diode D_2, D_1 are turned OFF, while the diode D_3 is turned ON. Fig. 6 depicts the Current path in mode-2 operation when Switch S_{w1} is faulty. The input voltage, L_2, and C_2 are series connected to transfer the stored energies to C_3 and the load. By utilizing Kirchhoff's voltage law gives

$$\begin{cases} V_{L2} = V_{in} + V_{C2} - V_{C3} \\ V_O = V_{C3} \end{cases} \tag{4}$$

2) Case-2: Switch S_{w1} is Healthy & Switch S_{w2} is Faulty: In this case, the converter operates in two modes in one switching cycle.

i) Mode-1(0-DT_S): During mode-1, switch S_{w1} and the diodes D_3, D_2 are turned ON, while the diode D_1 is turned OFF. Fig. 7 depicts the Current path in mode-1 operation when Switch S_{w2} is faulty. The voltage across the inductor (L_1) becomes positive and equal to the input voltage. The energy contained in capacitor C_1 is discharged to C_3 and load. Very small amount of leakage current flow through L_2 and C_2 which can be neglected. By utilizing Kirchhoff's voltage law gives

$$\begin{cases} V_{L1} = V_{in}, V_{C1} = V_O - V_{in} \\ V_O = V_{C3} \end{cases} \tag{5}$$

ii) Mode-2(DT_S-T_S): During mode-2, switch S_{w1} and the diodes D_3, D_2 are turned OFF, while the diode D_1 is turned ON. Fig. 8 depicts the current path in mode-2 operation when Switch S_{w2} is faulty. The L_1 and C_1 are connected in series with input voltage, which discharges and charges, respectively. The energy contained in capacitor C_3 is simultaneously released to the load, and small amount of current flow through L_2 and C_2 which can be neglected. By applying Kirchhoff's voltage law gives

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_O = V_{C3} \end{cases} \tag{6}$$

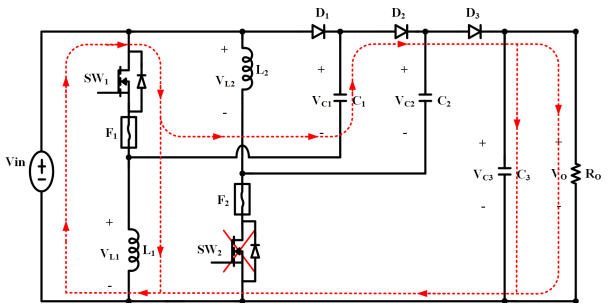


Fig. 7. Current path in mode-1 operation when switch S_{w2} is faulty.

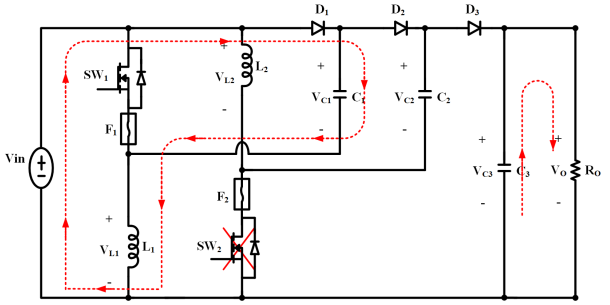


Fig. 8. Current path in mode-2 operation when switch S_{w2} is faulty.

C. Analysis of Proposed Converter in Continuous Current Mode:

This section details the proposed converter topology, voltage gain, inductor ripple current, and inductor design for continuous current mode operation.

1) Voltage Gain Under Healthy Operation: To obtain voltage gain for proposed converter, applying volt-sec balance across inductor L_1 and L_2.

$$\int_0^{DT_S} (V_{L1} + V_{L2}) + \int_{DT_S}^{T_S} (V_{L1} + V_{L2}) = 0 \tag{7}$$

Following equation can obtained by substituting inductor voltages from Eq. (1) and Eq. (2). we get

$$V_{C1} = \frac{V_{in}}{1-D}, \quad V_{C2} = \frac{V_{in}}{1-D} \quad + V_{in} \tag{8}$$

The voltage gain of converter in healthy operation is given as

$$M_{CCM}\,(Healty\ condition) = \left(\frac{V_O}{V_{in}}\right) = \frac{3-D}{1-D} \tag{9}$$

2) Voltage Gain Under Fault Operation:

i) Switch S_{w1} is Open Circuit: To obtain voltage gain for proposed converter in fault operation, applying volt-sec balance principle across inductor L_2.

$$\int_0^{DT_S} (V_{L2}) + \int_{DT_S}^{T_S} (V_{L2}) = 0 \tag{10}$$

Following equation can be obtained by substituting inductor voltages from Eq. (3) and Eq. (4). The voltage gain of proposed converter in fault operation is derived as

$$M_{CCM}\,(Fault\ condition) = \left(\frac{V_O}{V_{in}}\right) = \frac{2-D}{1-D} \tag{11}$$

ii) Switch S_{w2} is Open Circuit: To obtain voltage gain for proposed converter in fault operation, applying volt-sec balance principle across inductor L_1.

$$\int_0^{DT_S} (V_{L1}) + \int_{DT_S}^{T_S} (V_{L1}) = 0 \tag{12}$$

Following equation can be obtained by substituting inductor voltages from Eq. (5) and Eq. (6). The voltage gain of proposed converter in fault operation is derived as

$$M_{CCM}\,(Fault\ condition) = \left(\frac{V_O}{V_{in}}\right) = \frac{2-D}{1-D} \tag{13}$$

3) Calculation of Inductor Ripple Current: By assuming proposed converter is ideal

$$V_{in} I_{in} = V_O I_O \tag{14}$$

During normal operating modes of the proposed converter, the inductor current can be obtained as

$$I_L = \frac{I_O}{1-D} \tag{15}$$

From Eq. (1) inductor current can be written as

$$L\frac{di}{dt} = V_{in} \tag{16}$$

From above equation the peak-to-peak inductor ripple current can be obtained as

$$\Delta I_L = \frac{V_{in}}{L}\, DT_S \tag{17}$$

4) Calculation of Inductance: The required inductance value can be obtained from Eq. (17) as

$$L = \frac{V_{in}}{\Delta I_L}\, DT_S \tag{18}$$

In terms of inductor average current, peak-to-peak current equals to

$$\Delta I_L = x\%\ of I_L \tag{19}$$

Where x is allowable percentage ripple.
By substituting average inductor current, the value of inductor can be obtained as

$$L = \frac{V_{in}\,(1-D)\,D}{x\% * I_O * F_s} \tag{20}$$

where F_s= Switching frequency of converter

III. Voltage Stress Across Active Devices

In any converter configuration voltage stress occurs when active device is OFF or reverse biased. Therefore, it is necessary to compute the voltage stress across various active devices of proposed converter.

A. Healthy Operation of Proposed Converter

In mode-1 operation diode D_1 and D_3 are reverse biased as shown in Fig. 2. The voltage across diodes $V_{D1} = V_{C1}$ & $V_{D3} = V_{C3} - V_{C2}$. In mode-2 operation switch S_{w1}, S_{w2} and D_2 is reverse bias as shown in Fig. 3. The voltage across switch $V_{Sw1} = V_{C1}$; $V_{Sw2} = V_{C3} - V_{C2}$; $V_{D2} = V_{C3} + V_{C1} - V_{C2}$. By substituting the capacitor voltages, the voltage stress in terms of duty cycle and input voltage for all active devices is summarised in Table I.

TABLE I
VOLTAGE STRESS UNDER HEALTHY CONDITION

Device	Voltage stress	Device	Voltage stress
S_{w1}	$\frac{V_{in}}{1-D}$	D_1,D_3	$\frac{V_{in}}{1-D}$
S_{w2}	$\frac{V_{in}}{1-D}$	D_2	$\frac{2V_{in}}{1-D}$

B. Fault Operation of Proposed Converter

1) When Switch S_{w1} is Faulty: In mode-1 operation diode D_3 is reversed biased as shown in Fig. 5. The voltage across $V_{D3} = V_{C3} - V_{C2}$. In mode-2 operation switch S_{w2} and D_2 is reverse bias as shown in Fig. 6. The voltage across $V_{Sw2} = V_{C3} - V_{C2}$ & $V_{D2} = V_{C3} - V_{C2}$. By substituting the capacitor voltages, the voltage stress in terms of duty cycle and input voltage for all active devices is summarised in Table II.

2) When Switch S_{w2} is Faulty: In mode-1 operation diode D_1 is reversed biased as shown in Fig. 7. The voltage across $V_{D1} = V_{C3} - V_{in}$. In mode-2 operation switch S_{w1} and D_3 is reverse bias as shown in Fig. 8. The voltage across $V_{Sw1} = V_{C3} - V_{C1}$ & $V_{D3} = V_{C3} - V_{C1}$ .By substituting the capacitor voltages, the voltage stress in terms of duty cycle and input voltage can be obtained for all devices is summarised in Table II.

TABLE II
VOLTAGE STRESS UNDER FAULT CONDITION

Switch S_{w1} fault		Switch S_{w2} fault	
Device	**Voltage stress**	**Device**	**Voltage stress**
S_{w2}	$\frac{V_{in}}{1-D}$	S_{w1}	$\frac{V_{in}}{1-D}$
D_2,D_3	$\frac{V_{in}}{1-D}$	D_1,D_3	$\frac{V_{in}}{1-D}$

IV. CALCULATION OF FUSE RATING

Fuses are connected in series with power switches as shown in Fig. 1. Table III gives the equation for calculation of fuse melting integral for various input current waveforms of switches.

TABLE III
FUSE MELTING INTEGRAL VALUES

Waveform type	Equation
Triangular	$I^2T_{Fuse} = \frac{1}{3}\left((I_{ma})^2\right) + I_{ma}I_{mb}(I_{mb})^2T)$
Square	$I^2T_{Fuse} = (I_{ma})^2T$
Trapezoidal	$I^2T_{Fuse} = \frac{1}{3}(I_{ma})^2T$

$I_{ma} = maximum\ current's\ rising\ edge$
$I_{mb} = maximum\ current's\ falling\ edge$

The current pulse cycle affects the fuse ability to withstand the fuse pulse rate. Therefore, the fuse pulse factor is needed to quantify the fuse resistance to high peaks in a short time. The following equation can be obtained from Table IV as

$$I^2T_{Fuse} = (I_{ma})^2T \tag{21}$$

Table IV shows the fuse pulse factor in relation to its nominal fuse melting value. The switching time period can be calculated from the designed switching frequency of 33 kHz as 30.303 µs. If the duty cycle of converter is 90 %, the ON-time of the switches can be calculated as

$$T_{on} = DT_S = 0.9 \times 30.303\mu s = 27.27\ \mu s \tag{22}$$

The total time of the switches is obtained by multiplying

TABLE IV
FUSE PULSE FACTOR

No. of Pulse	Ratio
100000	$I^2T_{Fuse} = 22\ \%\ of\ nominal\ melting$
10000	$I^2T_{Fuse} = 29\ \%\ of\ nominal\ melting$
1000	$I^2T_{Fuse} = 38\ \%\ of\ nominal\ melting$

10000 pulses with the ON-time as

$$T = T_{on} \times 10000 = 0.2727\ s \tag{23}$$

The fuse melting value is determined from the maximum input current of converter for two stages as

$$I^2T_{Fuse} = 21^2 \times 0.2727 = 120.269\ A^2s \tag{24}$$

The fuse nominal melting is found from Table-V, for 10000 pulses as

$$I^2T_{Nominalmelting} = 414.722\ A^2s \tag{25}$$

From Table-VI, the nearest suitable fuse rating is selected for nominal fuse melting value of 414.722 A^2s, is 12 A.

TABLE V
ELECTRICAL PARAMETER FOR FUSE

Voltage Rating (V)	Current Rating (A)	Nominal Melting $I^2T_{Fuse}\ (A^2 - s)$
250	8	198.16
250	10	217.635
250	15	607.135

V. MODELLING OF PROPOSED CONVERTER

The proposed converter dynamic is determined by its state variables. When the converter is switched ON and OFF, its passive components change and are referred to as state variables. Five state variables are investigated in order to understand the dynamics of the suggested converter. Which including two inductors current and three capacitor voltages. Eq. (26) and Eq. (27) represent the small-signal ac model for the proposed converter using state space averaging.

State equations for small-signal model in CCM are

TABLE VI
COMPARISON OF VARIOUS DC-DC CONVERTERS

Parameters \ References		[18]	[19]	[21]	[22]	[23] N=2	[25] N=2	[27]	Proposed
No. of elements		10	22	6	13	13	8	10	10
Redundancy replacement		No	Converter	Leg	Element	No	No	No	No
Reconfiguration capability		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Voltage gain (M_{CCM})	**Pre-fault**	$\frac{1}{1-D}$	$(\frac{1}{1-2D})^2$	$\frac{1}{1-D}$	$\frac{2}{1-D}$	(N+1)	$\frac{1+D}{1-D}$	$\frac{2}{1-D}$	$\frac{3-D}{1-D}$
	Post-fault	$\frac{1}{1-D}$	$\frac{1}{1-2D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$	(N)	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2-D}{1-D}$
Voltage stress (V_{sw}/V_o)	**Pre-fault**	1	0.5,1	1	0.5	0.5	$\frac{1}{1+D}$	0.5	$\frac{1}{3-D}$
	Post-fault	1	1	1	1	1	1	$1, \frac{1}{2-D}$	$\frac{1}{2-D}$
Efficiency (%)		94.56	91.23	96.2	95.11	93.65	95.1	95.5	96.5
Continuous source current		Yes	Yes	No	Yes	No	Yes	Yes	Yes
Common grounding		Yes	Yes	No	No	Yes	No	No	Yes

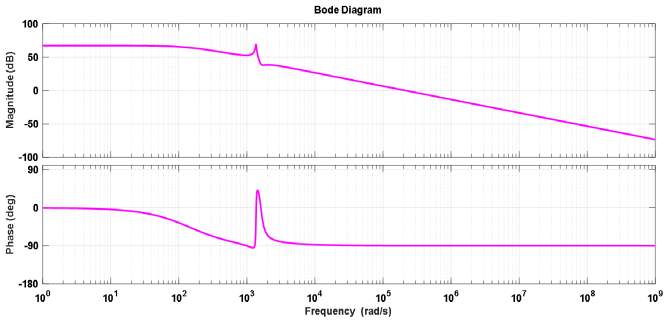


Fig. 9. Bode plot of the open-loop small-signal transfer function.

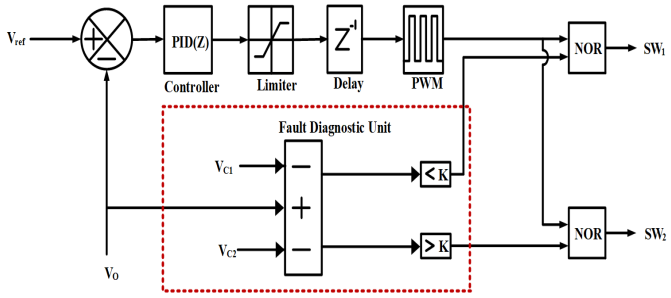


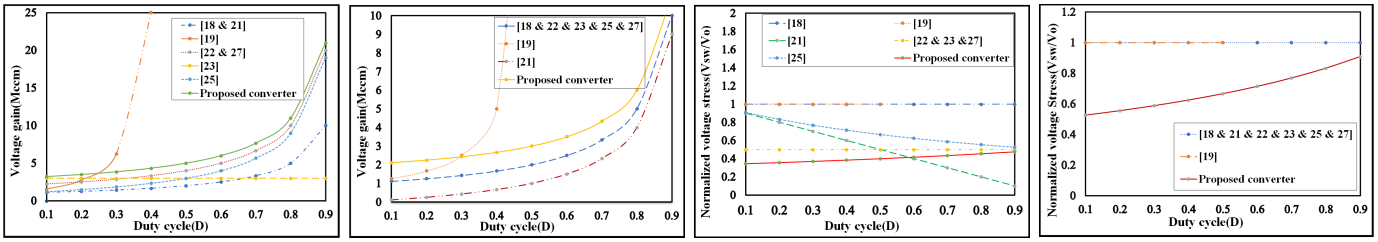
Fig. 10. Proposed converter control strategy.

$$\begin{pmatrix} \dot{\hat{I}}_{L1} \\ \dot{\hat{I}}_{L2} \\ \dot{\hat{V}}_{C1} \\ \dot{\hat{V}}_{C2} \\ \dot{\hat{V}}_{C3} \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{-(1-D)}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{(1-D)}{L_2} & \frac{-(1-D)}{L_2} \\ \frac{(1-2D)}{C_1} & \frac{-D}{C_1} & 0 & 0 & 0 \\ \frac{-D}{C_2} & \frac{-(1-2D)}{C_2} & 0 & 0 & 0 \\ \frac{(1-D)}{C_3} & 0 & 0 & 0 & \frac{-1}{R_O C_3} \end{pmatrix} \begin{pmatrix} \hat{I}_{L1} \\ \hat{I}_{L2} \\ \hat{V}_{C1} \\ \hat{V}_{C2} \\ \hat{V}_{C3} \end{pmatrix} + \begin{pmatrix} I_{L1}(\frac{2}{C_1} - \frac{1}{C_2} - \frac{1}{C_3}) \\ I_{L2}(\frac{2}{C_2} - \frac{2}{C_1}) \\ V_{C1}(\frac{1}{L_1}) \\ -V_{C2}(\frac{1}{L_2}) \\ V_{C3}(\frac{1}{L_2}) \end{pmatrix} \hat{d} \tag{26}$$

$$\left(\hat{V}_o\right) = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} \hat{I}_{L1} \\ \hat{I}_{L2} \\ \hat{V}_{C1} \\ \hat{V}_{C2} \\ \hat{V}_{C3} \end{pmatrix} + \begin{pmatrix} 0 \end{pmatrix} \left(\hat{d}\right) \tag{27}$$

Where all elements denoted by ($\wedge$) are small ac variation. To analyse the dynamic performance of the proposed converter, a small-signal frequency response test is performed. Fig. 9 shows the bode plot of the open-loop small-signal transfer function. As it was seen that the phase angle is about -90º when the magnitude goes to infinity. This confirms the stability of the proposed DC-DC converter topology. In order to stabilize the proposed converter in a closed loop, the voltage control technique is adopted. The control parameters are chosen in such a way that resultant system achieves required Gain-Margin and Phase-Margin.

Fig. 10 shows the closed-loop with PID controller and a fault-diagnostic unit. The output voltage is controlled in various operating scenarios by the controller. In the event of one switch fails, the controller modifies the other switch duty cycle to maintain the required output voltage. The fault detection unit does not identify a defect while the converter is operating normally and the output voltage is $V_O = V_{C1}+V_{C2}$. Once fault occur on any one of the switches, the controller prevents gate pulses to faulty switch by comparing both capacitor voltages (V_{C1} and V_{C2}) with output voltage. When losses are ignored, the sum of the capacitor voltages $V_{C1} = V_{in}$ and $V_{C2} = V_{in}$ is much less than V_O, indicating a failure on switch S_{w1}. The fault detection unit detects the defect and prevent gate pulses from switching S_{w1}. Similarly, when fault occur on switch S_{w2} sum of capacitor voltages $V_{C1} = \frac{V_{in}}{1-D}$ and $V_{C2} = \frac{V_{in}}{1-D}$ is much greater than V_O fault detection unit detect fault prevent gate pulses from switching S_{w2}.



(a) (b) (c) (d)

Fig. 11. (i). Voltage gain comparison (a). Healthy operation, (b). Fault operation (ii). Voltage stress comparison (c). Healthy operation, (d). Fault operation.

VI. Performance Comparison

The proposed DC-DC converter performance indices are compared with other fault tolerant converters reported in the literature and presented in Table VI. From Table VI, it is observed that [19],[21] and [22] require extra circuit components for re-configurable operation under faults. The converter reported in [18],[23],[25],[27] and the proposed fault tolerant converter can be reconfigured without need for extra circuit component. The proposed converter and converters reported in [21],[27] used fuses. When short circuit occur fuse will blow above the rated value of current and become open circuit fault in converter. The converter reported in [19] uses relays to bypass the faulty module by using switching pattern, which required a greater number of switches and converters reported in [18],[22],[25] deal with only open circuit faults doesn't uses fuse or relays. The proposed converter has high voltage gain, low voltage stress and, higher efficiency compares to remaining fault tolerant converter in healthy and fault operations. The proposed converter topology also has common grounding feature; hence it is also suitable for many applications which require lower electromagnetic interference and uniform distribution of current among power switches and inductors.

Fig. 11.(i) shows the graphical representation of voltage gain of the proposed converter with other fault tolerant converters. From Fig. 11.(i) it is observed that the voltage gain of proposed converter is higher at duty cycle in healthy & fault conditions, expect cascaded quasi-z source converter configurations. Fig. 11.(ii) shows the graphical comparison between the normalized voltage stress of switches and duty cycle for various fault tolerant converters in the CCM. From Fig. 11.(ii) it is observed that normalized voltage stress of switches is lower for the proposed converter at the same duty cycle in healthy and fault conditions.

VII. Experimental Validation

The proposed converter is fabricated and examined in order to evaluate its effectiveness under both healthy and fault dynamics. The DSP LAUNCHXL-F28379D processor is used to implement the control logic. The experimental results are obtained for continuous current mode. Fig. 12 shows the experimental prototype setup of proposed converter. The converter components used for experimentation are given in Table VII.

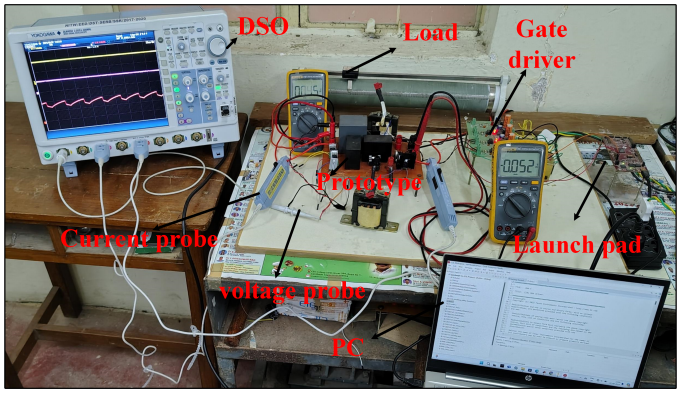


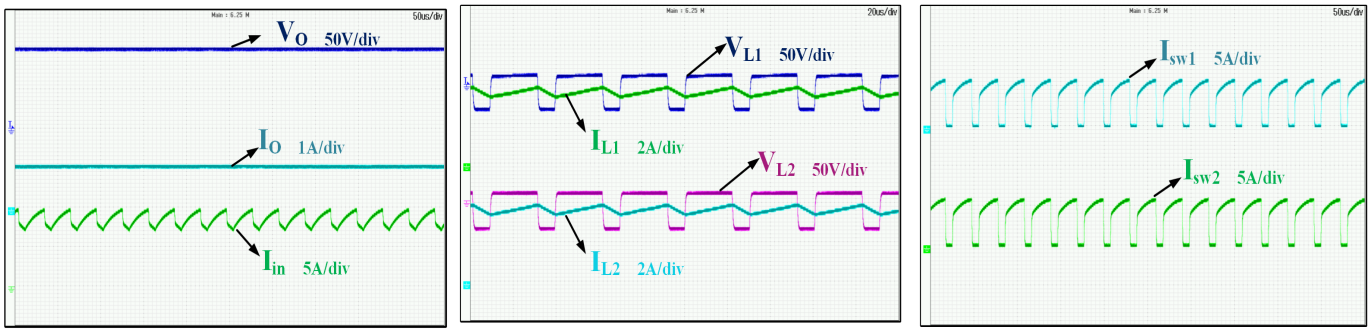
Fig. 12. Experimental setup prototype.

TABLE VII
Proposed Converter Specification

Component	Rating/Value
Input Voltage	12 V
Inductor L_1, L_2	0.5 mH
Capacitor C_1, C_2, C_O	100 µF,100 µF,100 µF
Load	100Ω
PID Controller Coefficients	K_P=0.018, K_I=1.5 K_D=1$*e^{-6}$, N_D=1000
Fuse	12 A (Fast acting fuse)
S_{w1} and S_{w2}	IRFP468PBF
D_1, D_2, and D_3	STPS60SM170C

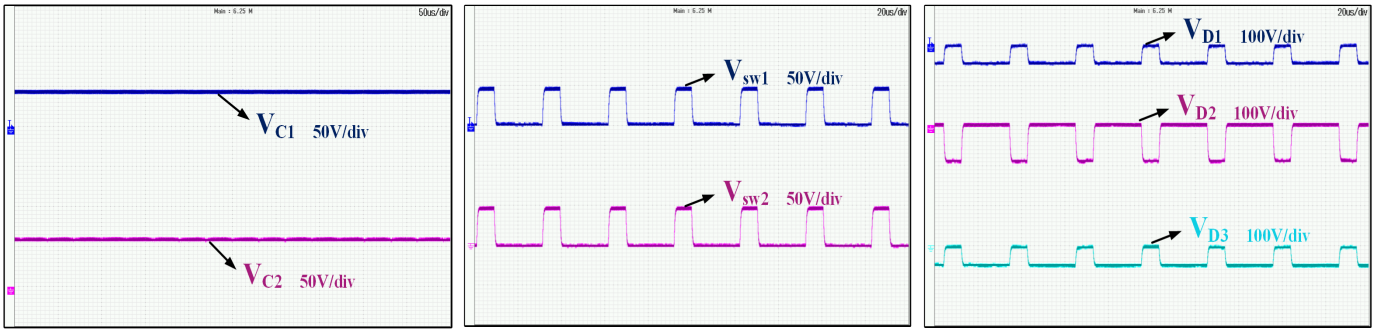
A. Normal Operation:

During normal operation, S_{w1} and S_{w2} switches are ON simultaneously. The waveforms of converter voltages are presented for voltage gain of M=8.33 which give an output power of 100 W at duty cycle of 0.73. The output voltage, output current and input current of proposed converter , is shown in Fig. 13.(a). The voltage and current of inductors L_1 and L_2 are depicted in Fig. 13.(b) & Fig. 13.(c) shows the switch currents. The voltage across the capacitors C_1 and C_2 are shown in Fig. 14.(a). The voltage stress across switches S_{w1} and S_{w2} is



(a) (b) (c)

Fig. 13. Experimental waveforms under normal operation (a). output voltage & current and input current (b). voltage and current in inductor-1 and inductor-2 (c). Current flowing in switch-1 and switch-2.



(a) (b) (c)

Fig. 14. Experimental waveforms under normal operation (a). voltage across capacitor-1 and capacitor-2 (b). voltage across switches (c). voltage across diodes.

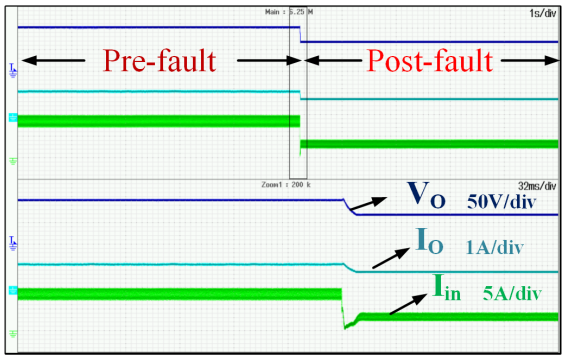


Fig. 15. Dynamic behaviour in open-loop (when switch S_{w1} is open-circuit).

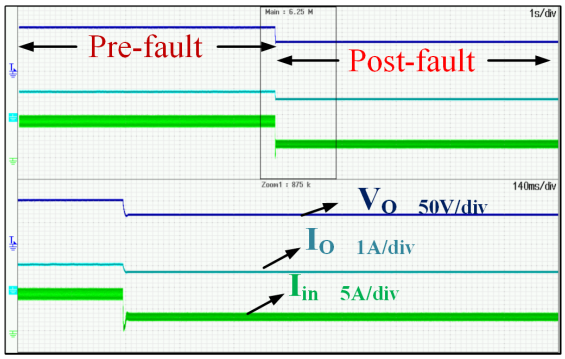


Fig. 16. Dynamic behaviour in open-loop (when switch S_{w2} is open-circuit).

presented in Fig. 14.(b) which is less than the output voltage and equal to V_{in}/(1-D). The voltage stress across diode D_1, D_2 and D_3 shown in Fig. 14.(c) which is equal to V_{in}/(1-D), $2V_{in}$/(1-D) & V_{in}/(1-D), respectively.

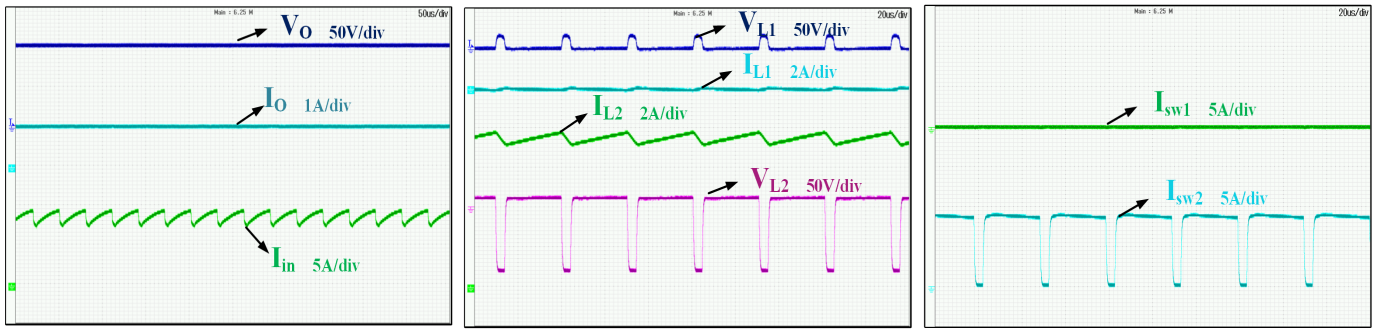
B. Dynamic Operation in Open-loop:

When switch S_{w1} is open circuit, no current flows through its drain-source terminals (V_{DS1}), then the converter is operated by switch S_{w2} only. The dynamic behaviour in open-loop operation of proposed converter from pre-fault to post-fault is shown in Fig. 15.

Similarly, when switch S_{w2} is open circuit, no current flows through its drain-source terminals (V_{DS2}), then the converter is operated by switch S_{w1} only. The dynamic behaviour in open-loop operation of proposed converter from pre-fault to post-fault is shown in Fig. 16.

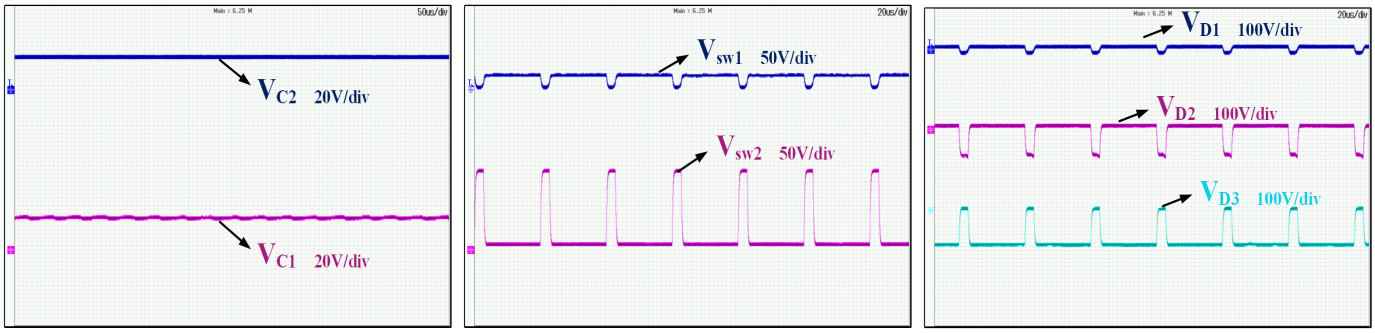
C. Fault Operation:

1) When Switch S_{w1} is Open Circuit: During fault operation, switch S_{w2} is in operation and switch S_{w1} has open circuit fault. In this case, waveforms of the proposed fault



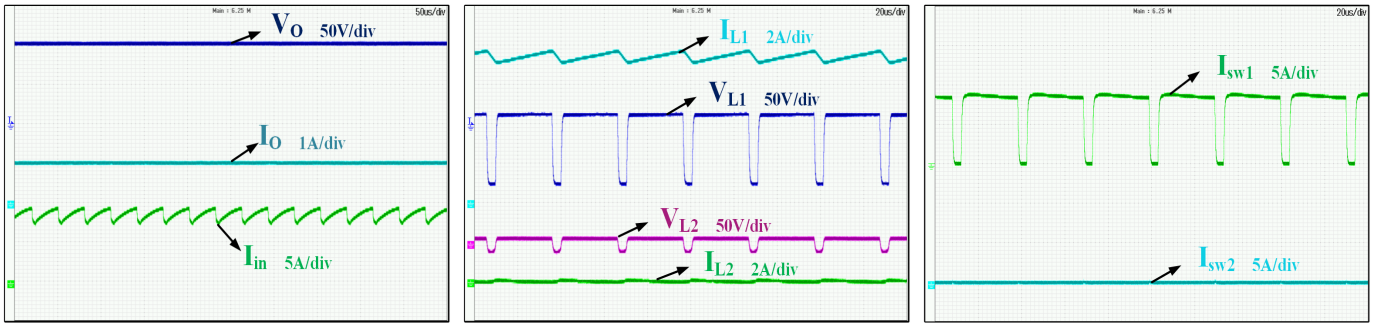
(a) (b) (c)

Fig. 17. Experimental waveforms when switch S_{w1} is open circuit (a). output voltage & current and input current (b). voltage and current in inductor-1 and inductor-2 (c). current flowing in switch-1 and switch-2.



(a) (b) (c)

Fig. 18. Experimental waveforms when switch S_{w1} is open circuit (a). voltage across capacitor-1 and capacitor-2 (b). voltage across switches (c). voltage across diodes.

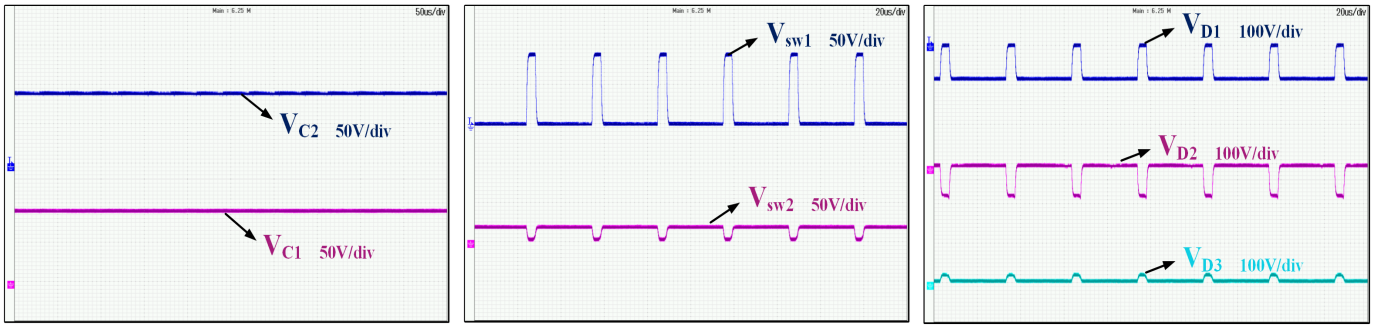


(a) (b) (c)

Fig. 19. Experimental waveforms when switch S_{w2} is open circuit (a). output voltage & current and input current (b). voltage and current in inductor-1 and inductor-2 (c). current flowing in switch-1 and switch-2.

tolerant converter voltages and currents are presented for step-up voltage gain of 8.33 for an output power of 100 W. The output voltage,output current and input voltage at duty cycle of 0.865 (86.5%) equals 100 V which is shown Fig. 17.(a). The voltage and current of inductors L_1 and L_2 are depicted in Fig. 17.(b) & Fig. 17.(c) shows the switch currents. The voltage across the capacitors C_1 and C_2 are shown in Fig. 18.(a). The voltage stress across switches S_{w1} and S_{w2} is presented in Fig. 18.(b) which is less than the output voltage and equal to V_o/(2-D). The diode voltage D_1, D_2, D_3 waveforms are shown in Fig. 18.(c).

2) When Switch S_{w2} is open circuit : During fault operation, switch S_{w1} is in operation and switch S_{w2} has open circuit fault. In this case, waveforms of the proposed fault tolerant converter voltages and currents are presented for step-up voltage gain of 8.33 for an output power of 100 W. The output voltage,output current and input voltage at duty cycle of 0.865 (86.5%) equals 100 V which is shown Fig. 19.(a). The voltage and current of inductors L_1 and L_2 are depicted in Fig. 19.(b) & Fig. 19.(c) shows the switch currents. The voltage



(a) (b) (c)

Fig. 20. Experimental waveforms when switch S_{w2} is open circuit (a). voltage across capacitor-1 and capacitor-2 (b). voltage across switches (c). voltage across diodes.

TABLE VIII
COMPARISON OF RECONFIGURATION TIME

REF.	[18]	[19]	[21]	[22]	[23]	[25]	[27]	Proposed
Time(msec)	48.8	50	12	250	15	10	10	7

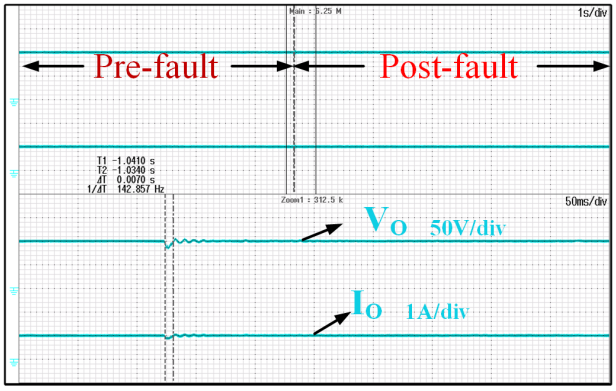


Fig. 21. Dynamic behaviour in closed loop when switch S_{w1} is open-circuit.

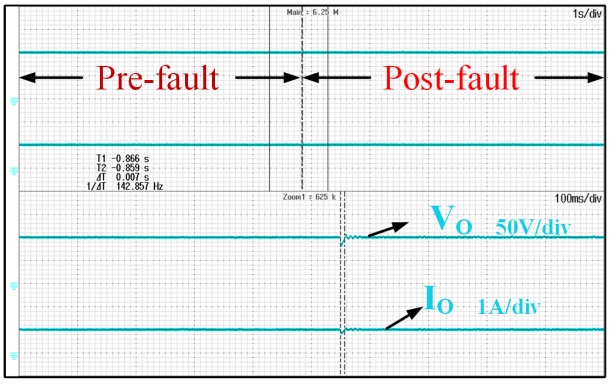


Fig. 22. Dynamic behaviour in closed loop when switch S_{w2} is open-circuit.

across the capacitors C_1 and C_2 are shown in Fig. 20.(a). The voltage stress across switches S_{w1} and S_{w2} is presented in Fig. 20.(b) which is less than the output voltage and equal to V_o/(2-D). The diode voltage D_1, D_2, D_3 waveforms are shown in Fig. 20.(c).

D. Dynamic Operation in Closed-loop:

When switch S_{w1} is open circuit, no current flows through its drain-source terminals (V_{DS1}), then the converter is operated by switch S_{w2} only. The dynamic behaviour of output voltage and current is shown in Fig. 21. It is observed that the output voltage reaches the reference voltage in 7 ms. Similarly, when switch S_{w2} is open circuit, no current flows through its drain-source terminals (V_{DS2}), then the converter is operated by switch S_{w1} only. The dynamic behaviour of output voltage and current is shown in Fig. 22. It is observed that the output voltage reaches the reference voltage in 7 ms.

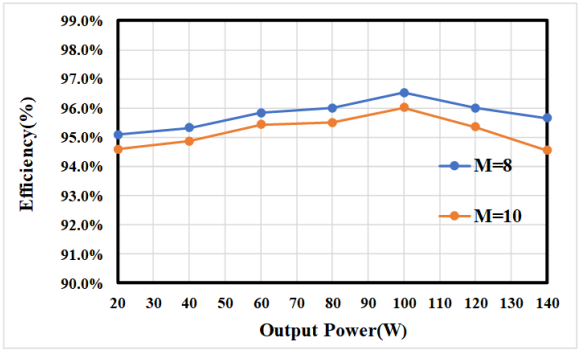


Fig. 23. Performance of the proposed converter.

Table VIII shows that the proposed converter offers better response compared to others fault-tolerant converters reported in the literature. The total losses are calculated by thermal analysis using PSIM software platform with the specifications of the selected devices which are used in proposed converter topology. Fig. 23. shows the efficiency of the propose converter

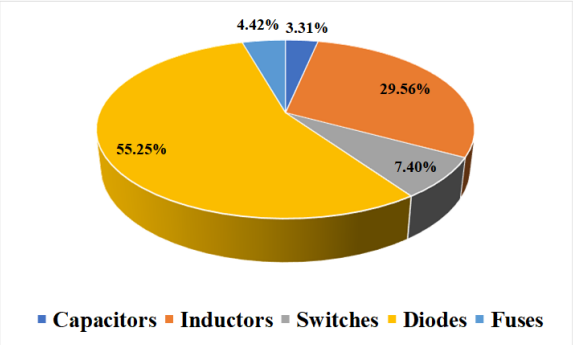


Fig. 24. Loss distribution of the proposed converter.

in normal operation for voltage gain of M = 10 & 8. From this it is observed that the highest experimental efficiency is obtained under normal operation at voltage ratio of 8 is 96.5 %, for 100 W output power. At this maximum efficiency loss distribution across various devices is shown in Fig. 24. From Fig. 24 highest loss occurs across diodes followed by inductors and switches respectively.

VIII. Conclusion

In this paper, a detailed analysis of fault tolerant high step-up DC-DC topology to achieve reconfiguration capability, high voltage gain, continuous input current, and common grounding. The proposed converter offers low voltage stress in both healthy and fault operation across the switches. Switching from healthy to faulty conditions can be performed seamlessly. This allows the use of low ON-state resistance MOSFETs for the converter. In the event of a switch fault, the converter can operate uninterruptedly to supply load current due to its reconfiguration capability. The stability of the converter has been examined using state space analysis. The experimental study illustrates the merits of the proposed converter and its control strategy for both healthy and fault operation. The duty cycle of the converter is controlled to maintains the constant output voltage at 100 V, offers efficiency of 96.5 % at voltage gain of 8.

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