Performance Enhancement of Reduced Component Multilevel Inverter with Optimal Placement of Level Shifter

L. Vijayaraja, *Member, IEEE*, S. Ganesh Kumar, *Member, IEEE*, Marco Rivera, and Ebrahim Babaei

***Abstract*- Multi-Level Inverter (MLI) structures with and without cross-connecting switches are constructed using bi-directional and uni-directional switches and their performances are verified via real-time experimentation. Initially a cross connecting switch inverter (CCSI) is constructed and then modified multilevel inverter (MMLI) is derived from it by removing the cross connecting switches. Two basic units are used in constructing the above converters. Further, the CCSI and MMLI configurations are studied with the identification of optimal placement of the level shifter circuit in the basic unit. In order to enhance the performance of the inverter, different types of procedures for the design of voltage sources are proposed. With the best method of defining the value of voltage sources among the proposed nine different algorithms and with optimal placement of level shifter in the MLI circuit, a 31-level CCSI, a 49 level and 71 level MMLI are designed and tested experimentally. Efficiency, total blocking voltage, harmonic presence, real and reactive powers are obtained for the proposed converters to study their performance. Finally, a comparative analysis is made for the proposed structure against the other MLIs in-terms of switch count, 'ON' state switches, voltage sources and efficiency.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/8526

***Index Terms*-Level shifter, multilevel inverter, power loss, total blocking voltage.**

I. Introduction

The rapid increase in industries necessitates the building of new schemes of inverters, but this presents some challenges like complexity in control, high voltage strain on switches and the need to develop an inverter to produce large voltage steps [1] – [4]. Compared to symmetric source inverters, asymmetric source inverters can produce more voltage steps without using additional components. Asymmetric voltage source values can be designed as unary, binary, trinary, etc., [5] - [8]. In [9], ten numbers of devices are used to construct a fifteen level output voltage. In [10], a thirteen-step inverter is designed using 10 devices and 6 DC sources. An increase in one DC source in the presented inverter configuration produces fifteen levels in the output with the same quantity of switches.

In [11], performances of thirteen and nine level inverters are studied. An asymmetric MLI is able to generate 49-levels using 12 uni-directional switches with parallel connected diodes across each device and 4 voltage sources [12]. The voltage sources are selected in the ratio 1:2:7:14 to obtain the desired voltage steps at the load. The authors attempted to produce a symmetrical waveform at the load with low harmonic content using the aforesaid voltage ratio instead of other voltage ratios.

A 27-level inverter is derived using a fundamental structure consisting of 4 dual direction, 8 single direction switches and 5 voltage sources. An axiom with equal voltage ratios and another axiom with unequal voltage ratios are framed to generate higher voltage steps [13]. In [14], an inverter block producing 13 voltage steps at the load is presented with 1:2 source voltage ratio, whereas the proposed blocks consist of two bi-directional and 6 uni-directional switches. The production of higher voltage steps made possible by interlacing the multiple fundamental units without a polarity generator to produce all the voltage levels. In [15], a generalized inverter unit is presented and by cascading more such units, can produce higher voltage steps with the source voltage ratio as 1:2:2:5. In the proposed work, nine and fifteen voltage levels are constructed using fixed and variable DC sources and the circuit consists of 10 uni-directional switches and 5 voltage sources.

A hybrid T-type inverter is designed without including an inversion circuit to yield 21-levels with voltage source ratio as 1:3. The inverter circuit is developed with 8 uni-direction and 2 bi-direction switches connected with 5 DC voltage sources [16]. A 9-step and 21-step inverter is designed in [17] using the same value of source voltage ratio and unequal voltage ratio without the use of any extra circuit for inversion. The MLI circuit includes 12 switches and 2 voltage sources. Two different axioms are derived to design the value of DC sources to construct more voltage steps. In [18], an MLI is designed using one dual direction and 8 single direction switches and 2 voltage sources without an inversion circuit. In the proposed work, the source voltage ratio is selected as 5:2 and a 15 step inverter is modelled, tested under dynamic load conditions.

From the above discussions, a few advantages in design aspects are found from [9]-[18], where MLIs can be designed without including the inversion circuit at the load end to produce both positive and negative voltage steps, which results in considerable reduction in the switch count. The MLI design presented in [17] produces low standing voltages and

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the MLI structures proposed in [12], [17] and [18] require fewer DC sources in comparison with other inverter designs. It is found that the topologies proposed in [9], [10], [13] and [16] require a greater number of DC sources. In [9], [17] and [18], the presence of capacitor necessitates extra attention to charge balancing and the presented MLI design in [10] and [15] needs a large variety of DC supplies, leading to higher TSV. Also, the MLI structure as shown in [13] utilizes a higher number of dual direction switches that leads to an increase in the total switch count. So, it is found that MLI design without including the inversion circuit has higher standing voltages and requires more varieties of DC sources compared to the MLI with inversion circuit. Hence, a compromise is to be made between reducing the varieties of DC sources, and standing voltage. Therefore, it is required to design an optimal MLI to produce higher voltage steps with reduced part count and standing voltages. In [19], 61-level inverter is designed with optimal structures by connecting basic units without modification and in [20], 15-level inverter is designed by cascading a separate circuit with a basic unit. The separate unit is used for generating the lowest voltage level.

In the proposed work, two fundamental units are connected with the cross-connecting switches and an optimal placement of a level shifter is identified in each fundamental unit of the CCSI. An output voltage of 31 level, 49 level and 71 level can be achieved by placing the level shifter in the optimal location of the fundamental unit in the CCSI and this is shown in Fig. 1. In the view of minimizing the number of switches further, cross connecting switches are removed from the CCSI and this is termed as MMLI.

In the proposed CCSI and MMLI, the following contributions are made:

- Optimal location for placing the level shifter is identified in the basic unit of MLI. Nine frameworks are defined for sizing the voltage sources. Third, fourth and ninth frameworks are identified among them to realise 31 level CCSI, 49 level MMLI and 71 level MMLI with the optimal placement of level shifter.
- Using 14 switches and 6 sources, the proposed MMLI generates 49 levels and 71 levels compared to the CCSI which uses 16 switches and 6 sources to generate 31 levels at the load.
- A considerable reduction in cumulative blocking voltage is achieved in CCSI as compared to MMLI.
- The numbers of 'ON' state switches are brought down in MMLI compared with CCSI.
- A comparative study is done for the CCSI & MMLI with MLIs in-terms of the switch count, 'ON' state switches, voltage sources and efficiency.

The paper is structured as follows: section 2 describes the design of CCSI and MMLI with best procedure identified to produce maximum voltage levels with minimum circuit components, a comparative analysis of CCSI & MMLI versus recent MLIs is presented in section 3, further experimental work of the proposed CCSI and MMLI is demonstrated with performance parameters in section 4 and followed by conclusion is furnished in the last section.

II. Proposed MLI Topology for Generating More Voltage Levels

A. Generalized CCSI Topology with Connecting Switches

The schematic diagram of the CCSI configuration with cross connecting switches is shown in Fig. 1 which is capable of expanding the range of voltage levels with more number of proposed units cascaded in series using the connecting switches S_c and $S_{c'}$. Each unit comprises of three voltage sources ($V_{1,1}$, $V_{1,2}$ & $V_{1,3}$), four uni-directional switches ($S_{1,2}$, $S_{1,3}$, $S_{1,4}$ & $S_{1,4'}$) and one bi-directional switch ($S_{1,1}$). The level generation is done by four switches (S_a, $S_{a'}$, S_b & $S_{b'}$). Increase in the number of voltage levels depends on the location of level shifter and the value of DC sources.

Amplitude of the sources in CCSI is defined using various frameworks such as; A_{x1}, A_{x2}…A_{x9} and the same are introduced in Table II for the proposed 'u' number of fundamental blocks of CCSI with inclusion of level shifter at location 1, 2 and 3. From Table II, it is inferred that for all frameworks, the components count remains same and it is furnished from equations (1) to (4).

$$N_{switch} = 7u + 2 \quad (1)$$

$$N_{source} = 3u \quad (2)$$

$$N_{driver} = 7u + 2 \quad (3)$$

$$N_{on,sw} = 2u + 2 \quad (4)$$

To find the best axioms as presented in Table II to build more number of voltage level across load for the proposed CCSI circuit with 'u' units and level shifter placed at location at 1, 2 and 3 is presented in Fig. 1.

Switching states and output voltage levels for the inverter with connecting switches is shown in Table I, and it is found that an inverter with two cascaded structures using axiom A_{x9} will generate the highest output voltage levels (71) when placing the level shifter at location 3.

Blocking voltage for the fundamental units of the inverter when the level shifter is placed at location 1 is presented in equations (5) and (6),

$$V_{block,u1} = 2(4^u) = V_{sa} = V_{sa'} \quad (5)$$

$$V_{block,u2} = 2(4^{u+1}) = V_{sb} = V_{sb'} \quad (6)$$

The voltage blocked by the switches S_c and $S_{c'}$ is given in equation (7),

$$V_{sc} = V_{sc'} = 8(4^u + 4^{u+1}) \quad (7)$$

Where V_{sa}, V_{sb}, V_{sc}, $V_{sa'}$, $V_{sb'}$ and $V_{sc'}$ are blocking voltages across the switches S_a, $S_{a'}$, S_b, $S_{b'}$, S_c and $S_{c'}$. By equating (5), (6) and (7), total blocking voltage of CCSI is obtained and presented in equation (8),

$$V_{block,T} = 6(4^u + 4^{u+1}) \quad (8)$$

Similarly, the total blocking voltage (TBV) for the CCSI in Fig. 1 with level shifter at location 2 and location 3 are given in equations (9) and (10) respectively,

$$V_{block,T} = 24(5^{u-1} + 5^u) \quad (9)$$

$$V_{block,T} = 30(6^{u-1} + 6^u) \quad (10)$$

For two fundamental units connected in series, the value for 'u' is to be considered as '1' to get the TBV present in CCSI design.

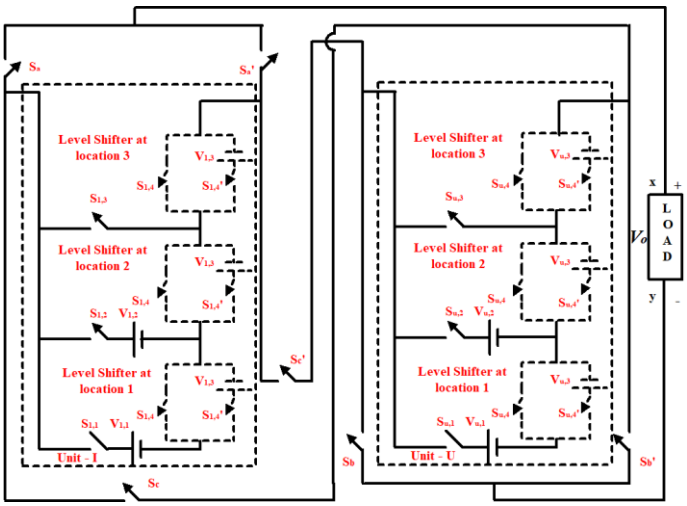

Fig. 1. CCSI with level shifter at location 1, 2 and 3.

TABLE I
ANALYSIS OF CCSI IN TERMS OF LEVEL SHIFTER LOCATIONS

Voltage step-(Output voltage)-(ON State switches)		
Location-1	Location -2	Location-3
Level 1- (0 V)-$S_{1,3}$, $S_{2,3}$,S_a,$S_{b'}$,$S_{c'}$	Level 1-(0 V)-$S_{1,3}$, $S_{2,3}$,S_a,$S_{b'}$,$S_{c'}$	Level 1-(0 V)-$S_{1,3}$, $S_{2,3}$,S_a,$S_{b'}$,$S_{c'}$
.	.	.
.	.	.
Level 16- (15 V)-$S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,S_a,$S_{b'}$, $S_{c'}$	Level 25-(24 V)-$S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,S_a,$S_{b'}$, $S_{c'}$	Level 35-(35 V)-$S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,S_a,$S_{b'}$, $S_{c'}$
.	.	.
.	.	.
Level 31-(-15 V)-$S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4}$,$S_{a'}$,S_b, S_c	Level 49-(-24 V)-$S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4}$,$S_{a'}$,S_b, S_c	Level 71-(-35 V)-$S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4}$,$S_{a'}$,S_b, S_c

To fix the amplitude of voltage sources, nine different axioms are presented in Table 2. By referring Table 2, Fig.2 is drawn between the number of voltage levels generated with respect to number of switches for the proposed fundamental units. From Table II and Fig.2, it is found that, by placing the level shifter in location 1, 2 and 3 for the CCSI configuration consisting of 'u' number of proposed fundamental units with connecting switches, the number of voltage steps constructed is high for axioms 3, 4 and 9 respectively.

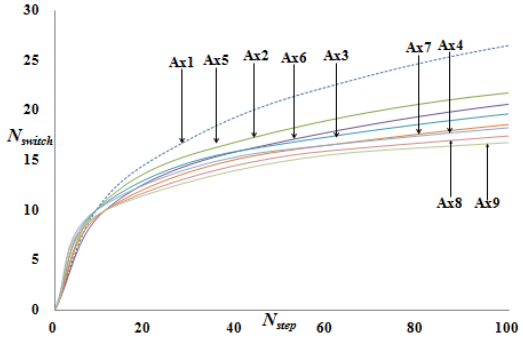

Fig. 2. Plot between N_{step} vs N_{switch} for proposed 'u' units based on different axioms.

B. Generalized MMLI Configuration

Fig. 4 shows the structure of a MLI without cross connecting switches. As there is no requirement of cross connecting switches, number of switches (N_{switch}) required for this topology will be$(5u + 4)$ and it is less than the earlier CCSI configuration $(7u + 2)$. Therefore, the number of driver circuits required is reduced to $(5u + 4)$. Other components like sources and quantity of 'ON' state switches will be the same for both the configurations. In a similar vein as the earlier discussion, the present topology can be analyzed with a level shifter by placing it in locations 1, 2 and 3 in the fundamental unit.

Different axioms for fixing the amplitude of the sources are mentioned in Table II. With the aim of finding the best axiom to generate higher voltage levels, plots are drawn between N_{step} vs $N_{sources}$ as shown in Fig. 3(a).

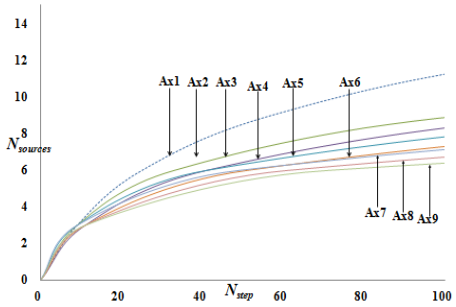

Fig. 3(a). N_{step} vs $N_{sources}$ of 'u' units from proposed axioms.

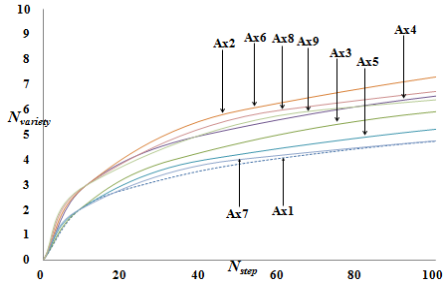

Fig. 3(b). N_{step} vs $N_{variety}$ of 'u' units from proposed axioms.

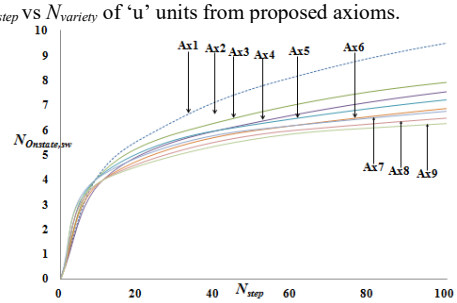

Fig. 3(c). N_{step} vs $N_{on,sw}$ of 'u' units from proposed axioms.

From the Fig. 3 (a), (b) and (c), it is seen that, the placement level shifter in location 1, 2 and 3 for the 'u' units of MMLI generates higher number of voltage steps with minimum number of DC sources, variety of DC sources and 'ON' state switches. Also while placing the level shifter at locations 1, 2 and 3 with axioms 3, 4 and 9, the proposed MMLI will generate higher number of output voltage levels i.e., 31, 49 and 71 levels and the switching pattern is provided in Table III.

TABLE II
AXIOMS TO ASSIGN THE AMPLITUDE OF DC SOURCES FOR THE CCSI & MMLI WITH LEVEL SHIFTER AT LOCATIONS 1, 2 & 3

Axiom's	Source Voltage Ratio	Location 1		Location 2		Location 3	
	$Unit\ 1: V_{1,1}: V_{1,2}: V_{1,3}$: $Unit\ U: V_{u-1,1}: V_{u-1,2}: V_{u-1,3}$	$V_{o,max} = \sum_{q=1}^{u} x\,V_{dc}$	N_{step}	$V_{o,max} = \sum_{q=1}^{u} y\,V_{dc}$	N_{step}	$V_{o,max} = \sum_{q=1}^{u} z\,V_{dc}$	N_{step}
		x		y		z	
Axiom-1 (A_{x1})	1:2:2 : 2:2:2	$3(2^u-1)$	$6(2^u-1)+1$	$4(2^u-1)$	$(2^{u+3})-7$	$4(2^u-1)$	$(2^{u+3})-7$
Axiom-2 (A_{x2})	1:2:2 : 3:3:3	$\frac{3(3^u-1)}{2}$	$3(3^u-1)+1$	$2(3^u-1)$	$4(3^u-1)+1$	$2(3^u-1)$	$4(3^u-1)+1$
Axiom-3 (A_{x3})	1:2:2 : 4:4:4	(4^u-1)	$2(4^u-1)+1$	$\frac{4(4^u-1)}{3}$	$\frac{2(4^{u+1}-4)}{3}+1$	$\frac{4(4^u-1)}{3}$	$\frac{2(4^{u+1}-4)}{3}+1$
Axiom-4 (A_{x4})	1:2:2 : 5:5:5	-	-	(5^u-1)	$2(5^u-1)+1$	(5^u-1)	$2(5^u-1)+1$
Axiom-5 (A_{x5})	1:2:3 : 2:2:2	-	-	-	-	$5(2^u-1)$	$5(2^{u+1}-2)+1$
Axiom-6 (A_{x6})	1:2:3 : 3:3:3	-	-	-	-	$\frac{5(3^u-1)}{2}$	$5(3^u-1)+1$
Axiom-7 (A_{x7})	1:2:3 : 4:4:4	-	-	-	-	$\frac{5(4^u-1)}{3}$	$\frac{10(4^u-1)}{3}+1$
Axiom-8 (A_{x8})	1:2:3 : 5:5:5	-	-	-	-	$\frac{5(5^u-1)}{4}$	$\frac{5(5^u-1)}{2}+1$
Axiom-9 (A_{x9})	1:2:2 : 6:6:6	-	-	-	-	(6^u-1)	$2(6^u-1)+1$

For location 1, the blocking voltage for each block and across the half bridge are given in equations (11) and (12), and the inverter blocking voltages are given in equations (13) and (14),

$$V_{block,b} = \sum_{q=1}^{u} 8(4^u-1)V_{dc} \quad (11)$$

$$V_{block,inv} = \sum_{q=1}^{u} 4(4^u-1)V_{dc} \quad (12)$$

$$V_{block,T} = V_{block,1} + V_{block,2} + \cdots + V_{block,b} + V_{block,inv} \quad (13)$$

$$V_{block,T} = 6(4^u-1)V_{dc} \quad (14)$$

Similarly the blocking voltages of MMLI with level shifter at location 2 are given in equations (15), (16) and (17),

$$V_{block,b} = \sum_{q=1}^{u} 8(5^{u-1})V_{dc} \quad (15)$$

$$V_{block,inv} = \sum_{q=1}^{u} 4(5^u-1)V_{dc} \quad (16)$$

$$V_{block,T} = 6(5^u-1)V_{dc} \quad (17)$$

TABLE III
ANALYSIS OF MMLI IN TERMS OF LEVEL SHIFTER LOCATIONS

Voltage step-(Output voltage)-(ON State switches)		
Location-1	Location -2	Location-3
Level 1- (0 V)- $S_{1,3}$,$S_{2,3}$,T_1, T_2	Level 1-(0 V)- $S_{1,3}$,$S_{2,3}$,T_1, T_2	Level 1-(0 V)-$S_{1,3}$, $S_{1,4}$,$S_{2,3}$, $S_{2,4}$,T_1, T_2
.	.	.
.	.	.
Level 16- (15 V)- $S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,T_1, T_2	Level 25-(24 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_1, T_2	Level 36-(35 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_1, T_2
.	.	.
.	.	.
Level 31-(-15 V)- $S_{1,1}$,$S_{1,4'}$,$S_{2,1}$,$S_{2,4'}$,T_1, T_2	Level 49-(-24 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_3, T_4	Level 71-(-35 V)- $S_{1,2}$,$S_{1,4'}$,$S_{2,2}$,$S_{2,4'}$,T_3, T_4

The blocking voltages of MMLI with level shifter at location 3 are given in equations (18), (19) and (20),

$$V_{block,b} = \sum_{q=1}^{u} 10(6^{u-1})V_{dc} \quad (18)$$

$$V_{block,inv} = \sum_{q=1}^{u} 4(6^u - 1)V_{dc} \quad (19)$$

$$V_{block,T} = 6(6^u - 1)V_{dc} \quad (20)$$

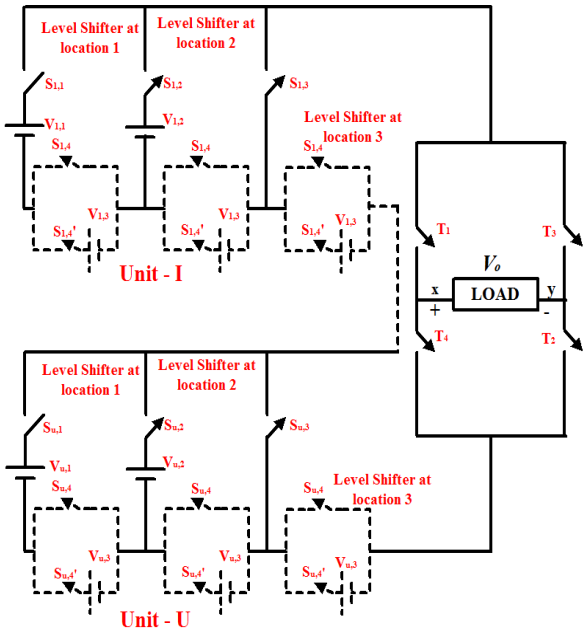

Fig. 4. MMLI design.

III. Comparison of CCSI & MMLI with Existing MLIs

The MMLI shown in Fig. 3 is analytically compared with recent MLIs presented in [13] – [18]. An examination is performed on the MLIs with the modified inverter design using A_{x4} and A_{x9}, focusing on the amount of driver circuits, switches and DC supply to produce any number of output voltage steps. Further, the quantities of 'ON' state switches with respect to N_{step} are compared and this is shown in Table IV.

A plot between the quantities of switches and the amount of voltage steps for referred MLI model [13]-[18], proposed CCSI and MMLI configurations is presented in (Fig. 5(a)). The plot shown in Fig. 5(b) explains the comparison of 'ON' state switches with respect to the referred MLI models in [13]-[18] and proposed inverter configurations. From the plot, it is inferred that the MMLI designed using A_{x9} shows better performance in comparison with the other referred MLIs and the proposed inverter configuration with fourth axiom A_{x4}.

Fig. 5(c) shows the plot between the quantities of voltage sources and voltage steps generated by the referred MLIs and the proposed inverter configurations. The plot shows that an MMLI with A_{x9} is able to generate more voltage steps using a minimum amount of sources. Also, the requirement of driver circuits for the proposed CCSI and MMLI configurations are lesser when compared to the other referred MLIs [13]-[18] and this is shown in Fig. 5(d). This results in a reduction in MLI size.

Fig. 5(e) represents the graph between the requirements of variety of voltage sources and the voltage levels generated by the existing MLIs, CCSI & MMLI. From Fig. 5(e), it is inferred that A_{x4} & A_{x9} are able to construct more voltage steps using minimum variety of sources except R_{15}.

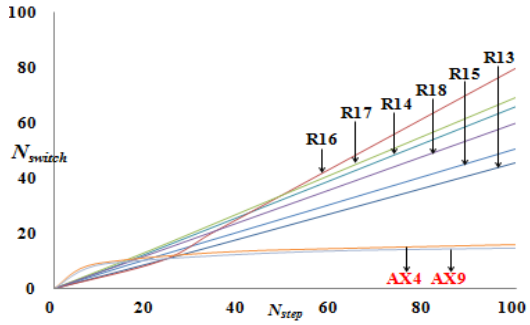

Fig. 5(a). Comparison of N_{step} vs N_{switch} for the recent MLIs with MMLI by placing level shifter at location 2 and 3.

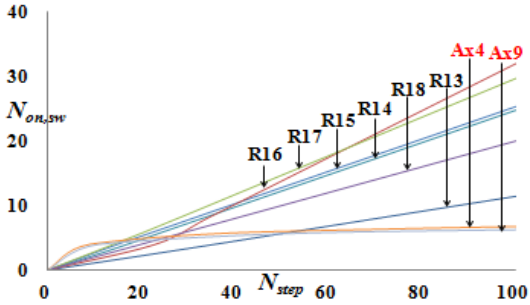

Fig. 5(b). Comparison of N_{step} vs $N_{on,sw}$ for the recent MLIs with MMLI with level shifter at location 2 and 3.

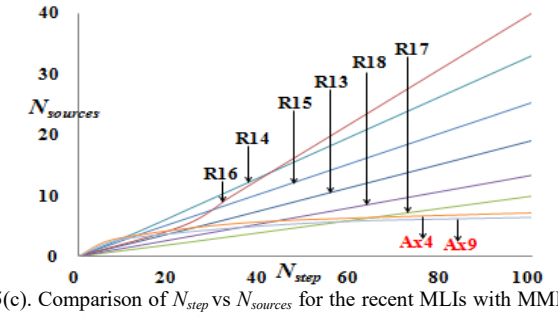

Fig. 5(c). Comparison of N_{step} vs $N_{sources}$ for the recent MLIs with MMLI with level shifter at location 2 and 3.

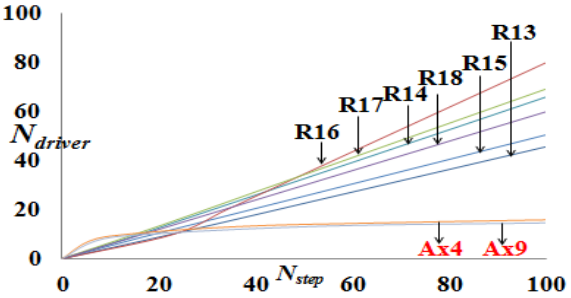

Fig. 5(d). Comparison of N_{step} vs N_{driver} for the recent MLIs with MMLI by placing level shifter at location 2 and 3.

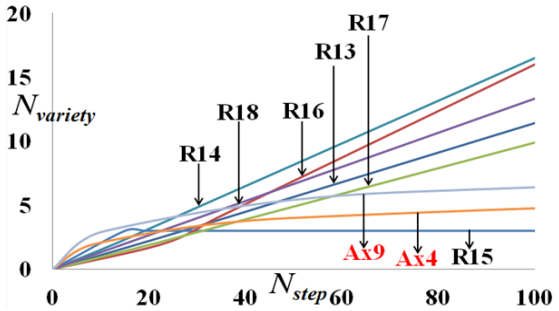

Fig. 5(e). Comparison of N_{step} vs $N_{variety}$ for the recent MLIs with MMLI by placing level shifter at location 2 and 3.

From the above analytical comparison, it is proposed to make a real-time model of 31-level CCSI based on Fig. 1 with level shifter placement at location 1, 49-level and 71-level MMLI configuration based on Fig. 4 with level shifter placement at locations 2 and 3 for fixed and variable load (assumed to be an impedance load) conditions.

IV. Experimentation of CCSI & MMLI to Generate 31-Levels, 49-Levels and 71-Levels

The CCSI circuit shown in Fig. 1 with two fundamental units is developed in real-time (Fig. 6) to produce 31 voltage steps at load, by placing a level shifter at location 1. Further, MMLI is developed in real time (Fig. 7) to construct 49 and 71 output voltage levels at a reactive load by placing the level shifter at locations 1, 2 and 3 respectively. The specifications of the designed MLI are given in Table V.

TABLE V
Specifications of the Developed MLIs

Axiom / Level shifter location	Input DC voltages assumed	Number of Voltage steps achieved (peak to peak voltage)	Load value used	Output Current (A)
Inverter with cross connected switches (CCSI)				
A_{x3} / 1	$V_{1,1}$=5V, $V_{1,2}$,$V_{1,3}$=10V $V_{2,1}$=20V, $V_{2,2}$,$V_{2,3}$=40V	31 (±75V)	250Ω -80mH, 135Ω-100mH, 100Ω-120mH	0.3 A 0.55 A
Inverter without cross connected switches (MMLI)				
A_{x4} / 2	$V_{1,1}$=5V, $V_{1,2}$,$V_{1,3}$=10V $V_{2,1}$=25V, $V_{2,2}$,$V_{2,3}$=50V	49 (±120V)	240Ω -140mH, 135Ω- 120mH, 95Ω-100mH	0.5 A 0.9A 1.3A
A_{x9} / 3	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=15V $V_{2,1}$=30V, $V_{2,2}$=60V, $V_{2,3}$=90V	71 (±175V)	100Ω -100mH, 60Ω -80mH, 40Ω-60mH	2 A 3 A 4 A

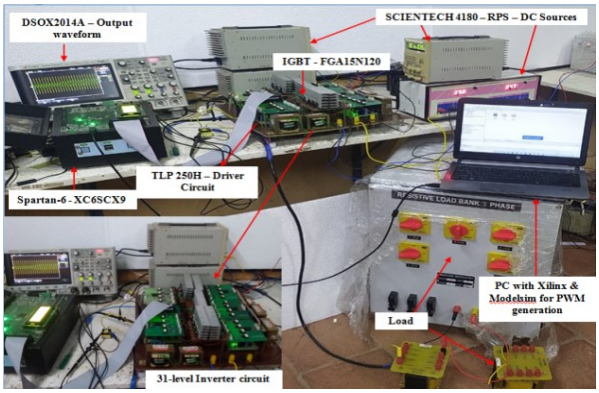

Fig. 6. Hardware setup of 31-level CCSI.

TLP250H is used to power the semiconductor switch FGA15N120 IGBT. The Xilinx Spartan 6 FPGA controller XC6SCX9 is used to provide pulses for the switches. The software coding is initially created in Modelsim and flashed onto an FPGA controller. To run the inverter, pulses are produced by the controller and given to the switches. Scientech 4180 regulated DC supplies with a single channel rating of 30V max and 2 channels are connected in series to create 60V that is utilized for validation. The edge control approach is used to generate the pulses.

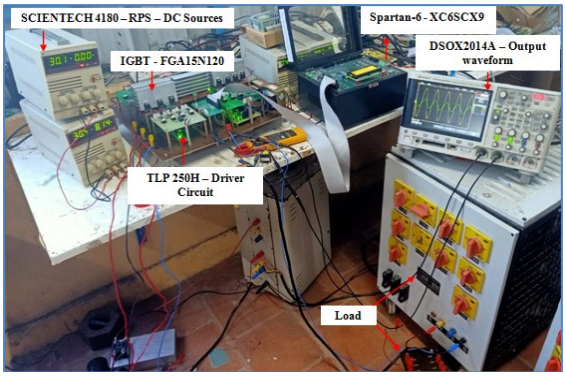

Fig. 7. Hardware setup of MMLI producing 49 and 71 voltage steps.

The experimental setup is validated against a sudden change in impedance load with the test parameters as given in Table V to generate 31, 49 and 71 voltage steps and this is shown from Fig. 8 to Fig. 10.

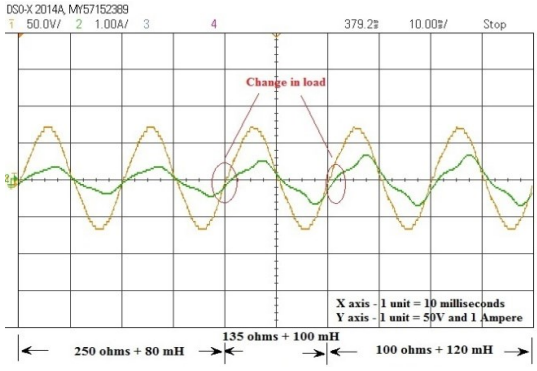

Fig. 8. Experimentation– 31 level CCSI – variable RL load.

It is evident that the developed MLIs can perform well when faced with a sudden shift in load; the voltage magnitudes remain constant while the current magnitudes change with change in the loading conditions. From the above, real time implementation and discussion, the features observed from CCSI and MMLI are promising.

It is seen that the developed CCSI as shown in Fig. 6 generate 31 voltage steps by using 16 switches, whereas the real-time setup shown in Fig. 7 (MMLI) produces 49-level and 71-level voltage steps by using only 14 switches. Hence, it is proved that significant reduction in the amount of switches is possible and generation of more output voltage steps is made by placing the level shifter at location 3 of the MMLI based on the experimental output as shown in Fig. 10.

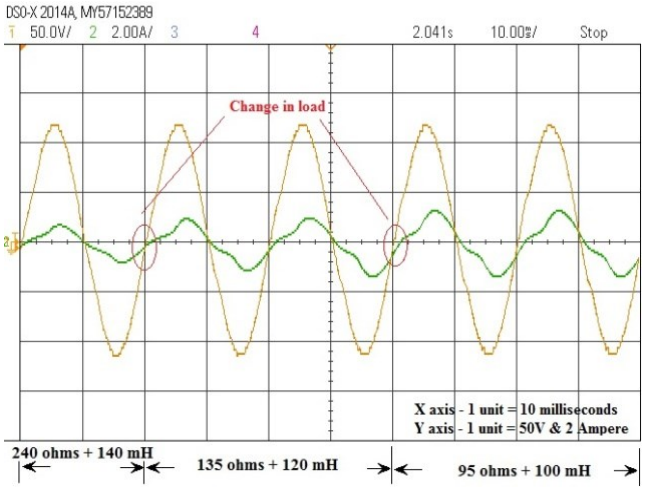

Fig. 9. Experimentation– 49 level MMLI – variable RL load.

It is observed that the wave shape of the load voltage looks sinusoidal, whereas the load current waveform becomes distorted, which is due to the effect of partial saturation in the transformer, which is connected as an inductive load.

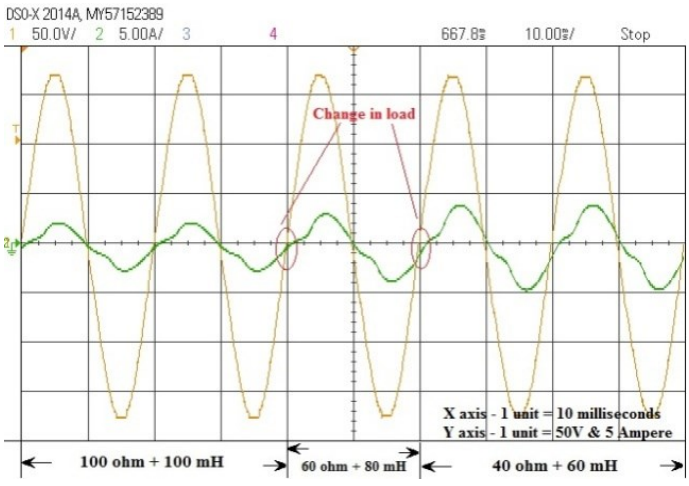

Fig. 10. Experimentation– 71 level MMLI – variable RL load.

A. Power Loss Calculation for the Proposed Inverter

Loss calculation of CCSI and MMLI can be done from equation (21).

$$P_{tcl} = [V_{sw} + R_{sw} i^{\beta}(t)] i(t) \qquad (21)$$

The overall conduction loss is shown in equation (22) when the number of IGBTs (N_{IGBT}) and diodes (N_{diode}) for a specific conduction interval are taken into account.

$$P_{tcl} = \frac{1}{2\pi} \int_0^{2\pi} [N_{IGBT}(t) P_{tcl,IGBT}(t) dt] \qquad (22)$$

Power loss due to switching is calculated from equation (23).

$$P_{tsl} = f \frac{1}{2\pi} \sum_{i=1}^{N_{IGBT}} [E_{ON} + E_{OFF}] = \frac{1}{6} V_{sw} (I T_{off} + I' T_{on}) \qquad (23)$$

The efficiency and total power losses (P_{tpl}) are given in equation

$$P_{tpl} = P_{tcl} + P_{tsl} \qquad (24)$$

$$\eta = \frac{P_o}{P_o + P_{tpl}} \qquad (25)$$

Where output power (P_o) is obtained from $V_{rms} * I_{rms}$

Taking into account the aforementioned equations, the efficiencies for the 31 level CCSI, 49 level and 71 level MMLI are tabulated for the load impedance (70+j21.98) Ω in Table VI. Table VI indicates that, efficiency obtained from 71 level MMLI is greater compared to 31-level CCSI and 49-level MMLI.

From Fig. 11, it is observed that the MLI configuration using A_{x9} is capable of generating 71 voltage steps in experimentation, which utilizes lower number of devices and drivers to produce load voltage of ±175V with low harmonic content in the load waveform when compared to 49 and 31 voltage steps configurations. Hence, it is concluded that the 71 level inverter is superior to the other two configurations, as presented in this paper. Also, this kind of inverter configuration plays a vital role in renewable energy systems for power conversion, since it uses isolated DC sources to produce a smooth sinusoidal waveform at the load.

TABLE VI
PERFORMANCE PARAMETERS OF CCSI & MMLI

No. of Level & MLI	Impedance Z (Ω)	V_{0rms}(V)	I_{0rms} (A)	P (W)	Q (var)	THD (I_0) %	TBV (V)	% η
31 CCSI	(70+j21.98)	54.01	0.736	39.77	10.88	2.81	$160V_{dc}$	95.74
49 MMLI		93.65	1.31	122.89	28.74	1.88	$144V_{dc}$	96.34
71 MMLI		129.72	1.73	224.58	58.92	1.22	$210V_{dc}$	97.05

A study is performed to compare the harmonic presence in the load waveforms between [14], [15], [16], [18], 49, and 71-level MMLI. It is found that the harmonic presence in the 71-level MMLI load wave form is found to be low, and is given as 1.22%. Also, the efficiency of the 49- and 71-level MMLIs is compared against the other MLIs, and is given as 96.74%, which is greater than the referred MLIs in [13], [15], and [18].

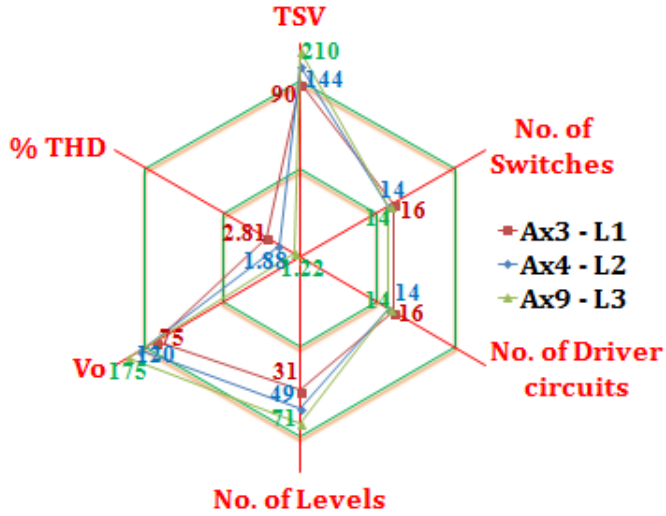

Fig. 11. Parameter comparison of proposed 31, 49 and 71 level inverter.

V. Conclusion

Multilevel inverter configurations with and without cross-connecting switches namely: CCSI and MMLI are presented in this paper. Two fundamental units are cascaded and this is taken for the consideration in the present study. Further, optimal placement of level shifter is identified for CCSI and MMLI. By performing said optimal placement, maximum number of levels in CCSI reaches $[6(2^u - 1) + 1]$ levels with 'u' numbers of basic units connected in series with level shifter placed at location 1. Whereas in the MMLI, the number of level reaches $3(3^u - 1) + 1$ and $2(4^u - 1) + 1$, by placing the level shifter in locations '2' and '3' respectively.

Maximization of the number of voltage steps is performed by selecting a suitable axiom (Table II) and placing the level shifter at location 1 for CCSI and locations 2 and 3 for MMLI. Nine axioms are defined for sizing the voltage sources from which A_{x3}, A_{x4} and A_{x9} are identified as the most optimal and they are used to produce 31-level (level shifter in first location), 49-level (with level shifter in second location) and 71-level (with level shifter in third location) respectively in real time. The details are furnished in Table VII.

TABLE VII
Best Procedure Identified for the Design of MLI

Axiom & Location	Voltage source values	Output Level	THD in %(RL load in Ω)	TBV (V)	% η
Inverter with cross connecting switches (CCSI)					
A_{x3} & 1	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=10V, $V_{2,1}$=20V, $V_{2,2}$=40V, $V_{2,3}$=40V	31	2.81 (90+j28.26)	$160V_{dc}$	95.74
Inverter without cross connecting switches (MMLI)					
A_{x4} & 2	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=10V, $V_{2,1}$=25V, $V_{2,2}$=50V, $V_{2,3}$=50V	49	1.88 (70+j21.98)	$144V_{dc}$	96.34
A_{x9} & 3	$V_{1,1}$=5V, $V_{1,2}$=10V, $V_{1,3}$=15V, $V_{2,1}$=30V, $V_{2,2}$=60V, $V_{2,3}$=90V	71	1.22 (190+j31.4)	$210V_{dc}$	97.05

Further, performance parameters such as efficiency, total blocking voltage and THD for the proposed circuit are examined. From the performance analysis and comparison with the proposed inverter structures, it can be concluded that proposed MMLI structures show better performance with the optimal placement of level shifter.

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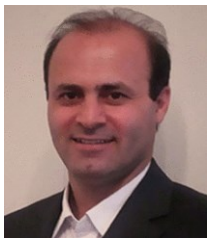

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