Verilog-A Modeling of an Electrophotonic Emitter-Waveguide-Detector (EWD) System Compatible with Standard CMOS Technology

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***Abstract*—Lab-On-A-Chip (LOC) devices that utilize light-based detection principles offer advantages compared with their electronic counterparts, such as higher sensitivity and not necessarily needing markers, simplifying their use, and reducing reagent consumption. Recently, the development of Si-based light emitters compatible with standard CMOS manufacturing processes has overcome one of the main obstacles in creating fully integrated electrophotonic systems on the same substrate. This groundbreaking achievement means the possibility of integrating photonic and driving circuitry in the same chip. However, due to its extreme novelty and specific electronic requirements, new design solutions must be tailored to further aid fulfilling the promise of a fully integrated electrophotonic system. The lack of existing circuit design models and tools hinders the advancement of this technology. To aid further in designing these systems, this article presents the development of a Verilog-A macromodel for an electrophotonic circuit composed of a Light Emitting Capacitor (LEC), a waveguide, and a sensor. The system was simulated in the Cadence Virtuoso environment, and a use case exhibits the system simulation including a CMOS circuit for emitter excitation and sensor reading.**

***Index Terms*—electrophotonic, OEIC, Light Emitting Capacitor (LEC), modeling, Verilog-A.**

I. Introduction

Electrophotonics is an emerging platform that facilitates the development of applications requiring the manipulation of both light and electricity, such as sensing applications [1]. Among the most promising applications are lab-on-a-chip (LOC) systems. The CMOS fabrication industry offers an attractive platform for producing fully integrated silicon-based solutions, which are cost-effective and enable point-of-care services. However, one of the most challenging requirements is to have a reliable light source that can be fabricated using a standard CMOS process , which relies solely on the use of silicon [2].

Recently, groundbreaking advances in the development of electrophotonic systems have been achieved, as described in [3]. The novel system comprises an all-silicon integrated emitter-waveguide-detector, which will be called the EWD system from now on. This system is compatible with a standard CMOS process. The EWD's structure, which is illustrated in Fig. 1 a), utilizes a non-conventional light emitter known as Light Emitting Capacitor (LEC), which uses Silicon-Rich-Silicon Dioxide (SRO) as the active material [4]. The system described in [3] was modified in [1] as seen in Fig. 1 b) by opening a window in the top coating in order to use it as label-free sensor.

Label-free detection is an alternative in optical biosensing. Unlike fluorescence-based detection that requires laborious labeling processes and may interfere with biomolecule function, label-free detection allows for easy and cost-effective measurements in their natural state [5]. It enables quantitative and kinetic assessment of molecular interactions, making it advantageous in ultrasmall detection volumes. Notably, the signal from label-free detection remains unaffected by sample volume because it measures refractive index changes induced by interactions, offering superior scalability. As a result, label-free optical biosensors offer greater versatility in biomedical research, healthcare, and various other applications [6].

The monolithic electrophotonic system presented in [1] and [3] is, to the best of our understanding, the first of its kind, and to fulfill the promise of a fully monolithic CMOS-compatible LOC, it is necessary to integrate all the required electronic circuitry that can drive the photonic elements. The latter constitute cutting-edge technology which does not operate under the same electronic conditions as conventional devices; and designing and integrating the circuitry capable of driving the integrable light emitters and capturing and processing signals from the photodetectors, constitute a significant challenge from the integrated circuit (IC) design standpoint. One wall to break is the lack of models of the integrable photonic devices, which significantly complicates the task of the IC designer, as it is not possible to design and simulate the electrophotonic system using standard IC tools directly and completely.

The current approach to simulate the behavior of devices that compose this type of system involves using finite element method simulators such as COMSOL Multiphysics® [7], Finite-Difference Time-Domain (FDTD) numerical solvers for Maxwell's equations [8], or more recently, component and system-level simulators such as Lumerical Interconnect [9]. While these programs provide detailed and precise results and offer great flexibility, they are also computationally intensive. Additionally, these software solutions are incompatible with

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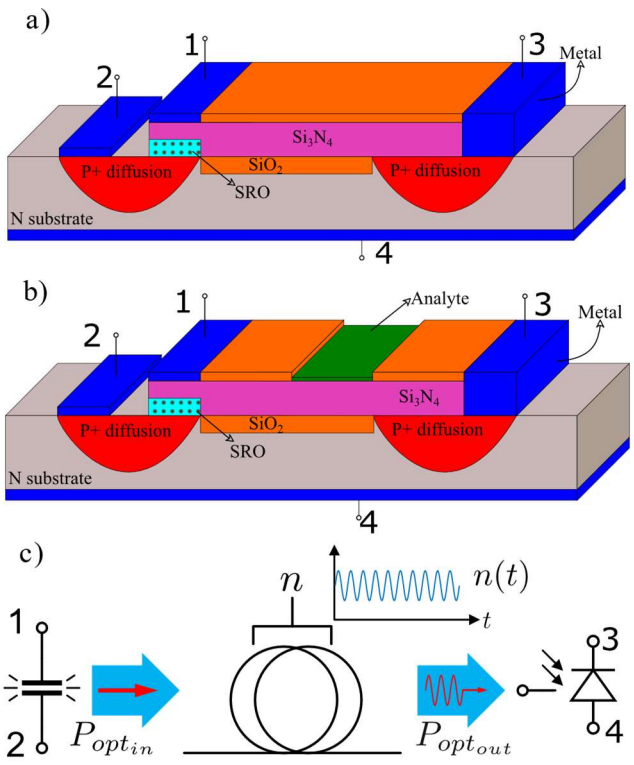

Fig. 1. a) Physycial impletation of electrophotonic integrated system developed in [3] from left to right it can be seen the emitter, the waveguide, and the detector; b) Modification to EWD system from a) here a window was opened in the top coating to analyze the effect of a change in refractive index on the detected optical power as reported in [1]; c) Schematic representation.

the typical design flow tools used in integrated circuit design or with the SPICE models commonly employed in industry and academia. On the other hand, there is the approach of the established electronics industry, which often uses assumptions and approximations to derive simpler governing equations or behavioral models that describe each electronic device. They use Verilog-A or SPICE, which enable the simulation of complex systems with lower computational requirements. Verilog-A can potentially be used to model and simulate electrophotonic components within the IC design tool. It is compatible with Cadence Virtuoso, the most widely used EDA tool, and allows the introduction of different disciplines, such as the optical domain.

Several articles have previously demonstrated Verilog-A macro-modeling of photonic and electronic components, as evidenced in references [10]–[12]. These works have predominantly focused on macro-modeling waveguides, lasers, Mach-Zehnder modulators, photodiodes, and even optomechanical systems, as exemplified in reference [13]. It is worth noting that these prior proposals primarily employed light emitters incompatible with standard CMOS processes.

However, modeling and simulating the new LEC presents a significant challenge due to the complexity of the underlying physics. This challenge is further amplified when considering a comprehensive system like the one depicted in Fig. 1. Typically, simulations of waveguides and sensors are conducted separately, with input light sources approximated to those of lasers. As such, there has not been a complete model to simulate the LEC, the waveguide, and the sensor in unison. This work introduces a pioneering macro-modeling approach for an electrophotonic system that utilizes a Light Emitting Capacitor (LEC). The LEC stands out as a revolutionary device compatible with standard CMOS manufacturing processes, showcasing its potential for various sensing applications. For the first time, this work presents the modeling of an electrophotonic EWD system using Verilog-A to co-simulate an electrophotonics system with a CMOS compatible light source, the LEC. This advancement paves the way for new research avenues, allowing for simulations that encompass not only the photonic circuit but also the CMOS circuitry, contributing to the advancement of monolithic integration of optics and photonics under the same technology and philosophy of standard Si-based integrated micro and nanoelectronics. The results from the macro-model were compared with experimental data for the DC curve of the LEC, transient simulations of the modified EWD system, and DC results for the wavesensor, which was simulated using a finite element simulator. The system is illustrated in Fig. 1.

The organization of the paper proceeds as follows: In Section II, the electrophotonic elements that are modeled are theoretically described, the proposed Verilog-A code is presented and discussed. Section III presents the results of the simulations, discusses their implications, and includes a comparison with experimental results. Section IV introduces a use case of the proposed model, where a circuit combining the electrophotonic part and the CMOS circuitry was designed using the proposed models. Finally, Section V summarizes the findings of the study and suggests avenues for future research.

II. Description of Devices and Theoretical Foundations of Operation

When a LEC is activated in an EWD system, light is generated, propagated through the waveguide, and detected in the sensor. The main novelty of this system is that the light source is CMOS-compatible and monolithically embedded into the nitride waveguide. This is advantageous as it avoids the alignment and insertion issues associated with external light sources and is compatible with a standard CMOS manufacturing process, reducing production costs.

In [1], a modification to the system proposed in [3] was implemented, opening a window in the upper cladding of the waveguide to analyze the changes in detected photocurrent due to the presence of a substance. It was found that the EWD can be used as a refractive index sensing system to the order of tenths. One way to improve the system's sensitivity is to develop integrated readout CMOS circuits that can detect lower changes in currents. The contributions of this work are the behavioral models for the EWD system that can be simulated alongside the electronics in the circuit design tool and the description of the electronic biasing and readout system working in the same EDA tool.

A. Light Emitting Capacitor (LEC)

A LEC is a light emitter converting an input electrical current into light. In this case, it consists of a bi-layer of Silicon Nitride (Si_3N_4) and Silicon-Rich-Silicon Dioxide (SRO), with an

aluminum gate as top-contact, and a p-type degenerately doped silicon well. The mechanisms by which this device emits light and its current-voltage relationship are still under investigation [14]. Some models of charge transport used to describe the relationship between the applied electric field and the current density of thin dielectric materials, as occurs in the LEC, are Fowler-Nordheim (FN) (1), Poole-Frenkel (PF) (2), and Trap-assisted Tunneling (TAT) (3) [15]. The device's current densities describe the physical behavior.

$$J_{FN} = \frac{q^2 m E_f^2}{8\pi h \phi_B m^*} \times \exp\left(-\frac{8\pi\sqrt{2qm^*}\phi_B^{3/2}}{3hE_f}\right) \quad (1)$$

$$J_{TAT} \propto \exp\left(-\frac{8\pi\sqrt{2qm^*}\phi_t^{3/2}}{3hE_f}\right) \quad (2)$$

$$J_{PF} \propto E_f \times \exp\left(-q\left(\phi_t - \sqrt{\frac{qE_f}{\pi\varepsilon_r}}\right)\Big/ kT\right) \quad (3)$$

Where J_{FN}, J_{PF} and J_{TAT} are the current densities for the conduction mechanisms FN, PF, and TAT, respectively; q, m and m^* are the charge, the mass, and the effective mass of the electron, respectively; h is the Planck constant, ϕ_B the height of the potential barrier, k the Boltzmann constant, ϕ_t the difference in energies between the conduction band and the level of traps, ε_r the relative permittivity of the material and T the temperature.

Determining the predominant conduction mechanism in advance is challenging; typically, a fitting to the charge models presented is made from the data. Therefore, the scheme in Fig. 2 proposes the device's macromodels. The DC component was modeled as constant series resistor R_s with a nonlinear parallel resistor R_p whose resistance is defined by a look-up table built from measurements in manufactured prototypes. Cubic splines were used to interpolate values. The look-up table variables are the voltage (V), the current (I), and the device area (A). The AC behavior was modeled as an equivalent capacitor composed of two series capacitors, one made from silicon nitride and another from SRO, as seen in (4)-(6). The model includes the photonic shot noise generated by the LEC and the thermal resistance noise. Finally, an optical port was created to model the optical power generated by the device, and it was modeled linearly with the parallel resistance current. The slopes were obtained from measurements in fabricated prototypes and fitted to a second-order polynomial.

$$C_{eq} = C_{Si_3N_4}\, C_{SRO}/(C_{Si_3N_4} + C_{SRO}) \quad (4)$$

$$C_{Si_3N_4} = \varepsilon_{Si_3N_4} A/th_{Si_3N_4} \quad (5)$$

$$C_{SRO} = \varepsilon_{SRO} A/th_{SRO} \quad (6)$$

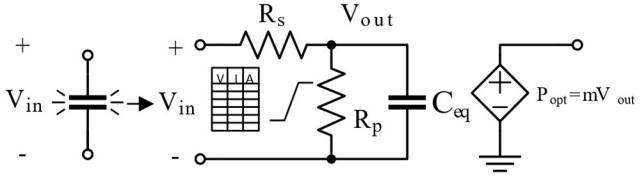

Fig. 2. Symbol and schematic representation of LEC proposed macro model.

```
analog begin
  @(initial_step) begin
    Clec=(Area/100)*Clec_A; // Capacitance in F
  end
  R=$table_model(Area,V(inp,inn),"LookupLEC.txt","3S,
3L");S,3L");
  Rp=R-Rs;
  I(int, inn) <+ V(int, inn)/Rp;
  I(inp, int) <+ V(inp, int)/Rs;
  I(inp, int)<+white_noise((4*`P_K*$temperature)/Rs);
  I(int, inn) <+ Clec*ddt(V(int,inn));
  optPower=(a*pow(Area,2)+b*Area+c)*V(int,inn)/Rp*100
0;//Optical Power in pW
  OptPwr(outLight) <+ optPower;
  OptPwr(outLight) <+
  white_noise((2*`P_H*`P_C/lambda)*optPower);
end
```

B. Integrate Waveguide

When a light signal propagates through a waveguide, the two principal effects are attenuation and chromatic dispersion [16]; the latter does not modify the intensity of the detected signal. Due to this application being in low frequency, this effect was not modeled. Fig. 3 shows the waveguide and modified waveguide schematic symbol and macro models block diagram. In the modified waveguide, a window was opened in the top coating to analyze the effect of a change in refractive index on the detected optical power and thus study its possibilities to serve as a refractive index detection system [3]. To model those effects on the output optical power, an input port representing the upper cladding's refractive index and a modulation function $f(n)$ were added. The function $f(n)$ is a second-order polynomial and was fitted to the experimental data.

```
analog begin
  @(initial_step) begin
    attenuation =pow(10,-attenuationdB/10);
  end
  OptPwr(outLight) <+
  attenuation*length*(a*pow(V(n),2)
  +b*V(n)+c)*OptPwr(inLight);
End
```

C. Light Detector

A photodetector turns optical power into electrical current; the transfer factor is the responsivity (R) and specifies how much current is generated from a given optical power.

A typical photodetector is a photodiode

Fig. 4 shows a simplified model of a photodiode operating in the inverse mode. I_{ph} is the photogenerated current, C_j the junction capacitance, I_{dark} the inverse current when there is no optical power, and I_{noise} is the photodiode noise current composed of shot and thermal noise.

x

Fig. 3. Integrated waveguide symbol and macro models block diagram.

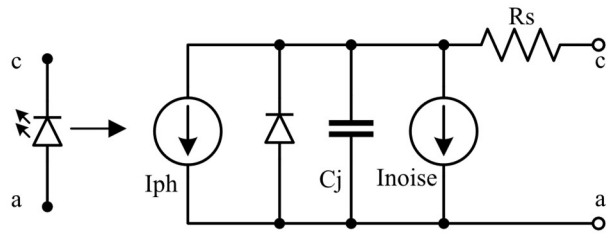

Fig. 4. Macro-model of a reverse biased photodiode.

```
analog begin
  I(c,int) <+ V(c,int)/Rs;
  I(int,a) <+ -Idark*(exp(V(a,int)/0.026)-1);
  I(int,a) <+ Cj*A*ddt(V(int,a));
  I(int,a) <+ Responsivity*OptPwr(opt)*1E-9;
  I(int,a) <+
white_noise(2*`P_Q*Idark*(exp(V(a,int)/0.026)-1));
  I(c,int) <+ white_noise(4*`P_K*$temperature/Rs);
end
```

Recently a new type of photosensor called wavesensor was proposed [17]; its structure can be seen in Fig. 5 b). It is a MISFET using silicon nitride as insulator, allowing it to couple with an integrated waveguide, thereby decreasing the insertion losses. Furthermore, the sensor has gain, which is attractive for sensing low-intensity signals. The sensor operates in punch-through mode, as described by the following equations:

$$I_{DS} = 9/8\ \varepsilon_s \mu_n A/L^3\ (V_{DS} - V_{PT})^2 \quad (7)$$

$$I_D = I_{dark} + \beta I_{opt} \quad (8)$$

$$I_{opt} = \eta q\, P_{in} \lambda / hc \quad (9)$$

Where μ_n is the electron mobility, ε_s the silicon permittivity, A is the cross-sectional area, L the drain to source separation, V_{PT} is the Punch-Through voltage, η is the quantum efficiency, P_{in} the input optical power and β the gain. The gain is a function of the polarization point, and it was extracted from device curves using a look-up table.

III. Simulation Results

The coherence of the proposed macromodels for the EWD system is validated using DC and transient simulations. In this study, both the waveguide length and attenuation were specifically chosen to replicate the experimental setup and findings presented in [1]. The waveguide, designed with a length of 0.1 cm, was chosen not only to maintain the device's compactness, minimizing its footprint, but also to ensure its visibility and ease of manipulation using standard laboratory probes. Additionally, this waveguide length was selected considering the technological constraints associated with nitride deposition. This parameter is inherently limited by the tensile and compressive forces that arise when depositing nitride on silicon. Furthermore, the thickness of the LEC needed to be kept constrained to diminish the voltage requirements for its activation. With these critical factors in mind, theoretical calculations were performed to estimate the losses in various designs, also considering the emission characteristics of the SRO and the responsivity of the silicon photodiode. The objective was to determine the maximum distance at which the signal could still be resolved effectively. A length of 1 mm was found to be significantly lower than this threshold, thus making it an acceptable reference value for the waveguide's design. The attenuation was defined as 2.25 dB/cm according to previous simulations, and the LEC area was varied according to the area of the fabricated devices.

The EWD's electrical properties were assessed using a dual-channel Keithley 2636B source-meter. To activate the emitter, tungsten microprobes were positioned on the designated pads, as depicted in Fig. 6. The photodiode's current was characterized by connecting a probe to the anode pad and the wafer holder to the alternate terminal of the channel. Channel A of the source-meter supplied power to the emitter, while channel B was linked to the photodiode to apply reverse bias and monitor its current readings. A specially developed software was employed to coordinate the data collection from both channels of the

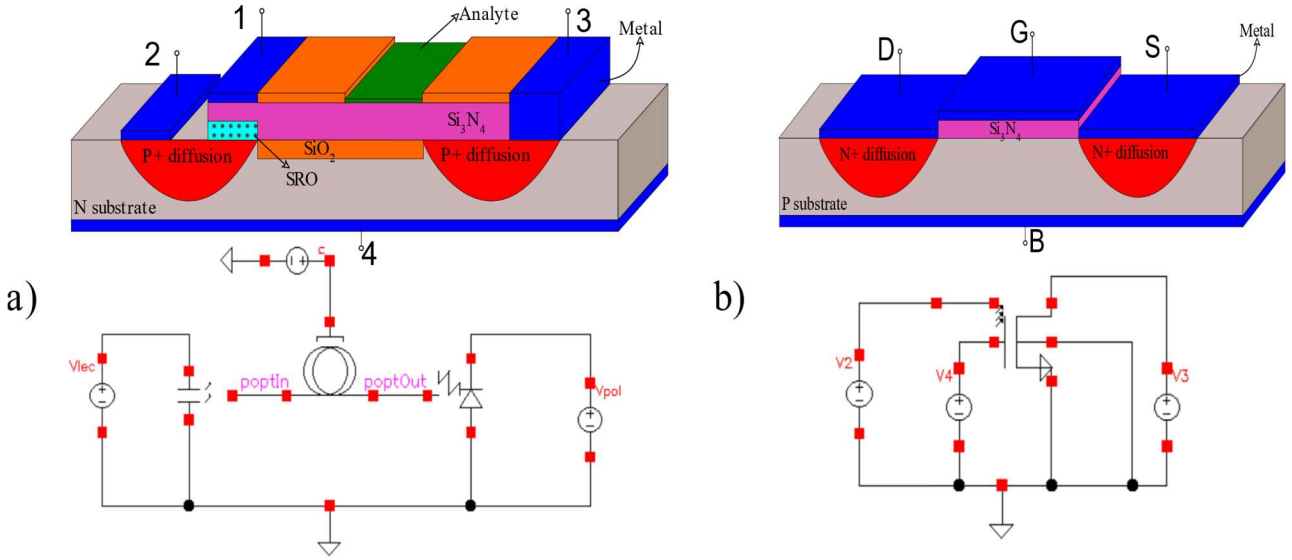

Fig. 5. Real structure and schematic implementation in Cadence with the cells of the proposed macromodels a) Modified EWD system, b) Wavesensor.

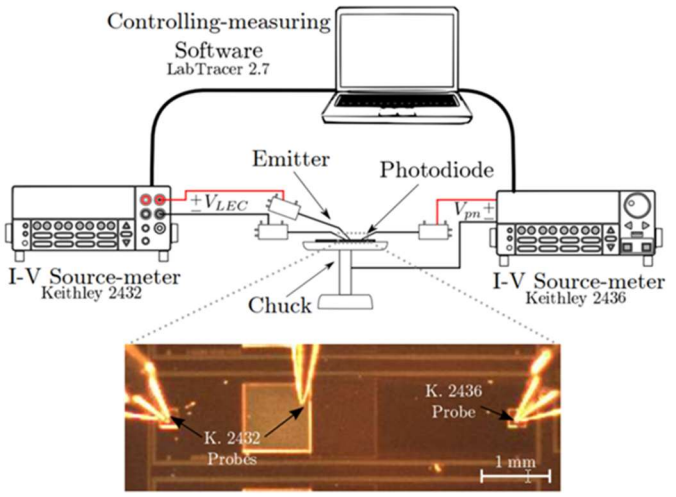

Fig. 6. Schematic of the experimental set-up used to apply/measure simultaneously V_{LEC} and I_{LEC} in the emitter, and V_{pn} and I_{pn} in the sensor.

source-meter. These experiments were executed under consistent lighting conditions. To ensure the reversibility of the system and closely match the conditions for water and air measurements. The selected parameters for the simulation of the devices are summarized in Table 1, The error associated with the photogenerated current measurements conducted using the Keithley 2636B is determined by the instrument's accuracy, which, in the 100 pA range, is ± (0.15% of the reading + 120 fA). This accuracy ensures the reliability of the data collected in our experiments.

The behavior of the wavesensor was simulated under the same conditions as those reported in [17] to verify that the Verilog-A generated model replicated the same results. DC and noise simulations were also performed for the EWD to estimate the limits in both bandwidth for the LEC and noise current in the sensing branch. The schematic simulated in the Cadence environment and the physical structure of the devices can be seen in Fig. 5 a).

Fig. 7 shows the simulated DC behavior of the LEC when varying the applied voltage from 0 to 20 V for three gate areas corresponding to square LECs with sides of 0.5 mm, 1 mm, and 2 mm. It is observed that although the behavior is linear with respect to the voltage, it is nonlinear with respect to the increase in the area; this is consistent with experimental results presented in [18].

Although the LEC has been biased with voltages up to 30 V in a laboratory environment, it is expected to have a completely integrated solution that uses standard and portable power sources such as a battery. Therefore, it is essential to design voltage boosters integrated into the manufacturing process itself, since the standard voltages of portable batteries are not high enough to generate sufficient optical power for the LEC.

To design a voltage booster, it is necessary to determine the minimum breakdown voltage value for the different breakdown mechanisms of the devices inherent to the manufacturing process. In [19], different breakdown mechanisms were measured, and it was found that the lowest breakdown voltage is around 20 V. At 15 V, the power consumption varies from

TABLE I
SUMMARY OF DEVICE SIMULATION PARAMETERS

Parameter	Value	Units
Waveguide Length	0.1	cm
Waveguide Attenuation	2.25	dB/cm
LEC Area	{0.25; 1; 4}	mm²
Photodiode Responsivity	0.2	A/W
Photodiode Area	2.47	mm²
Wavesensor Channel Length	10	µm
Wavesensor Area	2.33	µm²

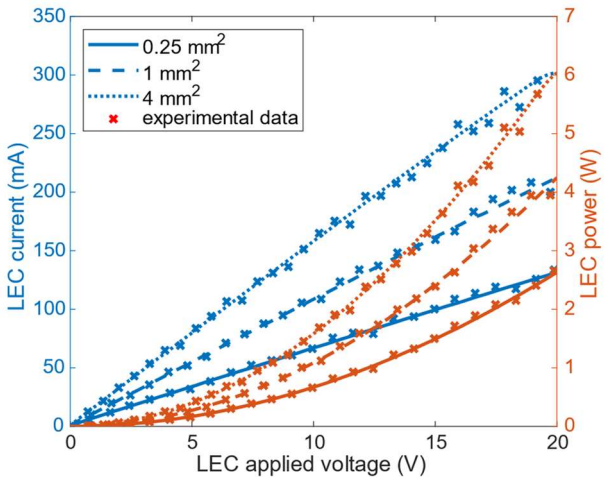

Fig. 7. Comparison of simulated and experimental DC LEC current and power as functions of applied LEC voltage and gate area.

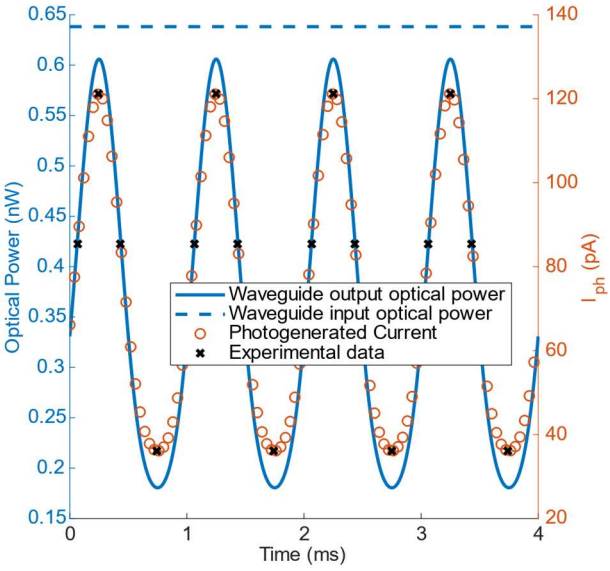

Fig. 8. EWD transient simulation, the photogenerated current, the input and output optical power are shown; the refractive index varies sinusoidally between 1 and 1.47 with a period of 1 ms.

1.5 W to 3.5 W for square LECs with areas ranging from 0.25 mm^2 to 4 $mm^{2,}$ according to Fig. 7. This can be a significantly high consumption and may reduce the system's autonomy. To address these issues later on, the design of a voltage booster and a PWM modulator is illustrated, which can help supply and control electrical power delivered to the EWD.

The EWD is expected to be used to measure changes in the refractive index of a substance present in the waveguide aperture. To analyze the effect of these changes on the photogenerated current, a transient simulation was performed by varying the refractive index and biasing the LEC with a voltage of 15 V and defining a responsivity in the photodiode of 0.2 A/W; the simulation results can be seen in Fig. 8.

It was observed that the photogenerated current by this device for this range of variation is between 36 pA to 121 pA, consistent with experimental results presented in [1], which is quite restrictive and demanding for a readout circuit since the currents are very low, hence the need to design new sensors like the wavesensor that can provide gain and the design of low noise current readout circuits.

One of the main drawbacks of these types of unconventional emitters is that the optical emission power is relatively low, resulting in photogenerated currents in the sensors on the order of picoamperes. Therefore, it is essential to simulate the noise introduced by each component of the electrophotonic system.

Noise simulations were performed with the following parameters: an area of 1 mm^2 for the LEC, an area of 2.47 mm^2 for the photodiode, a waveguide length of 0.1 cm, and a bias voltage of 15 V for both the photodiode and the LEC. Subsequently, the power noise integrals were calculated for a bandwidth of 1 kHz, revealing a total noise current of 135 fA rms referred to the photodiode branch. Fig. 9 shows the percentage contribution of the primary noise sources in the electrophotonic system, primarily the shot noise of the photodiode, the shot noise of the light emitted by the LEC, and to a lesser extent, the resistor's thermal noise.

AC simulations were performed, varying the device area. It was observed that as the area increases, the capacitance increases, but at the same time, the equivalent resistance decreases, varying the bandwidth from 25 MHz to 5 MHz for areas ranging from 0.25 mm^2 to 4 mm^2, as can be seen in Fig. 10. Although it is of interest to know the bandwidth that the device can achieve, this value is not a critical parameter because it is expected to operate in low-frequency ranges for sensing signals coming from variations in the refractive index.

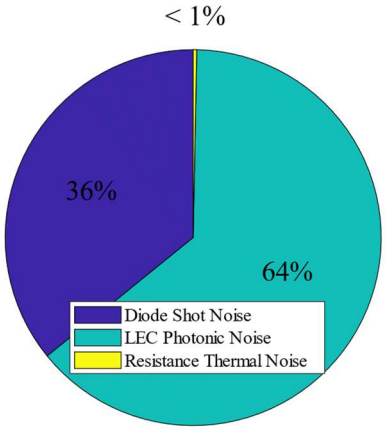

Fig. 9. Percentage contribution of the primary noise sources referred to the photodiode current; the total noise was 135 fArms.

To examine the behavior of the wavesensor model, the simulated sensor was biased with a V_{gs} voltage of -5 V. Meanwhile, the V_{ds} voltage and the input optical power to the sensor were varied, using the optical power value characterized in finite element simulations [17]. For each of these values, the corresponding I_{ds} curve was obtained. Fig. 11 illustrates the relationship between the sensor's gain, the operating point, and the input optical power.

IV. CMOS Circuitry and Electrophotonic Simulations

As observed in Fig. 7, the LEC requires high turn-on voltages and has considerable power consumption; with these factors in mind and considering a fully integrated design that takes advantage of the compatibility of these unconventional light emitters with a standard CMOS process, the circuit of Fig. 12 was designed. This circuit is composed of a current-starved ring oscillator (CSRO), which is a clock generator whose frequency is controlled externally, a four-phase generator, a four-phase Dickson charge pump which elevates the 5 V standard input voltage of the 2.5 µm process used to a higher voltage of 10 V, a pulse width modulator with variable frequency and duty cycle, and finally a current readout circuit which is a current integrator.

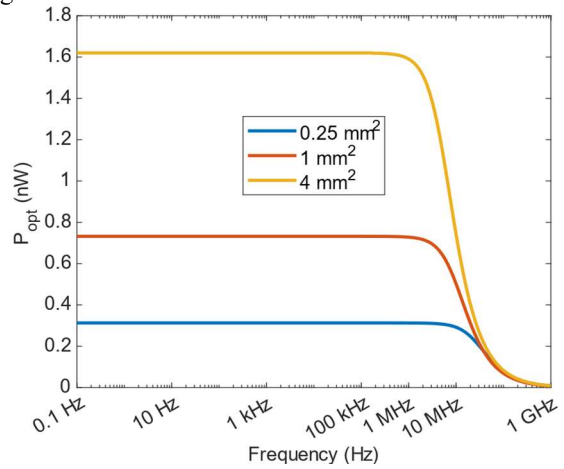

Fig. 10. Simulated AC response of the optical power emitted by the simulated LEC for different areas and a polarization voltage of 15 V.

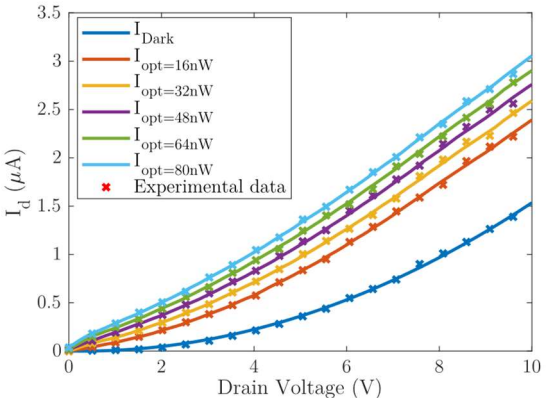

Fig. 11. Wavesensor DC curves for various polarization points and input optical power. The 'x' markers represent results from finite element simulations using SILVACO-Atlas as reported in [17], while the solid lines depict the macromodel simulation.

To increase the voltage, a 3-stage, 4-phase Dickson charge pump was designed as described in [14]; this configuration uses pass transistors instead of diodes, which is typical in conventional 2-phase Dickson charge pump configurations [20].

By doing so, losses introduced by diodes or transistor diode-connected devices are avoided. The load requirements can be derived from Fig. 7; the designed LEC has an area of 0.5 mm^2 and is expected to be polarized with 10 V, so a minimum current of 53.5 mA must be supplied. For a Dickson charge pump, the relationship between the output voltage and the input voltage is:

$$V_{out} = V_{DD} + N\left(\left(\frac{1}{1+k_c}\right)V_\varphi - V_F - \frac{I_{out}}{(C+k_c)f}\right) - V_F \quad (10)$$

Where N is the number of stages (3), C is the capacitance per stage (5.84 nF), V_φ is the clock signal amplitude (5 V), V_F is the voltage drop across the pass transistor (0.3 V), I_{out} is the output current, and f is the frequency of the clock signal which can be adjusted through the CSRO. For an oscillation frequency of 6 MHz, a design output voltage of 13 V is obtained, the simulated output voltage was 10 V which is less than expected but enough and can be attributed to incomplete charge transfer.

The proposed circuit was simulated in Cadence, using as load the EWD system simulated with the Verilog-A models proposed in this paper, the result of the electrophotonic simulation can be seen in Fig. 13. Initially, the charge pump is turned on. However, the LEC is turned off by the PWM, the charge pump output voltage rises and takes around 3 µs to establish around 16 V; at 5 µs, the PWM connects the LEC, and the charge pump decreases until 10 V and supplies current to the LEC constantly. The emitted optical power is around 0.3 nW, and the photodiode current is around 70 pA.

In addition, a capacitive transimpedance amplifier was designed to read the signal from the photodiode, a singled-ended folded cascode OTA, and a feedback capacitance of 100 fF was used; the integration time was 0.5 ms. The output voltage for a capacitive transimpedance amplifier at the end of the sample time is given by (11).

$$V_{out}(T_s) = -\frac{1}{C_f}\int_0^{T_s} I_{in}(t)\,dt \quad (11)$$

Fig. 14 shows the results from the simulation; the refractive index was varied sinusoidally from 1 to 1.47 with a period of 25 ms when a voltage of 10 V was applied to the LEC and the photodiode. The photodiode current varies from 34 pA to 60 pA, the integrator output varies from 163 mV to 145 mV, there is a gain and offset error, it was observed that it is necessary to design a better readout circuit with a lower offset. Additionally, due to the feedback capacitance being comparable to the parasitic capacitances of the transmission gates, undesired effects are introduced due to charge injection. However, it is demonstrated how both the electrophotonic system and the associated CMOS circuitry could be successfully simulated.

V. CONCLUSIONS

This work presents various macro-models for an electrophotonic platform based on LECs as light sources, implemented using Verilog-A. The models encompass optical and electrical behaviors, enabling comprehensive simulations of electrophotonic circuits based on LECs in Cadence Software. Look-up tables are employed to easily update the behavioral characteristics to account for the variability between LECs.

AC, DC, transient, and noise simulations were conducted to validate the model's performance. The obtained responses were consistent with available experimental data for these devices. The DC curves illustrate that LECS require high turn-on voltages and exhibit considerable power consumption. Despite these challenges, the LEC's compatibility with standard CMOS manufacturing processes renders it a promising component for fully integrated systems. Developing models like the ones presented in this work is crucial for achieving a fully integrated platform.

The study also underscored the significance of noise analysis in the design of these systems. The primary noise sources in the electrophotonic system were identified as the shot noise of the photodiode, the shot noise of the light emitted by the LEC, and to a lesser extent, the thermal noise of the resistors. The results represent a contribution to the advancement of the cutting-edge field of electrophotonics, as they show a step-forward towards the expansion of this technology for broader applications.

Future work should focus on enhancing the system's sensitivity and developing integrated readout circuits capable of detecting low currents. It will be critical to explore the development of new sensors, such as the wavesensor, which can provide gain, and design low-noise current readout circuits to address these objectives.

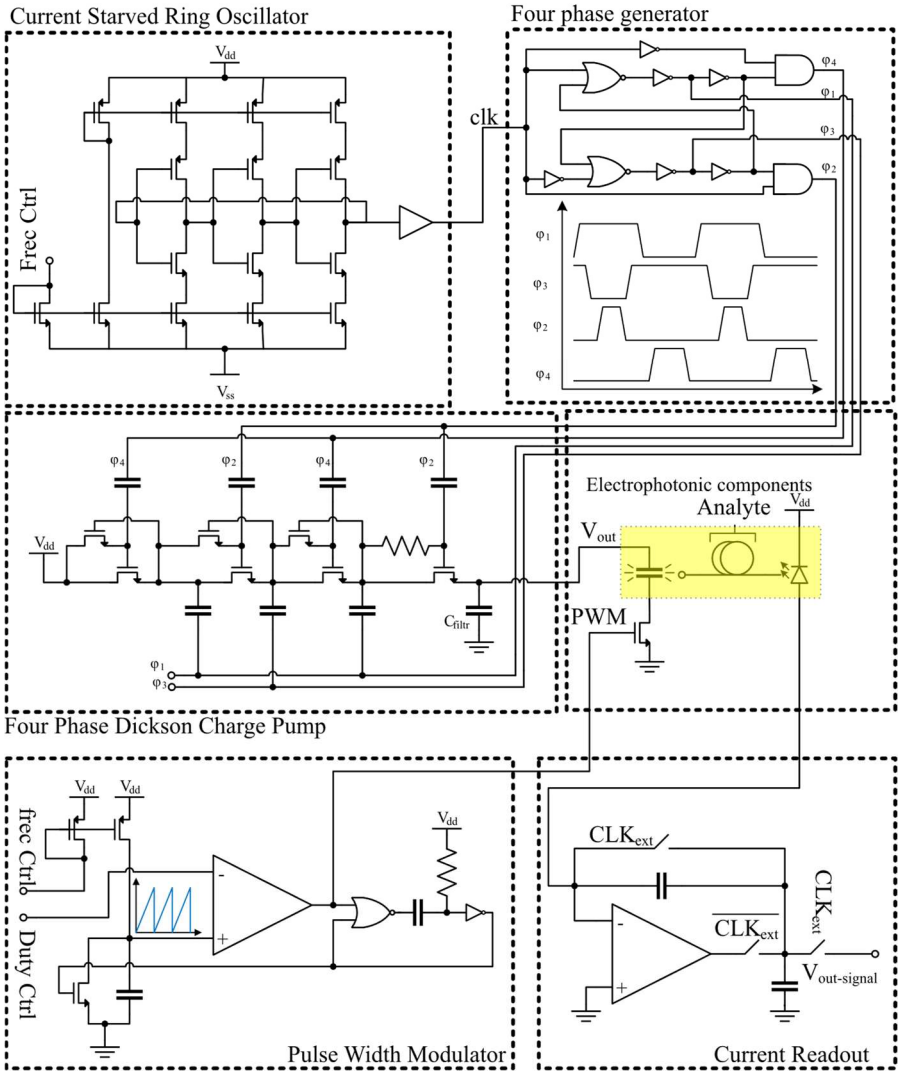

Fig. 12. Structure of the electro-photonic circuit simulated in Cadence, which includes both the control stage of the LEC and the readout circuit

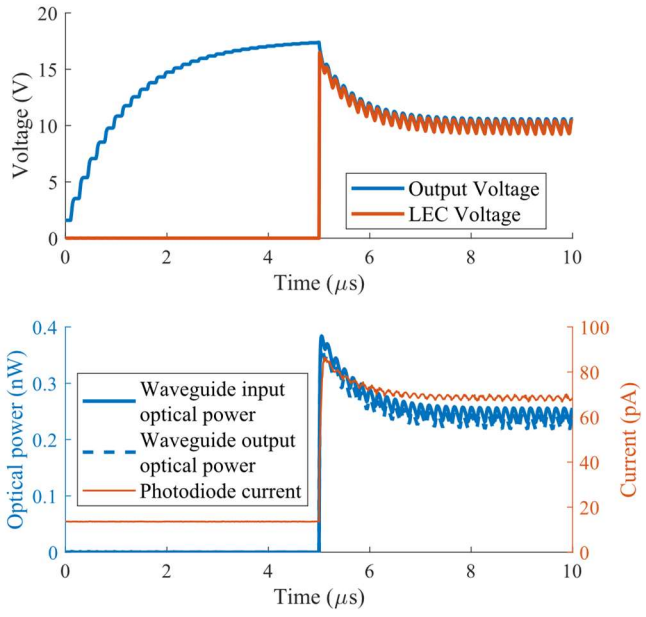

Fig. 13. Transient simulation of the charge pump using as load the EWD system.

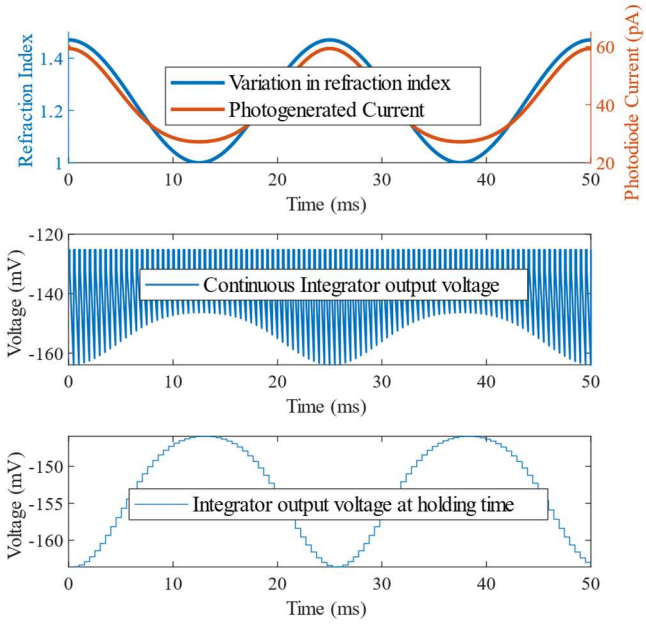

Fig. 14. Transient simulation results of the readout circuit using an integration time of 0.5ms.

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