An Area-Aware Figure of Merit for Improved State-of-the-Art Comparison of Analog-to-Digital Converters

Mauricio Velazquez-Diaz, Victor R. Gonzalez-Diaz, *Senior Member, IEEE*, and Guillermo Espinosa Flores-Verdad

***Abstract*—This paper introduces a new Figure-of-Merit (FoM) for Analog-to-Digital Converters (ADCs) that integrates silicon area alongside the traditional metrics of resolution, bandwidth, and power dissipation. As technology scaling and system-on-chip integration make area efficiency a critical design constraint, the established Walden and Schreier FoMs provide an incomplete comparison of state-of-the-art performance. The proposed Area-Aware FoM (FoM_A) enables a more integrated and equitable benchmarking by directly quantifying the trade-off between dynamic performance and physical implementation cost. The validity and utility of the FoM_A are demonstrated through a re-evaluation of 40 published ADCs, revealing significant shifts in architectural ranking and offering designers a more relevant metric for advanced technology nodes.**

Link to graphical and video abstracts, and to code:
https://latamt.ieeer9.org/index.php/transactions/article/view/10640

***Index Terms*—Figure-of-Merit, Analog-to-Digital Converters, Area, Resolution, Bandwidth, Power dissipation.**

I. Introduction

ANALOG-TO-DIGITAL CONVERTERS (ADCs) are critical components in modern communication, instrumentation, and mixed-signal processing systems. To objectively evaluate and compare their performance, the community has adopted Figures of Merit that encapsulate the fundamental trade-offs between resolution, speed, and power consumption. The two most widely used metrics are the Walden FoM (FoM_W) [1] and the Schreier FoM (FoM_S) [2], respectively defined as:

$$\text{FoM}_W = \frac{P}{2^{ENOB} \cdot f_s} \tag{1}$$

$$\text{FoM}_S = SNDR + 10\,log_{10}\left(\frac{BW}{P}\right) \tag{2}$$

where P is the power dissipation, $ENOB$ the effective number of bits, f_s the Nyquist sampling rate and $SNDR$ the signal-to-noise-and-distortion ratio. While the former is predominantly used to benchmark low-power, moderate-bandwidth ADCs, the latter is favored for high-resolution converters such as $\Sigma\Delta$ modulators. However, both metrics share a fundamental limitation: they omit the silicon area occupied by the circuit, a parameter that has become critical in scaled CMOS technologies and highly integrated Systems-on-Chip (SoCs).

Extensions to these classic FoMs have been proposed to incorporate the integration area. Prior works, such as those surveyed by Jonsson [3], include "Class C" FoMs where area A multiplies power in the numerator (e.g., $(P \cdot A)/(2^{ENOB} \cdot f_s)$). Sauerbrey et al. [4] employed a similar metric ($F = (10^{(DR-1.78)/20} \cdot BW)/(P \cdot A)$) to evaluate very-low-voltage $\Sigma\Delta$ modulators. In the image sensor domain, Kwon and Murmann [5] introduced a FoM normalizing the $P \cdot A$ product with dynamic range and conversion time. Nevertheless, these approaches are inefficient for universal comparison; they either favor a specific ADC type or fail to capture a balanced correlation among the four key variables: resolution, bandwidth, power, and area. This introduces bias when comparing diverse architectures or implementations across different technology nodes.

The trend toward SoCs integrating multiple functions (sensors, processing, RF) demands analog and data converter blocks that optimize not only dynamic performance but also physical footprint. A FoM ignoring this parameter may favor designs with excellent power and speed figures but inefficient layouts, making them less attractive for large-scale integration. This limitation becomes particularly relevant in application-driven systems such as wearable sensors and non-invasive health-monitoring devices, where resolution, bandwidth, power consumption, and silicon area must be jointly optimized to enable compact, energy-efficient, and scalable implementations, as discussed in [6]. In such domestic and industrial applications, an appropriate FoM directly impacts integration density, battery lifetime, and overall cost, motivating the explicit inclusion of silicon area when benchmarking ADC architectures intended for highly integrated systems.

This work proposes a new Figure of Merit that incorporates silicon area in a balanced and well-founded manner, alongside resolution, bandwidth, and power. The resulting metric enables a fair and comprehensive comparison across ADC architectures – from SAR and pipeline to $\Sigma\Delta$ – regardless of whether they are optimized for high resolution or low power.

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II. The Proposed Area-Aware Figure of Merit

A. Noise-based Motivation: Resolution as Amplitude Precision

A fundamental way to quantify the resolution of an ADC is through the root-mean-square (RMS) error in amplitude. For an ideal N-bit uniform quantizer with full-scale range V_{FS}, the quantization step is [7]

$$\Delta = \frac{V_{FS}}{2^N} \tag{3}$$

Under the standard uniform quantization noise model, the quantization error is approximated as a white random variable uniformly distributed in $[-\Delta/2, \Delta/2]$, yielding an RMS value

$$\sigma_q = \frac{\Delta}{\sqrt{12}} = \frac{V_{FS}}{2^N\sqrt{12}} \tag{4}$$

In practice, non-idealities increase the error beyond the ideal quantization noise; therefore, it is customary to replace N by the effective number of bits ENOB, which captures the measured resolution. From (4), a natural *amplitude-precision* metric can be defined as the inverse of the RMS error

$$\Pi \triangleq \frac{1}{\sigma_e} \propto 2^{\mathrm{ENOB}} \tag{5}$$

where σ_e denotes the effective RMS error (including quantization and non-ideal error contributions). Equation (5) provides a direct physical rationale for using 2^{ENOB} as a resolution factor: each additional effective bit halves the RMS error and thus increases amplitude precision proportionally to 2^{ENOB}.

B. Performance Rate: Combining precision and bandwidth

An ADC ultimately delivers *time-varying* information about an analog signal. For signals occupying bandwidth BW, a first-order measure of *delivered performance per unit time* is obtained by scaling amplitude precision by the characteristic signal rate. Thus, we define a precision-rate performance measure as

$$\mathcal{S} \triangleq \Pi \cdot BW \propto 2^{\mathrm{ENOB}} \cdot BW \tag{6}$$

This expression captures two essential and independent requirements: (i) *how accurately* the amplitude can be represented (precision, 2^{ENOB}) and (ii) *how fast* the relevant information evolves (bandwidth, BW).

C. Resource Efficiency with Area and Power

The practical implementation of an ADC incurs two dominant and complementary costs: energy consumption and silicon area. Power P quantifies the energy cost per unit time, while area A represents the physical cost (silicon budget) and directly impacts integration density, yield, and system-level scalability. Therefore, an efficiency metric that evaluates delivered precision-rate per consumed resources can be written as

$$\eta \triangleq \frac{\mathcal{S}}{A \cdot P} = \frac{2^{\mathrm{ENOB}} \cdot BW}{A \cdot P} \tag{7}$$

Finally, to obtain a logarithmic figure that is convenient for comparison across orders of magnitude, the proposed Area-Aware Figure of Merit is defined as

$$\mathrm{FoM_A} = 10\log_{10}\left(\frac{2^{\mathrm{ENOB}} \cdot BW}{A \cdot P}\right) \tag{8}$$

D. Consistency with Classical FoMs (Walden and Schreier)

The proposed $\mathrm{FoM_A}$ can be related to classical FoMs to demonstrate consistency.

1) Relation to Walden FoM: The Walden FoM is typically expressed as Equation 1. Rearranging this equation yields

$$\frac{2^{\mathrm{ENOB}} \cdot f_s}{P} = \frac{1}{\mathrm{FoM_W}} \tag{9}$$

As is known, signal bandwidth is proportional to sampling frequency (e.g., Nyquist sampling $f_s \approx 2BW$ or more generally $BW \propto f_s$), then

$$\frac{2^{\mathrm{ENOB}} \cdot BW}{P} \propto \frac{1}{\mathrm{FoM_W}} \tag{10}$$

and the proposed metric becomes the inverse Walden efficiency *penalized by area*:

$$\frac{2^{\mathrm{ENOB}} \cdot BW}{A \cdot P} \propto \frac{1}{A \cdot \mathrm{FoM_W}} \tag{11}$$

Thus, $\mathrm{FoM_A}$ extends the Walden concept by explicitly incorporating silicon occupation as an additional system-level constraint.

2) Relation to Schreier FoM: The Schreier FoM is often written as Equation (2). Using the standard approximation $SNDR \approx 6.02\,\mathrm{ENOB} + 1.76$, the proposed $\mathrm{FoM_A}$ in (8) can be expanded as

$$\mathrm{FoM_A} = 10\log_{10}\left(\frac{BW}{P}\right) + 10\log_{10}\left(2^{\mathrm{ENOB}}\right) - 10\log_{10}(A) \tag{12}$$

or equivalently

$$\mathrm{FoM_A} = 10\log_{10}\left(\frac{BW}{P}\right) + 3.01\,\mathrm{ENOB} - 10\log_{10}(A) \tag{13}$$

This shows that $\mathrm{FoM_A}$ preserves the energy–bandwidth structure of Schreier but adds an explicit area penalty. In addition, the resolution term in $\mathrm{FoM_A}$ is tied to an amplitude-precision (inverse RMS error) viewpoint, which explains why it scales with 2^{ENOB} rather than $2^{2\cdot\mathrm{ENOB}}$ (which is more naturally associated with power-based ratios).

E. Comparison with Previous Works

To compare the proposed formulation with previously reported FoMs that consider area, the metric defined in Eq. 7 can be rewritten in the general form

$$\eta = \frac{\text{Performance}}{\text{Resource cost}} \tag{14}$$

If the expressions reported in [3], [4], and [5] are recast under this same framework:
The Jonsson formulation can be written as

$$\eta_{Jonsson} = \frac{1}{FoM_{Jonsson}} = \frac{2^{\mathrm{ENOB}} \cdot f_s}{P \cdot A} \tag{15}$$

Since, for a broad class of ADCs, $f_s \propto BW$, it follows that

$$\eta_{Jonsson} \propto \frac{2^{\mathrm{ENOB}} \cdot BW}{P \cdot A} \tag{16}$$

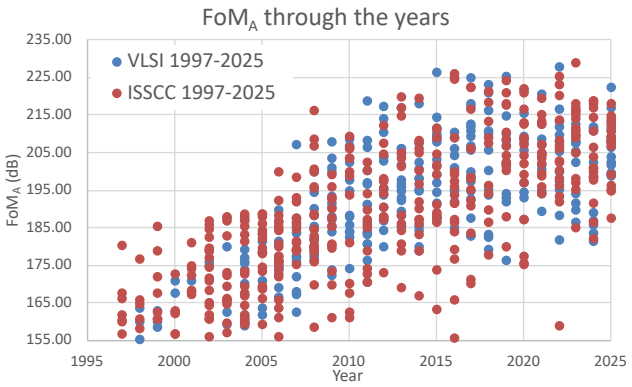

Fig. 1. Evolution of the proposed FoM with publication year, based on data from ISSCC and VLSI Symposium, highlighting long-term efficiency trends and recent saturation behavior.

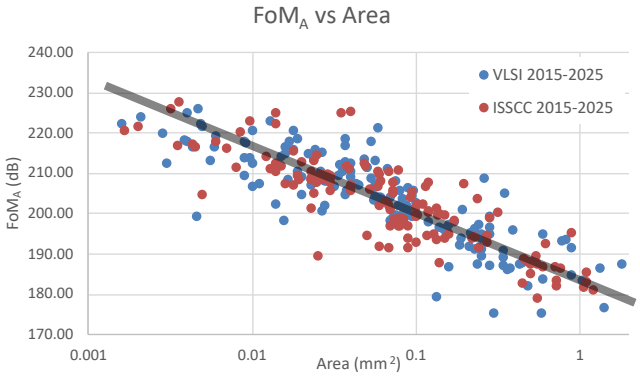

Fig. 2. Relationship between the proposed FoM and ADC core area for recent designs, illustrating the impact of silicon footprint on overall efficiency.

The Sauerbrey expression is

$$\eta_{Sauerbrey} = FoM_{Sauerbrey} = \frac{10^{(DR-1.78)/20} \cdot BW}{P \cdot A} \quad (17)$$

Using the approximation $DR \approx 6.02\,ENOB + 1.76$, is obtained

$$\eta_{Sauerbrey} = \frac{2^{\text{ENOB}} \cdot BW}{P \cdot A} \quad (18)$$

And finally, for Kwon-Murmann it has

$$\eta_{Kwon} = \frac{1}{FoM_{Kwon}} = \frac{10^{(DR-1.78)/20}}{P \cdot Ts \cdot A} \quad (19)$$

Knowing that $Ts = 1/f_s$ and the equivalencies that have already been presented for f_s and DR

$$\eta_{Kwon} \propto \frac{2^{\text{ENOB}} \cdot BW}{P \cdot A} \quad (20)$$

It can be observed that they converge to a form similar to the one proposed in this work. However, this comparison also makes the limitations of each prior formulation more evident. In Jonsson's case, the use of f_s instead of BW makes the metric inherently oriented toward Nyquist-rate ADCs. In addition, since the expression is inversely proportional to the FoM structure adopted in this work, it is more naturally interpreted as resource cost/performance, rather than as a direct efficiency metric.

In Sauerbrey's formulation, the use of DR instead of $SNDR$ (or, equivalently, ENOB) weakens the rigor of the resolution term. Furthermore, this formulation is more closely associated with $\Sigma\Delta$ converters operating under reduced dynamic range conditions.

Finally, the Kwon–Murmann expression again relies on f_s and DR, and is also defined in an inverse form with respect to the efficiency-oriented structure considered here.

Moreover, the proposed formulation is expressed on a logarithmic scale, which makes comparisons more suitable when variables span different orders of magnitude. This is particularly important when benchmarking ADCs of different types and targeting different applications.

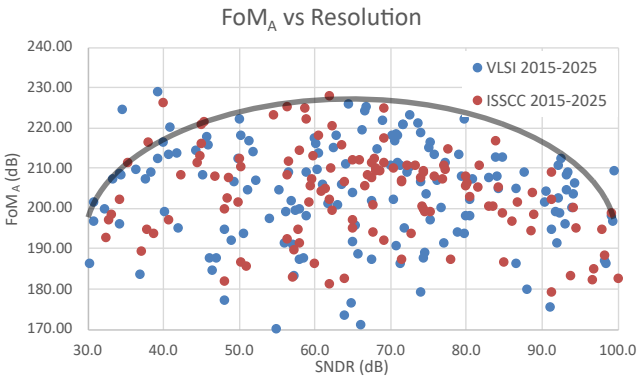

Fig. 3. Proposed FoM as a function of ADC resolution (SNDR), showing the characteristic performance envelope and the trade-off between accuracy and resource cost.

F. Key Mathematical Properties (Validity Checks)

The proposed FoM$_A$ in (8) satisfies basic desirability properties for a comparative metric:

- **Monotonicity:** FoM$_A$ increases with higher ENOB or BW, and decreases with higher P or A, reflecting the intended "higher is better" behavior.
- **Separability:** In logarithmic form, contributions from resolution, bandwidth, power, and area are additive, equation (12), enabling clear interpretation of trade-offs.

III. Analysis and Comparison with the State-of-the-Art

The effectiveness and necessity of the proposed Figure of Merit are demonstrated through a statistical analysis of published ADC data spanning nearly three decades, as compiled from major integrated circuits conferences [8]. The FoM$_A$ is evaluated against three fundamental axes: technological progression, physical implementation size, and achieved resolution. As shown in Fig. 1, the metric tracks the expected historical improvement in design efficiency with CMOS scaling, but also reveals a distinct plateau in recent years. Crucially, Fig. 2 validates the core premise of this work, demonstrating

a strong inverse correlation between the FoM_A and the active silicon area. This directly rewards area-efficient layouts and penalizes designs that achieve performance through brute-force sizing, a critical assessment for modern SoCs.

The most significant insight from the FoM_A is its balanced treatment of resolution. Fig. 3 plots the FoM_A against resolution (SNDR), revealing a curved performance envelope that peaks for converters with medium-to-high resolution (approximately 10-14 bits).

This characteristic diverges fundamentally from traditional FoMs, which exhibit monotonic bias (e.g., favoring either low-power or high-resolution designs). The declining envelope for very-high-resolution ADCs ($>$14 bits) indicates that the FoM_A correctly captures the substantial overhead—in area, power, or both—required to attain the last increments of accuracy. Consequently, the FoM_A promotes a fairer comparison by comprehensively accounting for the total cost of resources ($A \cdot P$) against the delivered performance ($2^{ENOB} \cdot BW$).

The proposed FoM is rigorously evaluated against the established Schreier FoM and Walden FoM metrics using a comprehensive dataset of state-of-the-art ADCs published between 2017 and 2025, as detailed in Table I. This comparative analysis reveals that the FoM_A introduces a critical recalibration of performance rankings by making the implicit cost of silicon area an explicit factor in the efficiency calculation.

Several designs exemplify how the FoM_A elevates architectures that achieve an exceptional balance across all four parameters. The SAR ADC in [17] (TCAS-II 2022) serves as a prime example. While its traditional FoMs are strong (FoM_W = 2.18 fJ/conv-step, FoM_S = 174.68 dB), its FoM_A of 232.47 dB is the highest in the survey. This results from its outstanding combination of a very low power (18.65 μW) and an extremely compact core area of 0.0013 mm^2, achieving 9.74-bit ENOB at 10 MS/s. Similarly, the SAR ADC in [25] (ISCAS 2023) and the pipeline ADC in [23] (TCAS-I 2023) achieve FoM_A values of 226.71 dB and 225.72 dB, respectively. Both designs combine medium-high resolution ($\sim$10 ENOB) with multi-MHz bandwidths while maintaining power consumption below 55 μW and areas under 0.0033 mm^2. The FoM_A uniquely identifies these works as leading in efficiency, a distinction obscured by their more modest traditional FoM rankings.

Conversely, the FoM_A provides a necessary and sobering counterpoint for high-performance designs that incur significant resource costs. For instance, the high-resolution $\Sigma\Delta$ modulator in [14] (JSSC 2021) achieves a top-tier FoM_S of 183.08 dB due to its 106.5 dB SNDR, but its FoM_A is a more moderate 194.64 dB. This reflects the substantial area (0.27 mm^2) and power (440 μW) required to attain such dynamic range at a low bandwidth. An even starker contrast is presented by the high-speed, high-resolution design in [18] (ISSCC 2022). It boasts an impressive FoM_S of 184.24 dB but an FoM_A of only 191.43 dB, penalized by its high power (15 mW) and large area (0.783 mm^2).

The FoM_A correctly contextualizes these designs as exceptional in a specific domain (resolution) but less optimal from a general resource-efficiency standpoint.

The FoM_A also proves effective in evaluating high-speed, medium-resolution converters prevalent in wireline applications. The pipeline ADC in [19] (VLSI 2022) operates at 1.1 GS/s with 10.43-bit ENOB, achieving a strong FoM_A of 207.77 dB due to its relatively compact area (0.084 mm^2) for its speed class. In contrast, the flash ADC in [36] (ISSCC 2025), despite a groundbreaking 10 GS/s sampling rate and an excellent FoM_W of 22.04 fJ/conv-step, achieves a comparable FoM_A of 214.01 dB. While its area is minuscule (0.009 mm^2), the FoM_A incorporates its high power (21.9 mW) and moderate resolution, offering a balanced assessment of its overall efficiency.

As indicated by the previous comparisons, FoM_A does not arbitrarily disrupt the trends established by Schreier and Walden FoMs, but rather refines them through a more implementation-aware ranking. From a rank-correlation viewpoint, the metric remains aligned with the general performance tendencies of classical FoMs; however, under controlled subgroup comparisons, it provides a clearer discrimination among designs with substantially different area and power penalties. At the same time, a consistent clustering by architecture is preserved, indicating that FoM_A sharpens the comparison within and across architectural classes instead of simply reordering them.

From this extensive dataset, a clear performance stratification for the proposed FoM_A emerges. Designs achieving values between 190 dB and 210 dB represent good, competitive converters that exhibit a sound balance. Values exceeding 210 dB indicate outstanding, state-of-the-art designs that have efficiently balanced the four variables, exemplified by [17], [23], [25], and [45] (VLSI 2025, FoM_A = 220.01 dB). This practical scale provides researchers and designers with an immediately meaningful benchmark.

Fig. 4 provides a visual summary of the state-of-the-art comparison derived from Table I. The set of representative ADCs previously discussed is evaluated using both the conventional Schreier FoM and the proposed Area-Aware FoM. Beyond the overall metric values shown in Fig. 4a–b, further decomposes each FoM into its main contributing terms. For FoM_S, the decomposition highlights a strong dependence on resolution, which dominates the final score and therefore introduces an intrinsic advantage for higher-SNDR designs (Fig. 4c). In contrast, the proposed FoM_A exhibits a more balanced interplay among the four key variables—resolution, bandwidth/speed, power, and area—by explicitly incorporating the silicon footprint (Fig. 4d). As a result, the resolution-driven dominance is mitigated and the area term emerges as a major contributor, enabling a comparison that better reflects implementation efficiency and scalability in modern SoCs.

A major advantage of the proposed FoM_A is that it resolves comparison ambiguities that remain hidden when only classical metrics are used. This is evident in the pair of works [43] and [47]: although they rely on fundamentally different topologies, they report essentially identical Schreier and Walden FoMs, leaving no clear basis to identify which implementation is more optimized. By explicitly accounting for silicon footprint, FoM_A immediately breaks this tie and reveals [43] as the more efficient solution, achieving a higher score primarily because its integration area is nearly five times smaller than that of [47]. The same effect is observed for [33] versus [45]. Their Schreier and Walden figures are very

TABLE I
SUMMARY OF STATE-OF-THE-ART ADC, INCLUDING KEY PERFORMANCE PARAMETERS (SAMPLING FREQUENCY, BANDWIDTH, SNDR, ENOB), RESOURCE METRICS (POWER AND SILICON AREA), AND A DIRECT COMPARISON OF CONVENTIONAL FIGURES OF MERIT (SCHREIER AND WALDEN) WITH THE PROPOSED $\mathrm{FoM_A}$

Ref.	F_s (MHz)	BW (MHz)	SNDR (dB)	ENOB (bit)	Power (μW)	Area ($\mathrm{mm^2}$)	FoM_S (dB)	FoM_W (fJ/conv)	$\mathrm{FoM_A}$ (dB)
JSSC 2017 [9]	11.29	0.02	103	16.82	1120	0.16	175.52	242.47	191.10
CICC 2019 [10]	10	5	57	9.18	24	0.0061	170.19	4.15	222.96
ISSCC 2020 [11]	8	0.024	99.4	16.22	134	0.28	181.93	36.59	196.88
Sensors 2020 [12]	0.01	0.000625	65	10.50	0.09	0.12	163.42	49.55	199.25
TCAS-II 2021 [13]	6	3	52.12	8.37	12.98	0.007	165.76	6.56	220.37
JSSC 2021 [14]	3.50	0.02	106.5	17.40	440	0.27	183.08	63.66	194.64
ISSCC 2021 [15]	6	0.024	100.6	16.42	116	0.07	183.76	27.59	204.13
ISCAS 2021 [16]	400	3.13	45.2	7.22	4550	0.011	133.57	4896.83	189.68
TCAS-II 2022 [17]	10	5	60.4	9.74	18.65	0.0013	174.68	2.18	232.47
ISSCC 2022 [18]	2	1	106.0	17.32	15000	0.783	184.24	45.98	191.43
VLSI 2022 [19]	1100	550	64.55	10.43	15100	0.084	170.16	9.95	207.77
ESSCIRC 2022 [20]	5.12	0.024	106.6	17.42	590	0.36	182.69	70.32	192.96
ISSCC 2022 [21]	5.8	0.02	105.4	17.22	203.5	0.0375	185.32	33.42	206.01
TCAS-II 2022 [22]	1000	500	41.37	6.58	9400	0.06	148.63	98.27	199.28
TCAS-I 2023 [23]	20	10	54.7	8.79	54	0.0022	167.38	6.08	225.72
ICICM 2023 [24]	70	35	46.2	7.38	553	0.0026	154.21	47.36	216.17
ISCAS 2023 [25]	10	5	62.2	10.04	34.06	0.0033	173.87	3.24	226.71
Microelec 2023 [26]	0.01	0.005	57.8	9.31	0.04	0.053	168.77	6.31	211.75
VLSI 2023 [27]	100	50	53.4	8.58	418	0.0072	164.18	10.94	218.03
ESSERC 2024 [28]	5	0.31	76	12.33	31.50	0.0045	175.97	9.77	220.56
APCCAS 2024 [29]	0.128	0.004	60.2	9.71	0.76	0.1476	157.40	114.06	194.73
ISSCC 2024 [30]	5	0.10	94.3	15.37	120	0.02	183.51	14.15	212.47
TCAS-II 2024 [31]	2.56	0.01	101.6	16.58	484	0.65	174.75	246.22	184.95
TCAS-II 2024 [32]	4	0.0039	108.7	17.76	385	0.34	178.76	221.73	188.22
BIOCAS 2025 [33]	0.005	0.0026	57.51	9.26	0.0097	0.158	171.80	3.03	210.18
Integration 2025 [34]	1	0.02	64	10.37	448	0.058	164.50	8460	180.08
TCAS-II 2025 [35]	0.512	0.008	60	9.67	14.90	0.129	147.30	1139.66	185.32
ISSCC 2025 [36]	10000	5000	41.7	6.63	21900	0.009	155.29	22.04	214.01
ISSCC 2025 [37]	2200	1100	45.8	7.32	6930	0.004	157.81	19.77	218.01
ISSCC 2025 [38]	1	0.004	99.6	16.25	12.20	0.029	184.76	19.53	209.46
ISSCC 2025 [39]	1000	500	68.2	11.04	15300	0.0219	173.34	7.28	214.96
ISSCC 2025 [40]	3000	1500	58.8	9.48	32500	0.04	165.44	15.22	209.14
ISSCC 2025 [41]	800	400	40.7	6.47	2890	0.0056	152.11	40.80	213.40
ISSCC 2025 [42]	350	80	70.1	11.35	4870	0.036	172.26	11.64	210.77
VLSI 2025 [43]	1	0.50	91.2	14.86	790	0.023	179.21	26.62	209.12
VLSI 2025 [44]	40	1.25	85.8	13.96	906	0.0035	177.20	22.74	217.98
VLSI 2025 [45]	85	42.50	61.2	9.87	284	0.014	172.95	3.56	220.01
VLSI 2025 [46]	16000	8000	35.3	5.57	19600	0.0139	151.41	25.76	211.45
VLSI 2025 [47]	80	0.25	91.2	14.86	392	0.11	179.25	26.42	202.36
VLSI 2025 [48]	2.56	0.01	86.7	14.11	11.80	0.10	175.98	33.38	201.76

close, making the comparison largely inconclusive; however, $\mathrm{FoM_A}$ clearly favors [45], indicating a more efficient overall trade-off rather than performance driven by a single dominant dimension. Finally, [25] and [39] exhibit similar Schreier FoM values, yet both Walden and $\mathrm{FoM_A}$ consistently favor [25], reflecting superior power efficiency together with a smaller implementation footprint.

Importantly, the purpose of a FoM is not to claim that one work is universally "better" than another—each design targets different specifications and applications.

Fig. 5 plots the proposed $\mathrm{FoM_A}$ for the ADCs listed in Table I, annotated by the corresponding fabrication process (technology node). The purpose of this plot is to verify that $\mathrm{FoM_A}$ does not inherently depend on the technology node itself. In principle, one might expect that more advanced nodes would systematically yield higher $\mathrm{FoM_A}$ values due to scaling benefits; however, the results show that $\mathrm{FoM_A}$ primarily reflects architectural and implementation efficiency rather than process generation.

Interestingly, several of the highest $\mathrm{FoM_A}$ results are reported in 65-nm technologies. This does not imply that 65 nm is intrinsically superior to 28 nm; rather, it indicates that $\mathrm{FoM_A}$

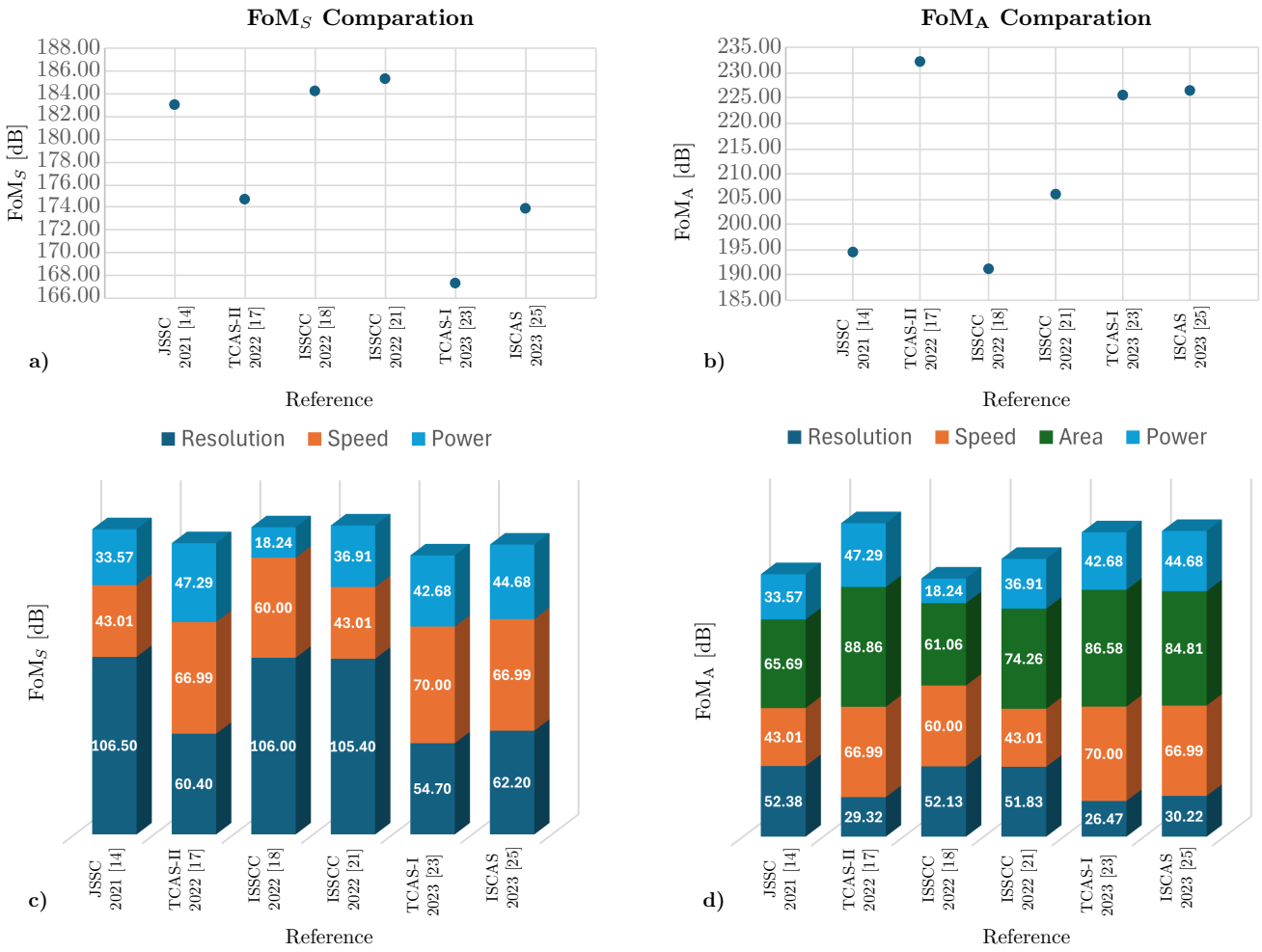

Fig. 4. Visual comparison of SoA ADCs using: a) Schreier FoM (FoM$_S$) for the representative works considered. b) Proposed Area-Aware FoM (FoM$_A$) for the same set of works. c) FoM$_S$ contribution breakdown showing the relative weight of resolution, speed/bandwidth, and power. d) FoM$_A$ contribution breakdown including the explicit area term, illustrating a more balanced contribution of resolution, speed/bandwidth, power, and area.

captures total implementation efficiency, which depends on the interaction between architecture, circuit style, and technology node. For analog-intensive ADCs, mature 65-nm processes often provide a highly favorable compromise among voltage headroom, intrinsic gain, passive-component quality, leakage behavior, matching, and design robustness, allowing optimized solutions with limited auxiliary overhead. By contrast, although 28-nm technologies offer clear benefits in integration density and digital assistance, they also impose reduced supply voltages, stronger device non-idealities, and, in many cases, additional calibration or support circuitry whose area and power costs are not negligible. This perspective is particularly relevant for the coming AI chips, where large numbers of embedded data converters must coexist under tight area and energy constraints. In such systems, a high FoM$_A$ is not only an indicator of converter quality, but also of scalability toward dense mixed-signal integration. Therefore, beyond its use as a general benchmarking metric, FoM$_A$ provides a practical reference for identifying ADC implementations that are better suited to the efficiency demands of future AI-oriented hardware.

IV. Conclusion

This paper has introduced a new Area-Aware FoM for ADCs, defined as $\text{FoM}_A = 10\,log_{10}\left(\left(2^{ENOB}\cdot BW\right)/\left(A\cdot P\right)\right)$, which rectifies a critical omission in established benchmarking metrics by incorporating silicon area as a fundamental fourth parameter alongside resolution, bandwidth, and power. The proposed FoM provides a balanced, symmetric, and architecturally neutral efficiency metric that accurately reflects the total resource cost (power-area product) per unit of information throughput in modern integrated systems. Validation against a comprehensive set of state-of-the-art ADC implementations demonstrates that the FoM$_A$ enables a more equitable and technology-relevant comparison, often reordering performance rankings by rewarding designs that achieve not only low power and high speed but also superior area efficiency. By completing the dimensionality of ADC

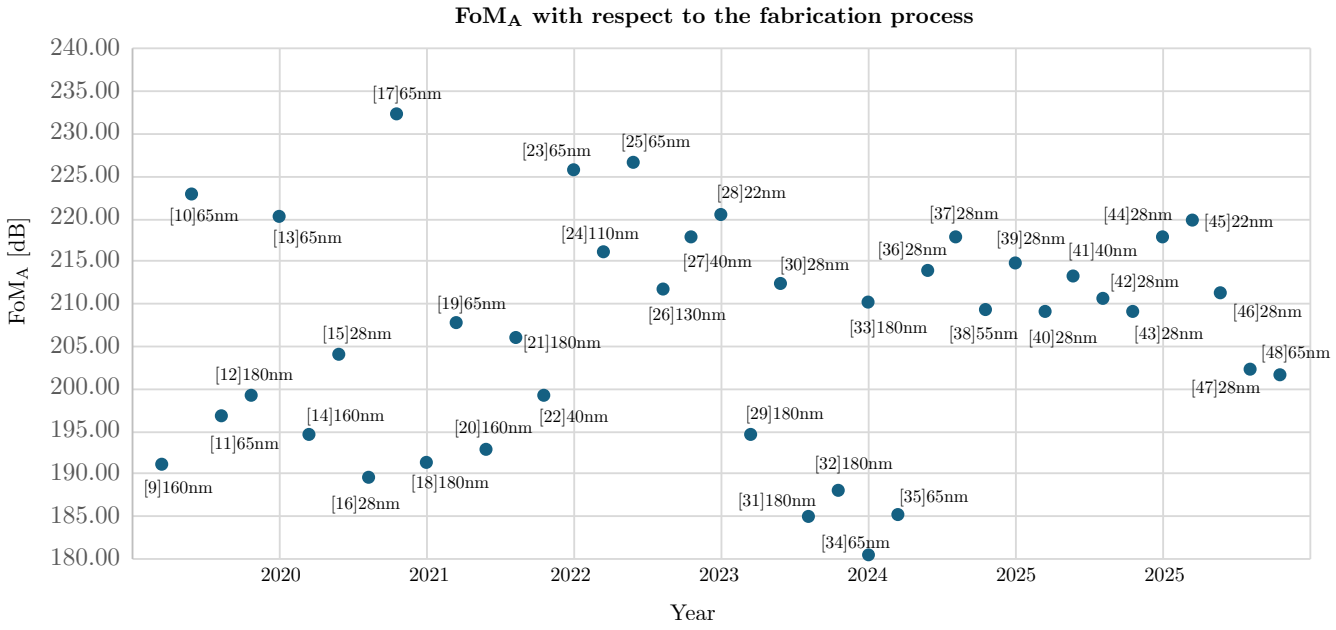

Fig. 5. FoM$_A$ values for the ADCs in Table I, annotated by reported fabrication node, showing a clear trend in recent years toward the use of more advanced technology nodes, while maintaining a relatively stable FoM$_A$ level.

assessment, this work provides designers and researchers with an indispensable tool for guiding architectural exploration and benchmarking in an era where silicon area is a primary constraint.

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