FPGA-Based Control of an Extendable Bidirectional DC-DC Converter for EV Application

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***Abstract*— This paper presents the FPGA-based control of an extendable bidirectional DC-DC converter (E-BDC) for medium and high voltage DC applications. The proposed topology introduces a key structural advantage in which each switch conducts only one inductor current per *n*-stage implementation, significantly reducing conduction losses and improving component utilization. In addition, the converter achieves high voltage gain with reduced device stress and inherent voltage self-balancing, while maintaining continuous low-voltage port current suitable for battery-integrated systems. Steady-state analysis is carried out under synchronous and phase-shifted switching schemes, where phase-shifted operation significantly reduces capacitor voltage ripple and capacitance requirements. A comprehensive small-signal model, including parasitic elements, is developed to characterize the dynamic behavior of the converter under both step-up and step-down modes. The analysis reveals non-minimum phase characteristics in step-up operation, which are explicitly accounted for in the controller design. A model-based PI control strategy is developed to ensure stable operation and satisfactory dynamic response under bidirectional power flow. The control algorithm is implemented on a Zynq-7000 FPGA platform, enabling high-speed and precise real-time operation. The proposed converter is validated using a 700 W, 800 V prototype operating at 50 kHz. Experimental results demonstrate reduced conduction losses, voltage self-balancing, and stable dynamic performance during bidirectional operation.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/10618

***Index Terms* - Bi-directional DC-DC converter, PI Control, Quadratic converter**

I. Introduction

ADVANCES in battery technology and power converters have played a crucial role in establishing battery-powered Electric Vehicles (EVs) [1]. The transition from traditional 400 V to 800 V DC architectures is being adopted to support fast charging, reduce conduction losses, and improve overall system efficiency [2]. In such systems, bidirectional DC-DC converters (BDCs) enable controlled power transfer between the high-voltage traction battery and the low-voltage auxiliary DC bus, while control units are responsible for monitoring and regulating this power flow, as shown in Fig. 1. However, designing such converters to operate efficiently across a wide voltage range presents several technical challenges, including component stress, dynamic stability, and control complexity [3].

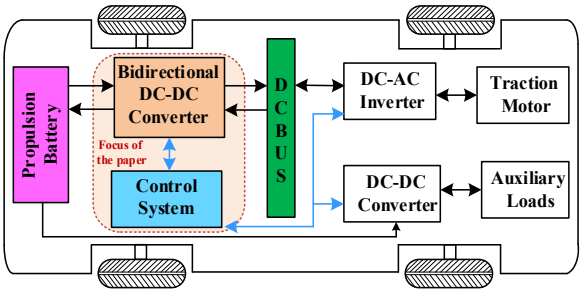

Fig. 1. Functional application block diagram of BDC [2].

Both isolated and non-isolated BDC topologies have been explored in the literature. Isolated BDCs provide galvanic isolation but its utilization is limited due to increased size, higher cost, and increased EMI. Coupled inductor based BDCs improve power density, and enable soft switching [4], [5] to enhance efficiency. But, they are prone to magnetic saturation, and leakage inductance issues. In contrast, non-isolated converters feature simpler and compact designs [6]. To optimize performance in EV applications, switch current and voltage stress must be minimized while achieving high Voltage Conversion Gain (VCG). In addition, the converter should maintain high efficiency over a wide operating range and employ effective control strategies [7].

Several non-isolated BDC topologies are synthesized from conventional synchronous boost-based BDCs, offering different voltage gains through series/parallel input-output configurations [8]-[10]. The VCG of such converters is typically expressed as $k/(1-D)$, where k depends on the topology. However, achieving higher VCG requires operation at large duty ratios, resulting in increased conduction and switching losses. Quasi-Z-source-based BDCs have also been investigated to improve voltage gain; however, they inherently limit the maximum duty ratio to 50%, thereby restricting achievable gain. To overcome these limitations, quadratic converters with gain of $1/(1-D)^2$ was developed, featuring continuous input current and improved gain characteristics [11]-[15]. Despite these advantages, some topologies suffer from increased switch current stress [11] [13], while others require additional passive components to achieve similar gain [14], leading to reduced efficiency. Further improvements using interleaved structures, switched inductor/capacitor cells, and voltage multiplier techniques have been reported [16]-[18]; however, these approaches

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often increase circuit complexity, component count, or control difficulty. Additionally, certain topologies lack a common ground or require a higher number of switches, further complicating practical implementation [17] [19].

In addition to topological structure, the design of an appropriate control strategy is critical for ensuring stable and efficient operation of BDCs. Conventional PI controllers are widely adopted due to their simplicity and ease of implementation [20], [21]. However, their performance degrade under wide operating conditions and parameter variations if not properly designed. To address these challenges, advanced control techniques such as sliding mode control [22], model predictive control [23], intelligent control methods including fuzzy logic control [24], have been investigated. While these approaches offer improved dynamic performance, they involve higher computational complexity and implementation cost, which limit their practical applicability. In addition, dead-beat control techniques have been reported for low-voltage side current regulation [25], providing fast transient response; however, they often lack control of high-voltage side in bidirectional operation. Modified PI-based approaches have also been proposed to enhance robustness [26], but they introduce additional design complexity. Therefore, a trade-off exists between dynamic performance, robustness, computational complexity, and practical implementation.

This paper presents an Extendable Bidirectional DC-DC converter (E-BDC) along with a model-based voltage-mode control framework combined with accurate system modelling and appropriate tuning for both the low-voltage and high-voltage sides. Accordingly, a model-based PI control strategy is developed using the derived small-signal model to ensure stable bidirectional operation, including under non-minimum phase characteristics in step-up mode. Furthermore, the controller is implemented on an FPGA platform, enabling high-speed, real-time control with improved reliability and practical feasibility. Although several quadratic high-gain DC-DC converters have been reported, the proposed bidirectional converter structure with reduced current stress characteristics has not been documented. The key features and contributions of the proposed *n*-stage E-BDC are summarized as follows:

- Novel E-BDC converter architecture
- Inherent inductor current sharing among switches
- Cascaded capacitor-based energy transfer
- Enhanced high voltage conversion gain capability
- Scalable quadratic voltage gain structure
- Continuous low-voltage port current
- Common ground between input and output ports
- Distributed voltage stress across capacitors
- Natural voltage balancing across switches
- Integrated bidirectional power flow capability
- Evaluation of SS and PSS switching strategy
- FPGA-based digital control implementation

II. Operation of Proposed E-BDC Converter

The circuit diagram of the E-BDC with *n*-stages requiring $(n + 1)$ inductors, $(n + 1)$ capacitors, and $(2n + 2)$ switches is shown in Fig. 2. The basic stage of E-BDC ($n = 1$) is comprised of 2 inductors, 2 capacitors and 4 switches. V_L and V_H denote the low-voltage and high-voltage sides, respectively. The analysis is performed for two distinct switching schemes: (i) Synchronous Switching (SS), where the switches S_1 and S_2 (or S_3 and S_4) are turned on and off simultaneously, and (ii) Phase-Shifted Switching (PSS), where S_1 and S_2 are operated with a defined 180° phase shift. The operation of the proposed E-BDC is explained under Continuous Conduction Mode (CCM) during both step-up and step-down modes.

A. Synchronous Switching

1. Step-up mode of operation: Switches S_1 and S_2 are controlled using a duty ratio D_H to enable E-BDC to operate in step-up mode, allowing power flow from low-voltage side to high-voltage side. The equivalent circuits of E-BDC converter in step-up mode, corresponding to State 1 and State 2, are illustrated in Fig. 3(a) and Fig. 3(b), respectively.

State 1 ($t_0 \le t \le t_1$): In this state, when switches S_1 and S_2 are turned on, inductor L_1 is energized by the low voltage source V_L, while inductor L_2 is energized by v_{C1}, as illustrated in Fig. 3(c). The dynamic equations for this state are given in (1). Switches S_1 and S_2 carry current, and i_{L2}, respectively. In contrast to conventional BDC [11], where one of the switches carries current of $(i_{L1} + i_{L2})$, the proposed E-BDC enables current sharing, significantly reducing conduction losses in the switches. Switches S_3 and S_4 experience voltage stresses of v_{C1} and V_H, respectively. The capacitor C_2 delivers the stored energy to the load.

$$L_1 \frac{di_{L1}}{dt} = V_L; \quad L_2 \frac{di_{L2}}{dt} = v_{C1} \tag{1a}$$

$$C_1 \frac{dv_{C1}}{dt} = -i_H - i_{L2}; \quad C_2 \frac{dv_{C2}}{dt} = -i_H \tag{1b}$$

State 2 ($t_1 \le t \le T_s$): When switches S_1 and S_2 are turned off, the stored energy in the inductors is transferred to the high - voltage side through the body diodes of switches S_3 and S_4.

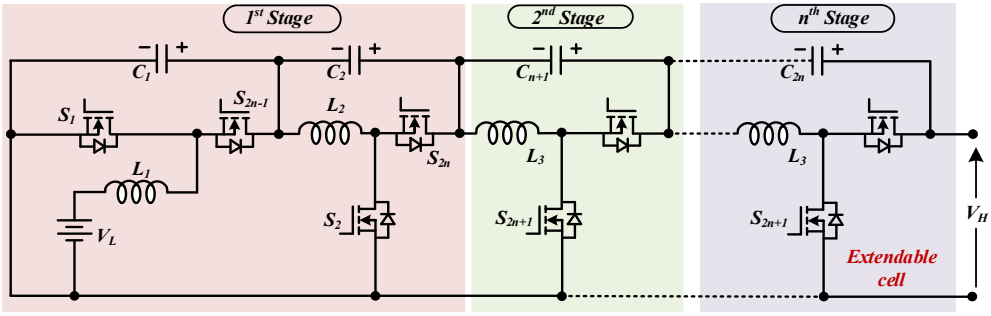


Fig. 2. Circuit diagram of the proposed *n*-stage E-BDC.

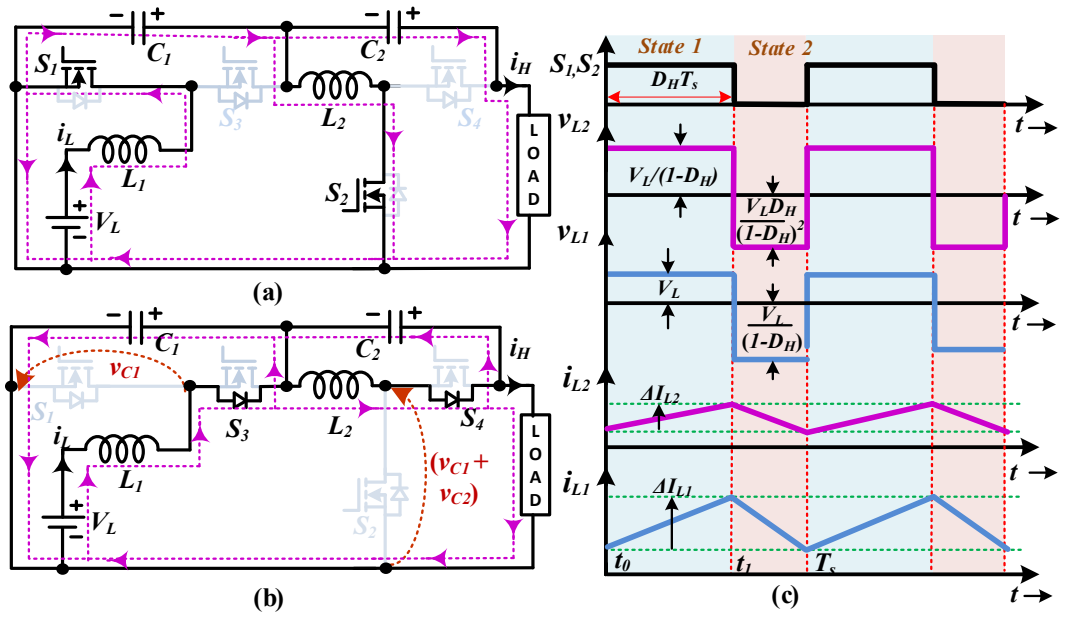


Fig. 3. Equivalent circuits during Step-up operation (a) State 1 (b) State 2 (c) Analytical waveforms.

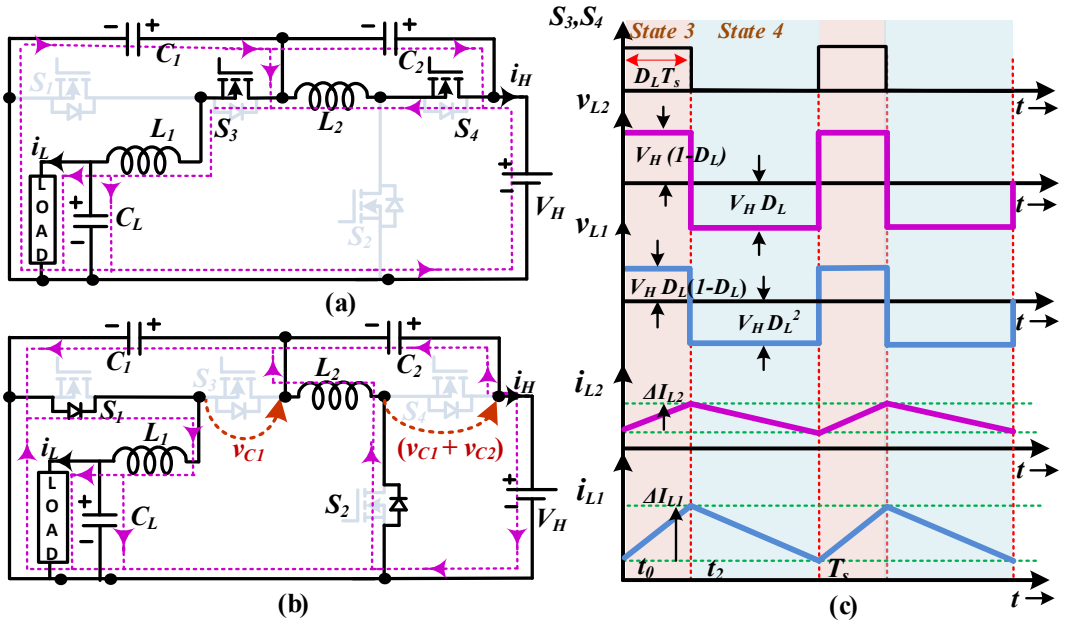


Fig. 4. Equivalent circuits during Step-down operation (a) State 3 (b) State 4 (c) Analytical waveforms.

The equivalent circuit and analytical waveforms for state 2 are shown in Fig. 3(b) and Fig. 3(c), respectively. Switches S_1 and S_2 experience a voltage self-balancing, with voltage stresses of v_{C1} and (v_{C1}+ v_{C2}), respectively as indicated in Fig. 3(b). The voltages across the inductors and the currents through the capacitors are expressed in (2).

$$L_1\frac{di_{L1}}{dt}=V_L-v_{C1};L_2\frac{di_{L2}}{dt}=-v_{C2};V_H=(v_{C1}+v_{C2}) \quad (2a)$$

$$C_1\frac{dv_{C1}}{dt}=(i_{L1}-i_H)\;;\;C_2\frac{dv_{C2}}{dt}=(i_{L2}-i_H) \quad (2b)$$

The steady-state voltages of C_1 and C_2, along with the output voltage, V_H are derived from (1) and (2), as expressed in (3).

$$\langle V_{C1}\rangle=\frac{V_L}{(1-D_H)};\langle V_{C2}\rangle=\frac{V_LD_H}{(1-D_H)^2};\langle V_H\rangle=\frac{V_L}{(1-D_H)^2} \quad (3)$$

In step-up mode of operation, the output voltage of n-stage E-BDC is obtained as $\langle V_{H_n}\rangle=V_L/(1-D_H)^{n+1}$.

2. Step-down Mode of Operation: In the step-down mode of E-BDC, power is transferred from high-voltage side to low-voltage side by controlling switches S_3 and S_4 with a duty ratio D_L. The corresponding equivalent circuits for State 3 and State 4 are illustrated in Fig. 4(a) and Fig. 4(b), respectively.

State 3 ($t_0 \le t \le t_2$): When the switches S_3 and S_4 are turned on, inductors L_1 and L_2 are energized with voltages (v_{C1}-V_L) and (V_H-v_{C1}), respectively. The dynamic equations during this state are given in (4).

$$L_1\frac{di_{L1}}{dt}=(v_{C1}-V_L)\;;\quad L_2\frac{di_{L2}}{dt}=(V_H-v_{C1}) \quad (4a)$$

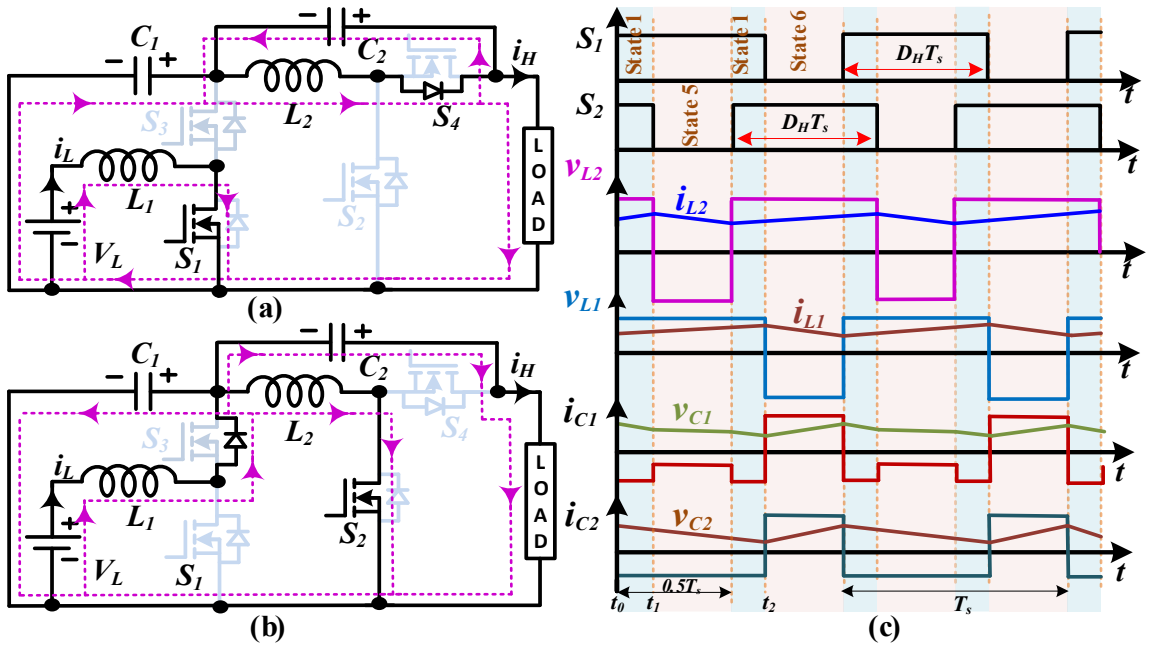


Fig. 5. Equivalent circuits during PSS (a) State 5 (b) State 6 (c) Analytical waveforms.

$$C_1\frac{dv_{C1}}{dt}=(i_H-i_{L1})\;;\quad C_L\frac{dv_{CL}}{dt}=(i_{L1}-i_L) \tag{4b}$$

State 4 ($t_2 \le t \le T_s$): The stored energy of L_2 is delivered to the capacitor C_1 through the body diode of switch S_2, when the switches S_3 and S_4 are turned off. The energy of L_1 is delivered to the low voltage side through the body diode of switch S_1. The analytical waveforms for the state 4 are shown in Fig. 4(c). The equations governing this state are given in (5). From the inductor voltage expressions given in (4a) and (5a), the average voltages across capacitors C_1 and C_2, and output voltage V_L, during the step-down mode of operation are obtained, as given in (6).

$$L_1\frac{di_{L1}}{dt}=-V_L\;;\quad L_2\frac{di_{L2}}{dt}=-v_{C1} \tag{5a}$$

$$C_1\frac{dv_{C1}}{dt}=(i_H+i_{L2})\;;\quad C_L\frac{dv_{CL}}{dt}=(i_{L1}-i_L) \tag{5b}$$

$$\langle V_{C1}\rangle=D_LV_H\;;\ \langle V_{C2}\rangle=(1-D_L)V_H\;;\ \langle V_L\rangle=D_L{}^2V_H \tag{6}$$

The *n*-stage E-BDC achieves the output voltage of $\langle V_{L_n}\rangle=(D_L)^{n+1}V_H$.

B. Phase Shifted Switching

In addition to the synchronous switching scheme, the E-BDC is also analyzed under 180° PSS, where switches S_1 and S_2 are alternately turned on with a phase shift of 180°, introducing a modulation offset within each switching period. The equivalent operating states under this modulation are illustrated in Fig. 3(a), Fig. 5(a) and Fig. 5(b), corresponding to *State 1*, *State 5* and *State 6*, respectively. The analytical waveform associated with this switching sequence is depicted in Fig. 5(c). *State 1* ($t_0 \le t \le t_1$) is as explained in section II.A.1, where both switches S_1 and S_2 are turned on. This state is followed by *State 5* ($t_1 \le t \le T_s/2$), where S_1 remains on while S_2 is turned off. In this interval, inductor L_1 is energized by the low voltage source V_L, while inductor L_2 partially discharges through the load via the body diode of S_4, as shown in Fig. 5(a). The dynamic equations of this interval are given in (7).

$$L_1\frac{di_{L1}}{dt}=V_L\;;\quad L_2\frac{di_{L2}}{dt}=-v_{C2} \tag{7a}$$

$$C_1\frac{dv_{C1}}{dt}=-i_H\;;\quad C_2\frac{dv_{C2}}{dt}=(i_{L2}-i_H) \tag{7b}$$

In *State 6* ($t_2 \le t \le T_s$), the roles of S_1 and S_2 are reversed (S_2 is turned on and S_1 is off). In this state, inductor L_1 charges capacitor C_1 through body diode of S_3, while L_2 is energized by the capacitor voltage v_{C1} as described by the dynamic equations given in (8).

$$L_1\frac{di_{L1}}{dt}=V_L-v_{C1}\;;\qquad L_2\frac{di_{L2}}{dt}=v_{C1} \tag{8a}$$

$$C_1\frac{dv_{C1}}{dt}=i_{L1}-i_{L2}-i_H\;;\quad C_2\frac{dv_{C2}}{dt}=-i_H \tag{8b}$$

From the dynamic equations under PSS, the average capacitor voltages (C_1, C_2) and output voltage remain identical to SS. However, alternating energization reduces simultaneous charging-discharging stress on the same capacitor. Consequently, C_1 exhibits lower voltage ripple and improved output voltage stability, as experimentally validated in Section V.

III. Component Design and Performance Comparison

A. Component Design:

To facilitate converter design and enable a fair performance comparison, the steady-state voltages, currents, and ripple characteristics of the passive components and semiconductor devices are derived under CCM.

Inductor Design: The inductors L_1 and L_2 are designed to ensure CCM operation with controlled current ripple. The average inductor currents in step-up and step-down modes are given by (9) and (10), respectively.

$$\left.\begin{aligned}\langle I_{L1}\rangle &= \frac{I_H}{(1-D_H)^2};\langle I_{L2}\rangle = \frac{I_H}{(1-D_H)}\Big|_{step-up}\\ \langle I_{L1}\rangle &= \frac{I_H}{D_L^{\,2}};\langle I_{L2}\rangle = \frac{I_H}{D_L}\Big|_{step-down}\end{aligned}\right\} \quad (9)$$

The inductance values are selected based on the allowable peak-to-peak ripple (Δi_{L1}, Δi_{L2}) and switching frequency f_s. Accordingly, the required inductances are obtained as:

$$\left.\begin{aligned}L_1 &\geq \frac{V_L D_H}{f_s \Delta i_{L1}}\Big|_{step-up} \; and \; \frac{V_H D_L^{\,2}(1-D_L)}{f_s \Delta i_{L1}}\Big|_{step-down}\\ L_2 &\geq \frac{V_L D_H}{f_s \Delta i_{L2}(1-D_H)}\Big|_{step-up} \; and \; \frac{V_H D_L (1-D_L)}{f_s \Delta i_{L2}}\Big|_{step-down}\end{aligned}\right\} \quad (10)$$

The ripple currents are typically chosen as 10% of the respective average inductor currents to ensure a trade-off between dynamic response and component size. The converter rating and designed inductance values of L_1 and L_2 are given in Table I. In the hardware implementation, values of L_1 = 2 mH and L_2 = 12 mH are chosen to ensure reduced current ripple and improved efficiency. For these values, the theoretical peak-to-peak ripple currents are Δi_{L1} = 0.547 A and Δi_{L2} = 0.289 A, which are within acceptable limits. Although the selected inductance values may appear relatively large, they do not represent a limitation of the proposed converter. Instead, they reflect a design trade-off aimed at minimizing current ripple, reducing RMS current, and thereby improving efficiency. If higher ripple (e.g., up to 30% of the average inductor current) is acceptable, the inductance values can be significantly reduced to $L_1 \approx$ 0.416 mH and $L_2 \approx$ 4.17 mH. However, such a reduction increases RMS current and conduction losses, adversely affecting efficiency. Therefore, the chosen inductance values provide a balanced trade-off between performance, efficiency, and component sizing, making the converter suitable for high-gain applications such as electric vehicles and renewable energy systems.

Capacitor Design: The capacitors C_1 and C_2 are designed to maintain the desired voltage levels while limiting the voltage ripple within acceptable bounds. The average capacitor voltages in step-up mode are given by (3). The capacitance values are determined based on the allowable peak-to-peak voltage ripple (Δv_{C1}, Δv_{C2}). Accordingly, the capacitor values are expressed as given in (11).

$$\left.\begin{aligned}C_1 &\geq \frac{i_H D_H (2-D_H)}{f_s (1-D_H)\Delta v_{C1}}\Big|_{step-up} \; and \; \frac{i_L D_L (D_L^{\,2}-1)}{f_s \Delta V_{C1}}\Big|_{step-down}\\ C_2 &\geq \frac{i_H D_H}{f_s \Delta V_{C2}}\Big|_{step-up} \; and \; \frac{i_L D_L (1-D_L)}{f_s \Delta V_{C2}}\Big|_{step-down}\end{aligned}\right\} \quad (11)$$

In practice, the voltage ripple is typically limited to <1% of the respective capacitor voltages to ensure stable operation.

MOSFET Design: The voltage and current stresses of the switches are critical for device selection and reliability assessment of the proposed E-BDC converter. In the proposed E-BDC, only two switches are actively controlled in each mode, while the remaining switches conduct through their body diodes. The current and voltage stress of the switches are given in Table II.

TABLE I
COMPONENT SPECIFICATION

Parameters	*Symbol*	*Rating*
Low and high voltage	V_L and V_H	80 V and 800 V
Rated output power	P_o	700 W
Switching frequency	fs	50 kHz
Inductor ripple current	Δi_{L1} & Δi_{L2}	10% of i_{L1} & 10% of i_{L2}
Inductors (EE core)	L_1 & L_2	2 mH, 20 A &12 mH, 5 A
Capacitor ripple voltage	Δv_{C1} & Δv_{C2}	< 0.5% of v_{C1} & v_{C2}
Capacitors (Electrolytic)	C_1 & C_2	39µF, 400V & 4.7µF, 650V
Switches (MOSFETs)		C2M0040120D

TABLE II
CURRENT AND VOLTAGE STRESS OF MOSFET SWITCHES

Parameters	*Step-up*	*Step-down*
Current of S_1, I_{S1rms}	$\frac{I_H\sqrt{D_H}}{(1-D_H)^2}$	$\frac{I_H(1-D_L)}{D_L^{\,2}}$
Current of S_2, I_{S2rms}	$\frac{I_H\sqrt{D_H}}{(1-D_H)}$	$\frac{I_H(1-D_L)}{D_L}$
Current of S_3, I_{S3rms}	$\frac{I_H}{(1-D_H)^{1.5}}$	$\frac{I_H}{D_L^{1.5}}$
Current of S_4, I_{S4rms}	$\frac{I_H}{(1-D_H)^{0.5}}$	$\frac{I_H}{D_L^{0.5}}$
Voltage of S_1, V_{S1peak}	V_{C1}	V_{C1}
Voltage of S_2, V_{S2peak}	V_H	V_H
Voltage of S_3, V_{S3peak}	V_{C1}	V_{C1}
Voltage of S_4, V_{S3peak}	V_H	V_H

It can be observed that the current stress is distributed among the switches due to the topological structure. This characteristic enables reduced device rating requirements and improved efficiency in both step-up and step-down modes.

B. Proposed E-BDC versus Conventional BDCs:

Table III presents a performance comparison of the proposed converter against conventional BDC topologies, considering VCG, component count, stress levels, and control complexity. Converters with lower switch stress [6], [7] are limited by low voltage gain, which restricts their suitability for high step-up applications such as the targeted 80 V to 800 V operation. In addition, the lack of common ground and control implementation in certain topologies [7], [9] further limits their practical deployment. Topologies that provide enhanced functionality or multiple operating modes [8], [10] improve flexibility but at the expense of increased switch count or higher current stress, which negatively affects efficiency and design simplicity. Similarly, converters designed for low ripple or improved switching characteristics [9], [21] introduce additional passive components or complex control schemes, increasing implementation complexity.

Converters focusing on high VCG [17], [19], [23] achieve

improved gain characteristics; however, this is accompanied by increased component count, higher capacitor voltage stress, or overall circuit complexity, which can adversely impact efficiency and reliability. Although [14] reduces switch count compared to conventional quadratic BDCs, it

TABLE III
COMPARISON WITH CONVENTIONAL CONVERTER TOPOLOGIES

Ref.	Step-up gain	Step-down gain	Switch	Inductor	Capacitor	Diode	Advantages	Disadvantages	Control strategy adopted
[6]	$\frac{1+D_H}{1-D_H}$	$\frac{D_L}{2-D_L}$	4	2	3	0	• Low components • Low switch voltage/current stress	• Limited gain	• PI Controller with dual loop control in MATLAB SISO tool
[7]	$\frac{1}{1-D_H}$	D_L	4	2	4	0	• Low switch voltage stress	• Limited gain • No common ground	• No control mechanism
[8]	$\frac{1+D_H}{1-D_H}$	$2D_L-1$	8	2	2	0	• Different modes of operation possible	• Higher switch count • No common ground	• Type III and integral controllers
[9]	$\frac{1+D_H}{1-2D_H}$	$\frac{D_L}{2-D_L}$	4	2	1	1	• Low current ripple	• No common ground	• PID controller
[10]	$\frac{2}{1-D_H}$	$\frac{D_L}{2}$	4	2	2	0	• Dual input integration	• Higher switch current stress	• Global state observer
[14]	$\frac{1}{(1-D_H)^2}$	D_L^2	3	2	2	2	• The switch count is lower compared to the existing quadratic BDCs	• Uses 2 extra diodes to achieve the quadratic gain	• Non-linear control using input-output feedback linearization
[17]	$\frac{(1+D_H)}{(1-D_H)^2}$	$\frac{D_L^2}{2-D_L}$	4	3	4	2	• Improved VCG	• Increased component count	• No control mechanism
[19]	$\frac{(3-D_H)}{(1-D_H)^2}$	$\frac{D_L^2}{2+D_L}$	6	2	5	0	• Improved VCG • Low switch voltage stress	• Increased component count including switches •	
[21]	$\frac{1}{1-D_H}$	D_L	4	2	2	0	• Achieves zero current switching	• Complex control circuitry	• Power flow and feed forward control
[23]	$\frac{(1+D_H)}{(1-D_H)^2}$	$\frac{D_L^2}{2-D_L}$	5	2	3	0	• Improved VCG	• Higher capacitor voltage stress	• Dead beat controller
Proposed	$\frac{1}{(1-D_H)^2}$	D_L^2	4	2	2	0	• Low switch current stress • Low capacitor voltage stress	• Voltage stress across 2 switches are still V_H	• PI controller in FPGA platform

requires additional diodes to achieve gain enhancement, thereby introducing extra conduction losses. In contrast, the proposed converter achieves a balanced performance trade-off, offering a quadratic voltage conversion gain with only two active switches, while avoiding additional passive components for gain enhancement. It also ensures low switch current stress and reduced capacitor voltage stress, improving efficiency and reliability. Furthermore, the presence of a common ground simplifies practical integration compared to several existing topologies. The advantages of the proposed topology are further supported by the voltage conversion characteristics shown in Fig. 6. As illustrated in Fig. 6(a), the step-up output voltage V_H increases nonlinearly with duty ratio, achieving high voltage gain at moderate duty cycles, thereby avoiding extreme duty operation typically required in conventional converters. Similarly, Fig. 6(b) demonstrates the controlled step-down behavior of V_L, ensuring a wide and stable operating range in bidirectional mode. These characteristics confirm that the proposed converter can achieve the required high conversion ratio without incurring excessive conduction losses or control difficulty. BDC topologies with the same VCG are compared with the

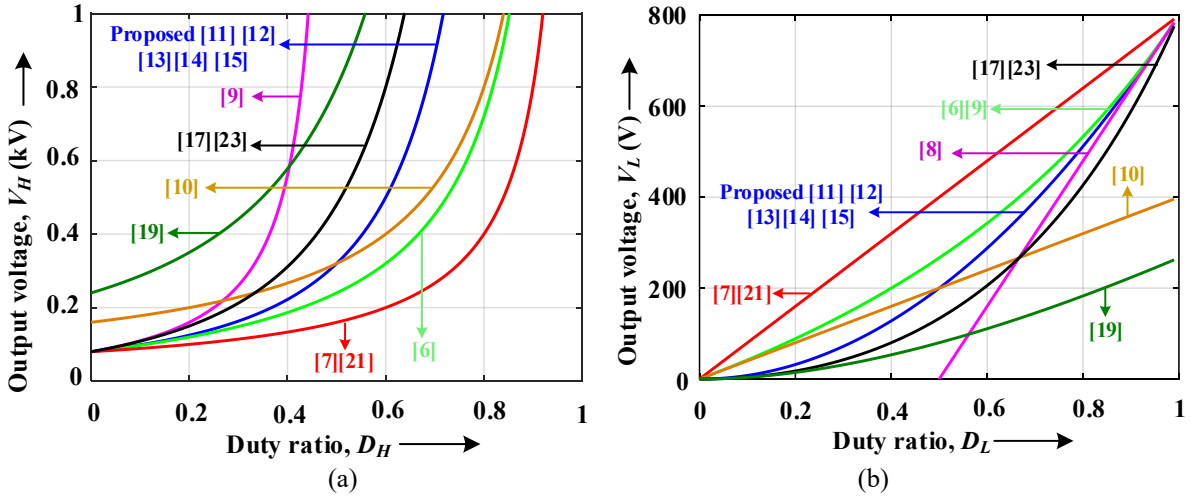


Fig. 6 Output voltage comparison (a) Step-up voltage V_H versus duty ratio D_H (b) Step-down voltage V_L versus duty ratio D_L.

TABLE IV
COMPARISON OF QUADRATIC BDCS WITH VCG=1/(1-D_H)^2

Parameter	Proposed	[11]	[12]	[13]	[14]	[15]	CB
L/C/S/D	2/2/4/0	2/2/4/0	2/2/4/2	2/2/4/0	2/2/3/2	2/2/4/0	2/2/4/0
I_{L1}	$\frac{i_H}{(1-D_H)^2}$	$\frac{i_H D_H}{(1-D_H)^2}$	$\frac{i_H}{(1-D_H)^2}$	$\frac{i_H}{(1-D_H)^2}$	$\frac{i_H}{(1-D_H)^2}$	$\frac{i_H}{(1-D_H)^2}$	$\frac{i_H}{(1-D_H)^2}$
I_{L2}	$\frac{i_H}{(1-D_H)}$	$\frac{i_H}{(1-D_H)}$	$\frac{i_H}{(1-D_H)}$	$\frac{i_H D_H}{(1-D_H)^2}$	$\frac{i_H}{(1-D_H)}$	$\frac{i_H}{(1-D_H)}$	$\frac{i_H}{(1-D_H)}$
I_{S1}	i_{L1}	$i_{L1}+i_{L2}$	i_{L1}	i_{L1}	i_{L1}	i_{L1}	i_{L1}
I_{S2}	i_{L2}	i_{L2}	$i_{L1}+i_{L2}$	$i_{L1}+i_{L2}$	$i_{L1}+i_{L2}$	i_{L2}	i_{L2}
I_{S3}	i_{L1}	i_{L1}	i_{L1}	i_{L1}	-	$i_{L1}-i_{L2}$	i_{L1}
I_{S4}	i_{L2}	i_{L2}	i_{L2}	$i_{L1}+i_{L2}$	i_{L2}	i_{L2}	i_{L2}
V_{S1}, V_{S3}	V_{C1}	V_{C1}	V_{C1}	V_{C1}	V_{C1}	V_{C1}	V_{C1}
V_{S2}	V_H	V_H	V_H	V_H	V_H	V_H	V_H
V_{S4}	V_H	V_H+V_{C1}	V_H	V_H	V_H	V_H+V_{C1}	V_H
V_{C2}	$D_H V_H$	V_H	V_H	V_H	V_H	V_H	V_H
η (%)	97.29	96.79	95.34	95.79	95.39	97.20	97.25
Volume (cm^3)	860.62	911.18	975.17	911.18	943.17	911.18	911.18
Power density (W/cm^3)	0.813	0.768	0.718	0.768	0.742	0.768	0.768
Cost (USD)	67.30	72.29	91.81	90.59	80.19	71.72	73.87
PSS	Low voltage ripple	Lower Gain	Not possible	Higher voltage Drop	Not possible	Lower Gain	No change in ripple
PSS Gain	$\frac{1}{(1-D_H)^2}$	$\frac{D_H}{(1-D_H)^2}$	-	$\frac{1}{(1-D_H)^2}$	-	$\frac{D_H}{(1-D_H)^2}$	$\frac{1}{(1-D_H)^2}$

#Cost includes the cost of switches, inductors, capacitors, and heat sinks
Color coding: Better performance; Lower performance

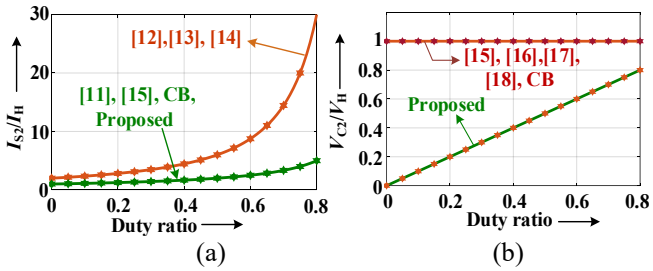


Fig. 7 Performance comparison (a) Current stress in switch, S_2 (b) Voltage stress of capacitor, C_2.

proposed E-BDC, as summarized in Table IV. Converters [12] and [14] require additional diodes to achieve the same VCG, while the proposed E-BDC maintains a reduced component count. Although [14] reduces the number of active switches, it does so at the cost of added passive components. In terms of current stress, the proposed E-BDC, along with [11] and [15], exhibits lower current stress on switch S_2, as illustrated in Fig. 7(a). In contrast, converter [13] experiences the highest current stress, equal to (i_{L1} + i_{L2}) through both switches, which significantly increases conduction losses. Similarly, elevated current stress is observed in switch S_1 of [11] and switch S_2 of [12] and [14], as summarized in Table IV. While [15] reduces current stress on S_3, it suffers from substantially higher voltage stress on S_4, indicating a trade-off between current and voltage stresses in existing designs. With respect to voltage stress, the proposed E-BDC offers a clear advantage. In [11] and [15], the switches are subjected to voltages exceeding the high-side potential (V_H + v_{C1}), necessitating higher voltage-rated switches. In contrast, the proposed topology maintains controlled voltage levels across all semiconductor devices. This advantage is further evident in the output capacitor stress, as shown in Fig. 7(b). In the proposed converter, the voltage across C_2 is regulated as $D_H V_H$, resulting in a normalized stress of v_{C2}/V_H = D_H, which is lower and dependent on the duty cycle. Conversely, converters [15]-[18] and the Cascaded Boost (CB) converter exhibit a constant normalized stress of v_{C2}/V_H = 1, since the output capacitor directly supports the full output voltage. The cascaded structure of capacitors C_1 and C_2 in the proposed E-BDC ensures that v_{C2} remains below V_H, enabling the use of lower-rated capacitors and improving overall reliability.

From a current distribution perspective, the proposed E-BDC effectively shares current between inductors i_{L1} and i_{L2}, thereby reducing the peak current burden on individual components. A similar current sharing is observed in the CB converter; however, other topologies [12]- [13] concentrate current in a single switch, leading to increased conduction losses. The inherent current-sharing feature of the proposed topology minimizes current stress and enhances efficiency. Furthermore, under PSS operation, the proposed E-BDC achieves low voltage ripple while maintaining the desired VCG. In contrast, the CB converter attains the same VCG with higher ripple, and PSS operation is not feasible in [12] and [14]. Although PSS can be applied in [11] and [15], it results in reduced voltage gain, limiting their effectiveness. Overall, the proposed E-BDC demonstrates clear advantages over existing quadratic bidirectional DC-DC converters in terms of reduced component count, lower voltage and current stress, effective current sharing, improved ripple performance, and compact structure, while achieving the same VCG.

C. Loss Analysis:

To determine the efficiency of E-BDC, it is essential to compute the losses associated with each component during both the step-up and step-down modes of operation. The loss, P_L resulting from the parasitic resistance (R_L) in the inductor of the proposed E-BDC is computed, as given in (12).

$$P_L = (I_{L1}^2 + I_{L2}^2)R_L = R_L I_H^2\left(\frac{2-2D_H+D_H^{\,2})}{(1-D_H)^4}\right) = R_L I_H^2\left(\frac{1+D_L^{\,2}}{D_L^{\,4}}\right) \quad (12)$$

The capacitor loss P_C, associated with the ESR (R_C) of the capacitor expressed as ($I^2_{C1,rms}$ + $I^2_{C2,rms}$) R_C is given in (13), where $I_{C1,rms}$ and $I_{C2,rms}$ are the RMS current flowing through the capacitors C_1 and C_2, respectively.

$$P_C = R_C I_H^2\left(\frac{(2D_H-2D_H^{\,2}+D_H^{\,3})}{(1-D_H)^3}\right) = R_C I_H^2\left(\frac{(1-D_L)}{D_L^{\,3}}\right) \quad (13)$$

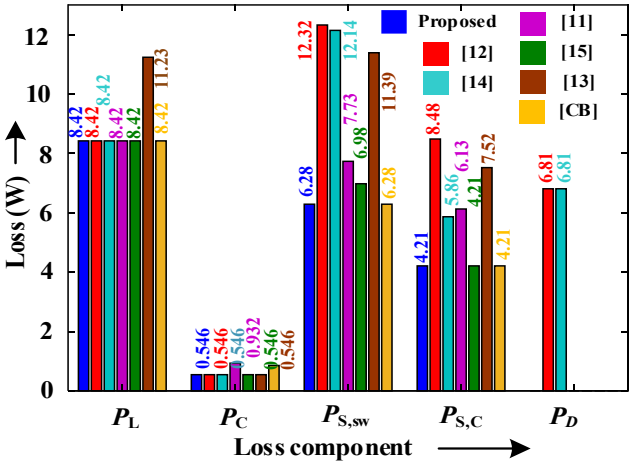
The conduction loss of the switches is determined using (14), where the resistance of each switch is denoted as R_S.

$$P_{S\_Cond} = R_S I_H^2 \left(\frac{2-2D_H+D_H^2}{(1-D_H)^4} \right) = R_S I_H^2 \left(\frac{1+D_L^2}{D_L^4} \right) \quad (14)$$

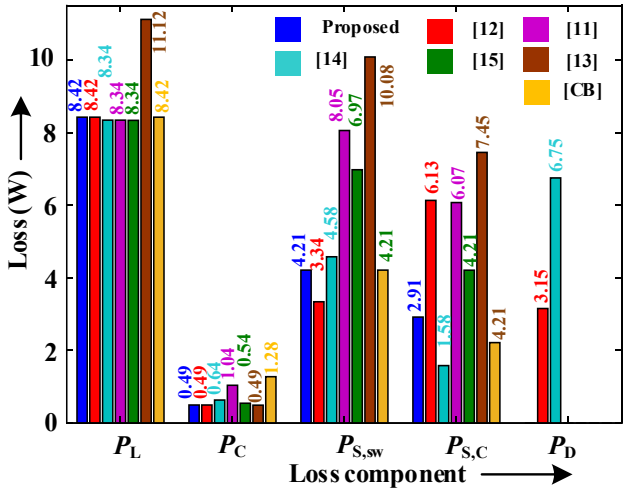
The switching loss of the four switches is given in (15),

$$P_{S,SW} = \frac{1}{2}\left[\sum_{i=1}^{4} V_{Si} I_{Si,avg} \right] (t_{on} + t_{off}) f_s \quad (15)$$

where V_{Si} and $I_{Si,avg}$ are the average voltage and current across the i^{th} switch, t_{on} and t_{off} are its effective turn-on and turn-off transition times, respectively and f_s is the switching frequency. The loss associated with each component for the rated operation is displayed for both step-up (Fig. 8(a)) and step-down (Fig. 8(b)) operations. The analytical efficiency of the proposed E-BDC is computed by using these loss values. Fig. 9 illustrates the efficiency profiles for the step-up (Fig. 9(a)) and step-down (Fig. 9(b)) modes of operation at different output power levels. These loss and efficiency analysis considered, the parasitic resistances of R_L = 100 mΩ, R_C = 30 mΩ, and R_S = 50 mΩ for both the proposed and conventional BDCs. As observed from Fig. 9, the analytical efficiency of the proposed E-BDC outperforms compared to [11] - [15] and CB during both step-up and step-down modes of operation.



(a)

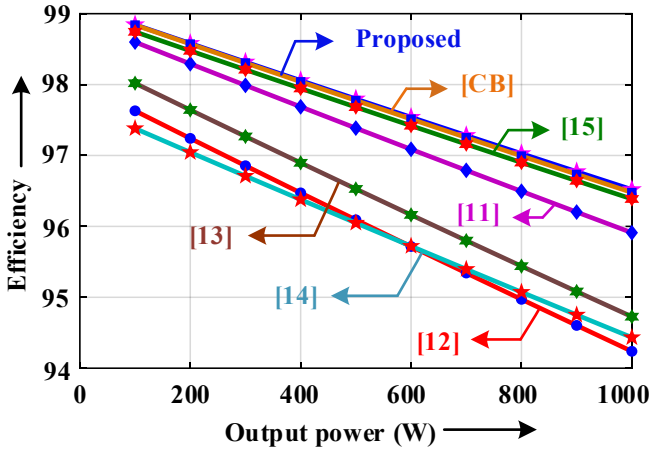


(b)

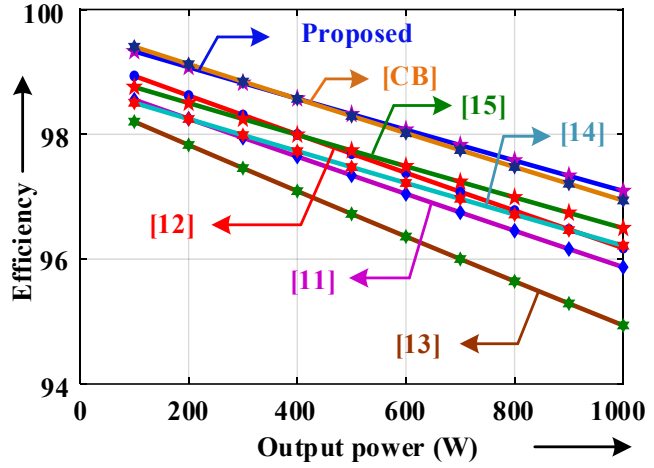
Fig. 8. Theoretical loss breakdown (a) step-up mode (b) step-down mode.

D. VCG Considering Parasitic Elements:

The presence of parasitic elements causes the output voltage to deviate from the ideal value. By accounting for parasitic effects, the output voltages in the step-up and step-down modes are calculated, as given in (16) and (17),



(a)



(b)

Fig. 9. Efficiency profile *versus* output power (a) step-up mode (b) step-down mode.

respectively.

$$V_{H_{Para}(n=1)} = \frac{V_L}{(1-D_H)^2 + \frac{R_L}{R}m + \frac{R_C D_H m}{R(1-D_H)} + \frac{R_S}{R}m}; m = \left(\frac{2-2D_H+D_H^2}{(1-D_H)^2} \right) \quad (16)$$

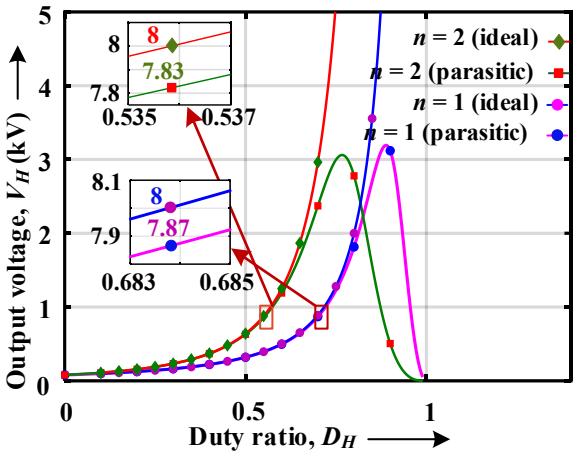
$$V_{L_{Para}(n=1)} = \frac{V_H D_L^2}{\left[1 + \frac{R_L}{R}(1+D_L^2) + \frac{R_C}{R}(D_L^2 - 2D_L^4 + D_L) + \frac{R_S}{R}(1+D_L^2) \right]} \quad (17)$$

The parasitic VCG of the proposed E-BDC for n = 2 is derived in (18) and (19). Fig. 10(a) and (b) display the analytical output voltage *versus* duty ratio for both the ideal and parasitic VCGs when n = 1 and n = 2, respectively. Although the multi-stage E-BDC configuration increases the number of switches and inductors, the reduction in current stress on each component leads to an overall improvement in efficiency, particularly at higher output voltage levels. As shown in Fig. 11(a), the n = 2 stage converter exhibits higher efficiency than the single-stage topology for $V_H \geq 600$ V at 200 W load. Similarly, Fig. 11(b) demonstrates improved efficiency across the entire power range for V_H = 2000 V.

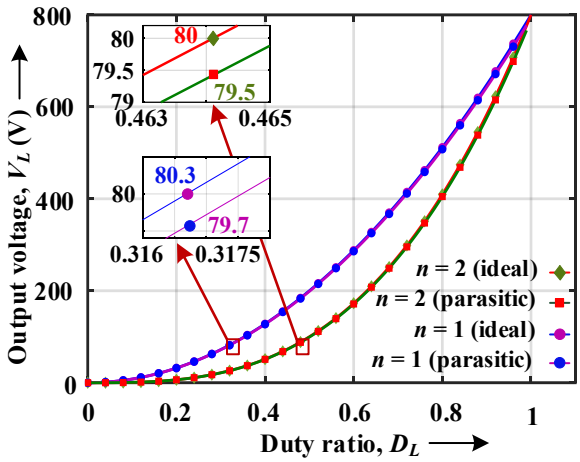
This confirms that despite the additional components, the distributed current among multiple stages effectively reduces conduction and thermal losses, resulting in a net enhancement in conversion efficiency at medium power and high-voltage operation.

$$V_L\big|_{n=2} = \frac{V_H D_L^3}{\left[1+\frac{R_L}{R}(1+D_L^2+D_L^4)+\frac{R_C}{R}(D_L+D_L^2+2D_L^3-D_L^5-3D_L^6)+\frac{R_S}{R}(1+D_L^2+D_L^4)\right]} \tag{18}$$

$$V_H\big|_{n=2} = \frac{V_L}{(1-D_H)^3\left[1+\frac{R_L}{R}\left(\frac{3-6D_H+7D_H^2-4D_H^3+D_H^4}{(1-D_H)^6}\right)+\frac{R_C}{R}\left(\frac{14-34D_H+34D_H^2-16D_H^3+3D_H^4}{(1-D_H)^5}\right)+\frac{R_S}{R}\left(\frac{-6D_H+7D_H^2-4D_H^3+3+D_H^4}{(1-D_H)^6}\right)\right]} \tag{19}$$



(a)



(b)

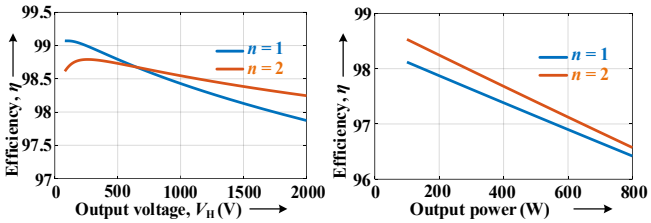
Fig. 10. Performance comparison for n =1 and n = 2 (a) Ideal and parasitic voltage waveforms during step-up; (b) Ideal and parasitic voltage waveforms during step-down.

IV. Dynamic Analysis and Robust Controller Design

Although steady-state behavior is discussed, dynamic modeling is necessary to analyze transient performance and design controllers. Due to its wide operating range and bidirectional operation, a state-space model is developed to accurately represent both step-up and step-down modes.

A. Dynamic Modeling in Step-Up Mode:

In step-up operation, the dynamic behavior of the E-BDC over one switching period can be described by two linear time-invariant subsystems corresponding to the switching states identified in the steady-state analysis. By selecting the inductor currents and capacitor voltages as state variables, the converter dynamics can be expressed in state-space form for each switching interval. The state-space equations governing



(a) (b)

Fig. 11 (a) Efficiency profile with respect to output voltage (b) Efficiency profile with respect to varying load conditions.

the converter dynamics are given by (20).

$$\left.\begin{aligned}[\dot{x}_H] &= [A_j][x_H]+[B_j][u_H]\\ [y_H] &= [E_j][x_H]+[F_j][u_H]\end{aligned}\right\} j = \begin{cases}\text{H}_{\text{on}}\,(\text{when S}_1\text{ and S}_2\text{ is on})\\ \text{H}_{\text{off}}\,(\text{when S}_1\text{ and S}_2\text{ is off})\end{cases} \tag{20}$$

where, j represents operational state of the switch, $[x_H]$ is the state vector, $[i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}]^T$. $[u_H]$ is the input vector given by v_L in the step-up mode, and $[y]$.is the output vector. When switches S_1 and S_2 operate in their respective switching states, the converter dynamics, including the parasitic resistances of the circuit components, are described using state-space representations corresponding to the on and off intervals. To obtain a continuous-time description of the converter, the state-space averaging technique is applied over one switching period. The resulting averaged large-signal model is expressed as a duty-ratio-weighted combination of the individual switching state models, as given in (21).

$$\begin{aligned}[A_{av}] &= \left[A_{H_{on}}D_H + A_{H_{off}}(1-D_H)\right];\ [B_{av}] = \left[B_{H_{on}}D_H + B_{H_{off}}(1-D_H)\right]\\ [E_{av}] &= \left[E_{H_{on}}D_H + E_{H_{off}}(1-D_H)\right];\ [F_{av}] = \left[F_{H_{on}}D_H + F_{H_{off}}(1-D_H)\right]\end{aligned} \tag{21}$$

The averaged large-signal model is then linearized about a nominal operating point using small-signal perturbation theory, wherein the state variables, duty ratio, and input quantities are expressed as the superposition of their steady-state values and small-signal components. This yields a linear time-invariant small-signal model that accurately characterizes the dynamic response of the converter to input variations and duty-cycle changes. Based on the linearized model, the control-to-output transfer function is derived as given in (22), establishing the relationship between duty-ratio perturbations and the output voltage variation. From (22), it is evident that the four poles ($-37.6 \pm i3.11 \times 10^3$, $-174 \pm i919$) are located in the left half of s-plane, confirming the inherent

stability of the open-loop dynamics. While two zeros (-341 ±2.96 × 10^3) lie in the left half-plane, a right-half-plane zero at (2.74 × 10^3) is also observed. This indicates that the converter exhibits non-minimum phase characteristics, which introduce additional phase lag and impose limitation on the achievable control bandwidth. Consequently, the controller must be carefully designed to ensure adequate phase margin and stable closed-loop operation.

$$\frac{\hat{v}_H(s)}{\hat{d}_H(s)} = \frac{-1.674\times10^6 s^3 + 3.436\times10^9 s^2 - 1.173\times10^{13} s + 4.063\times10^{16}}{s^4 + 422.2 s^3 + 1.059\times10^7 s^2 + 3.428\times10^9 s + 8.47\times10^{12}} \tag{22}$$

$$\frac{\hat{v}_L(s)}{\hat{d}_L(s)} = \frac{2.523\times10^{10} s^3 + 1.261\times10^{17} s^2 - 8.875\times10^{19} s + 1.402\times10^{24}}{s^5 + 5.022\times10^6 s^4 + 1.096\times10^{11} s^3 + 5.531\times10^{14} s^2 + 9.811\times10^{17} s + 2.82\times10^{21}} \tag{23}$$

B. Dynamic Modeling in Step- Down Mode:

A similar modeling procedure is followed for the step-down mode of operation, wherein the corresponding on and off state equations are formulated based on the switching sequence of switches S_3 and S_4. By applying state-space averaging and small-signal linearization, the control-to-output transfer function for step-down operation is obtained as given in (23). As observed from (23), although all the poles (-349 ± *i*2.49 × 10^3, -5.81 × 10^3, -1.54 × 10^4, -5 × 10^6) and one zero (-5 × 10^6) are located in the left half of the s-plane, the step-down dynamics also exhibit non-minimum phase behavior. This is due to the presence of two right-half- plane zeros at (353 ± *i*3.32 × 10^3) which introduce additional phase lag and influence the achievable control bandwidth.

C. Controller Design:

To evaluate the closed-loop stability and dynamic performance of the proposed E-BDC under bidirectional operation, two separate PI controllers are designed: one for step-up mode and another for step-down mode, as illustrated in Fig. 12. Since the control-to-output transfer functions differ in the two operating modes, independent controller designs are necessary. The Stability Boundary Locus (SBL) method is employed to systematically determine the stabilizing regions of proportional and integral gains based on the converter's small-signal dynamics. For each operating mode, the closed- loop characteristic equation is formulated by combining the PI controller with the corresponding small-signal model. By applying stability boundary conditions in the frequency domain, admissible regions of controller gains that guarantee closed-loop stability are obtained. These stability regions are depicted for step-up and step-down modes in Fig. 13(a) and Fig. 13(b), respectively. Although the SBL method provides the stabilizing gain ranges, the final gain selection is guided by frequency-domain performance criteria. The gains are chosen to ensure adequate Phase Margin (PM), Gain Margin (GM), and an appropriate crossover frequency. In step-up mode, special care is taken to select a crossover frequency well below the right-half-plane zero to mitigate non-minimum phase effects and preserve stability. The selected gains are $K_p = 2\times 10^{-5}$ and $K_i = 0.018$ for step-up mode, and $K_p = 1\times 10^{-4}$ and $K_i = 0.3$ for step-down mode. Frequency response analysis confirms substantial stability improvement. In step-up mode, GM and PM improve from -60 dB and -89.8º (unstable) to 11.4 dB and 92.1 º (Fig. 14(a)), respectively. Similarly, in step-down mode, GM increases from -53.9 dB to 17.9 dB, and PM improves from 8.16º to 89.3º (Fig. 14(b)), validating the effectiveness of the controllers.

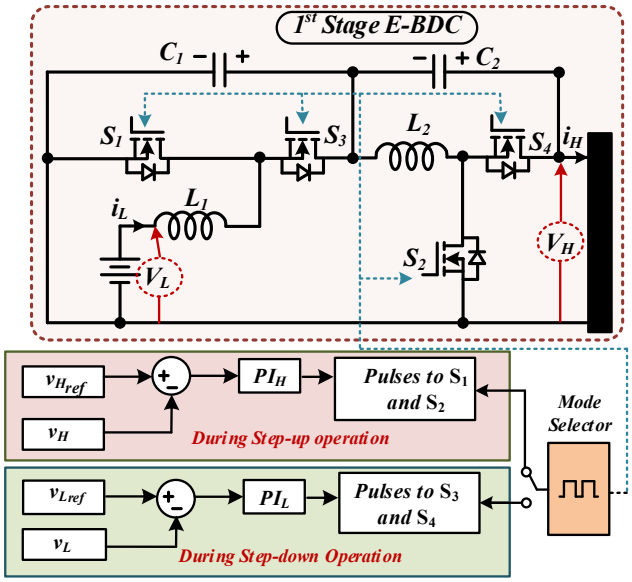


Fig. 12. Block diagram for closed-loop control of E-BDC for both step-up and step-down mode of operation.

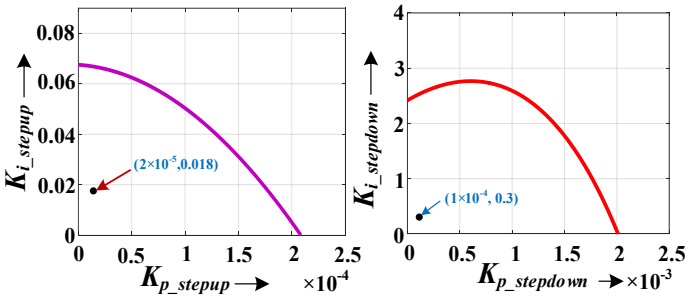


Fig. 13. Boundary for K_p & K_i (a) Step-up (b) Step-down.

V. HARDWARE DEVELOPMENT AND TESTING

A laboratory-scale prototype of the proposed E-BDC, rated at 700 W, 800 V, and operating at 50 kHz, was fabricated to experimentally validate the theoretical analysis. The experimental setup is shown in Fig. 15. The hardware setup consists of a programmable low-voltage DC source (GWINSTEKPSW-250/13.5), a programmable high-voltage DC source (PAT850/9.4T), and an electronic load

(PLZ1005WH2) to facilitate experimental verification under both step-up and step-down operating modes. The selection of operating mode is achieved through the switching control strategy: in step-up mode, switches (S_1, S_2) are activated with duty ratio D_H, enabling power transfer from the low-voltage side to the high-voltage side, whereas in step-down mode, switches (S_3, S_4) are controlled with duty ratio D_L, enabling reverse power flow from the high-voltage source to the low-voltage side.

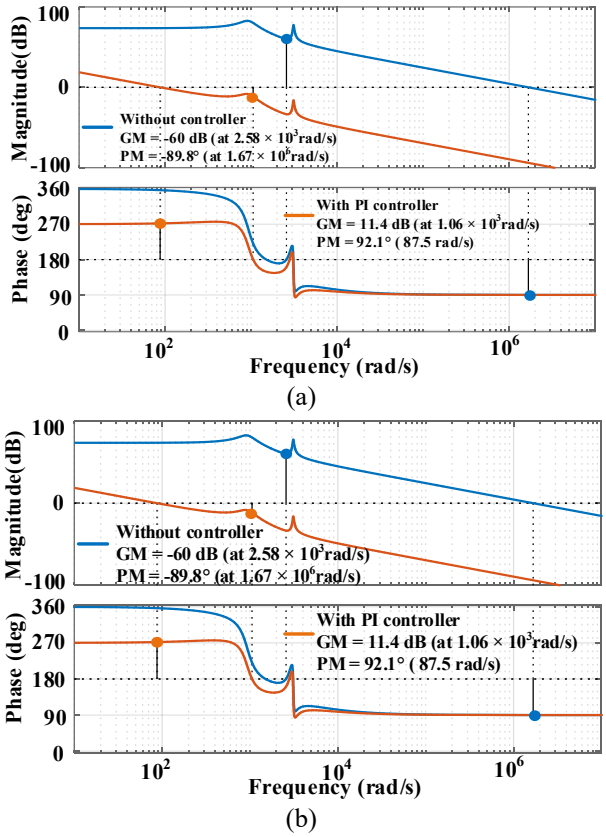


Fig. 14. Frequency response of E-BDC with and without controller for (a) step-up mode (b) step-down mode.

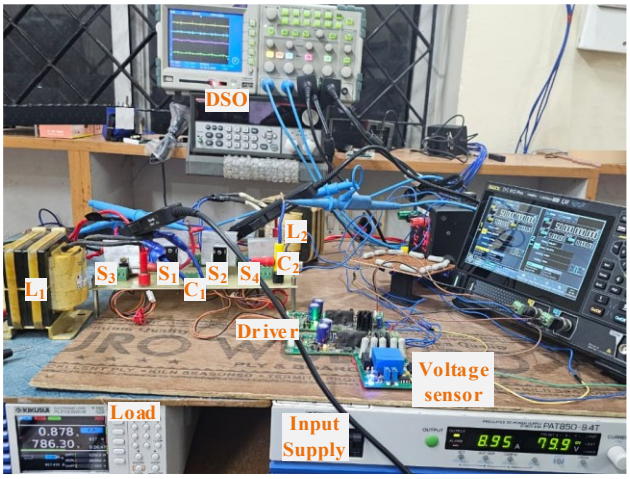


Fig. 15. Experimental setup of the proposed E-BDC in laboratory environment.

In step-up mode, the measured waveforms (Fig. 16) closely agree with analytical predictions. Inductor L_1 is energized at 80 V and de-energized at 173 V, while L_2 is energized at 253 V and de-energized at 547 V (Fig. 16(a)), confirming proper energy transfer. Due to the proposed topology, each switch conducts only one inductor current, reducing current stress; for instance, switch S_2 carries 2.82 A, equal to the L_2 current. At a duty ratio of 68.40%, the converter delivers 787 V output with 0.878 A output current (Fig. 16(b)), corresponding to 700 W and achieving an efficiency of 96.47%. Capacitor voltage measurements verify reduced voltage stress, with the output voltage equal to the sum of v_{C1} and v_{C2} (Fig. 16(c)). The switch voltage waveforms show negligible oscillations due to inherent voltage self-balancing and capacitive turn-off protection (Fig. 16(d)). Furthermore, ripple measurements under synchronous and phase-shifted switching (Fig. 17(a) and (b)) confirm that phase-shifted operation significantly reduces capacitor and output voltage ripple.

In step-down mode (Fig. 18), the experimental inductor voltage and current waveforms closely match the analytical results. With an input voltage of 800 V, the converter produces 78.20 V at a duty ratio of 31.70%, achieving an efficiency of 97.00%, thereby demonstrating stable and efficient bidirectional operation. The pulsating nature of the high-voltage side current i_H, as observed in Fig. 18(a), is inherent to the operating principle of the proposed converter. However, this pulsation is primarily confined to the internal energy transfer paths and does not significantly impact the load-side voltage due to the presence of output capacitors, which effectively smooth the delivered voltage. For applications involving sensitive sources, the ripple in i_H can be mitigated through appropriate design measures such as increased output capacitance, LC filter. To validate this, an LC filter is incorporated at the high-voltage side, and the corresponding experimental waveforms are presented in Fig. 18(b) and Fig. 18(c). It is observed that the current drawn from the high-voltage source becomes continuous, thereby eliminating the aforementioned limitation associated with pulsating current.

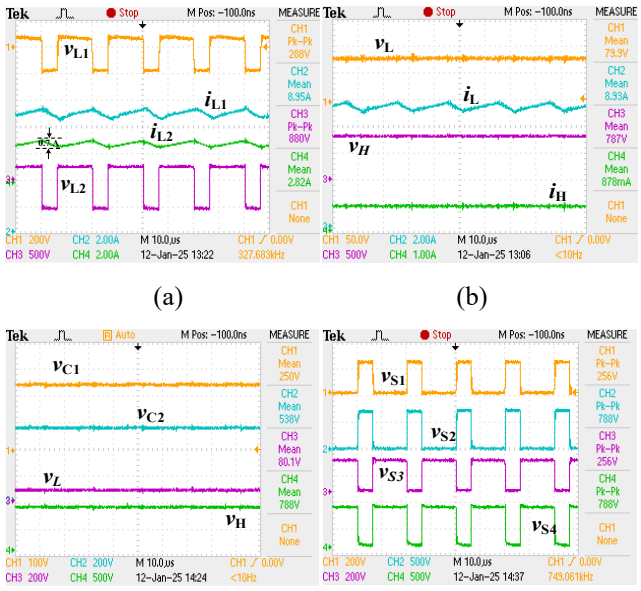
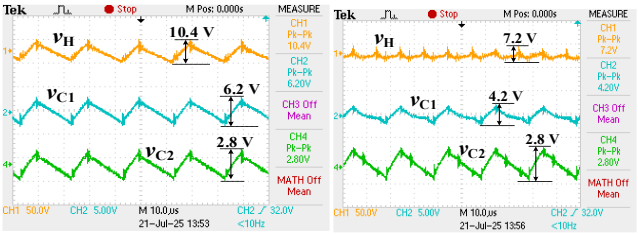


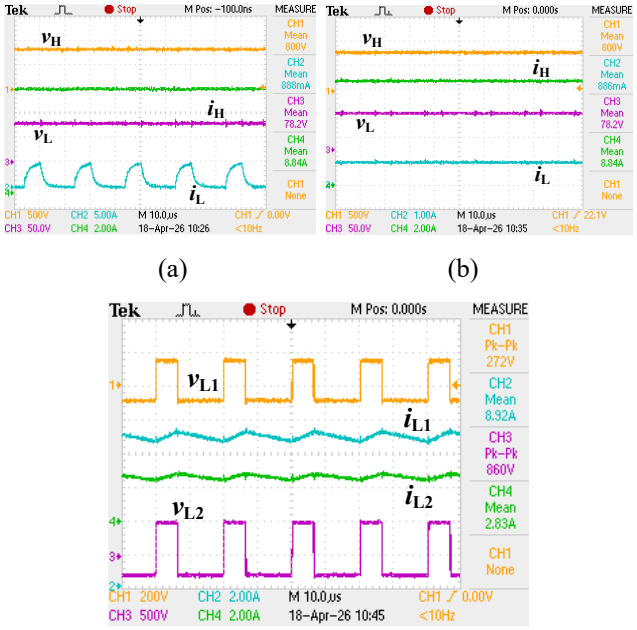
Fig. 16. Experimental waveforms during step-up mode for (a) Inductors (v_{L1}, i_{L1}, i_{L2}, v_{L2}) (b) Input-output (v_L, i_L, v_H, i_H) (c) Capacitors (v_{C1}, v_{C2}), v_L, v_H (d) Switches (v_{S1}, v_{S2}, v_{S3}, v_{S4}).



(a) (b)

Fig. 17. Voltages across the capacitors (v_{C1}, v_{C2}) and high- voltage side (v_H) during step-up operation (a) SS (b) PSS.

The experimental efficiencies for various output powers are plotted in Fig. 19(a) for both step-up and step-down modes of operation. The plot closely matches the analytical results shown in Fig. 9. Additionally, the output voltages corresponding to varying duty ratios, ranging from 30% to 70%, are plotted in Fig. 19(b) for both step-up and step-down

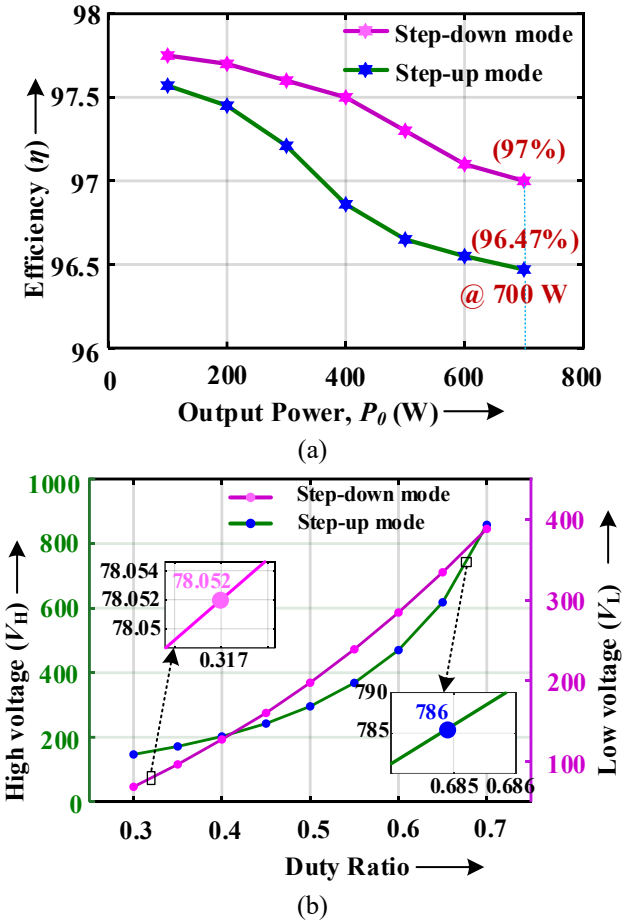


(a) (b)

(c)

Fig. 18. Experimental waveforms during step-down mode:(a) v_H, i_H, v_L, i_L without filter (b) v_H, i_H, v_L, i_L with filter (c) v_{L1}, i_{L1}, i_{L2}, v_{L2} with filter.

Closed-Loop Operation and Controller Implementation: The closed-loop controller of the proposed E-BDC is implemented on the Zynq-7000 FPGA platform using Xilinx System Generator (XSG) in the *MATLAB/Simulink* environment. The control algorithm, including the PI controller, PWM generation, and signal conditioning blocks, is modeled in XSG and synthesized to generate a hardware-compatible bitstream (.bit file). This bitstream is programmed onto the Zynq FPGA, enabling real-time digital control. The feedback signals, including output voltage and output currents, are sensed using voltage and current sensors, conditioned through appropriate signal conditioning circuits, and interfaced to the FPGA via onboard ADC channels. The digital PI controller processes the error between reference and measured signals to generate the duty ratios (D_H or D_L), which are used to produce high-frequency PWM pulses for the corresponding switch pairs. Dead-time insertion and synchronization between switching signals are ensured within the FPGA to avoid shoot-through. In addition, protection features such as over-voltage, over-current, and fault shutdown are incorporated in the FPGA logic for reliable operation.



(a)

(b)

Fig. 19. (a) Experimental efficiency versus output power (b) Output voltage versus duty ratio.

modes of operation.

Step-Up Mode Operation: The closed-loop performance is evaluated under both input voltage and load disturbances using the designed PI controller with the K_p and K_i values provided in Section IV.C. When a ramp variation in input voltage from 82 V to 92 V is applied, the output voltage V_H is effectively regulated at 800 V, as shown in Fig. 20(a). The controller restores the output to its reference within approximately 70 ms, demonstrating robust disturbance rejection. Similarly, under load variation, when the output current is changed from 0.50 A to 0.375 A, the converter maintains the output voltage at 800 V with a settling time of about 60 ms and an overshoot of less than 6.8%, as depicted in Fig. 20(b). The results indicate that the controller effectively compensates for both source and load perturbations, ensuring stable operation and tight voltage regulation in step-up mode.

Step-Down Mode Operation: The closed-loop performance of the proposed E-BDC is evaluated using the same PI

controller implemented on the Zynq 7000 FPGA platform.

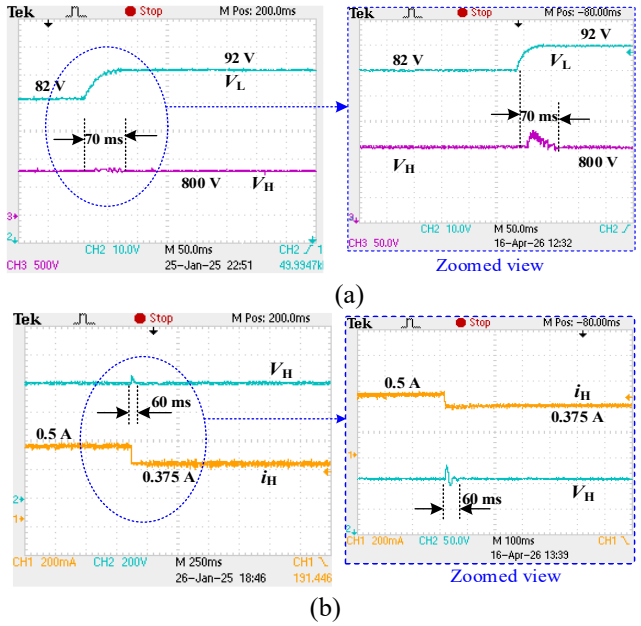


Fig. 20. Closed loop response during step-up mode (a) regulated V_H for disturbance in V_L (b) regulated V_H for disturbance in i_H.

The controller parameters (K_p and K_i) for step-down operation ensure robust regulation under both source and load disturbances. When a variation in the high- voltage side input from 740 V to 790 V is introduced, the voltage V_L is effectively regulated at the desired reference of 80 V, as depicted in Fig. 21(a). Despite the significant perturbation in the input voltage, the controller maintains stable operation, and the output voltage returns to its nominal value within a settling time of approximately 100 ms. Similarly, the dynamic response of the converter under load variation is analyzed by applying a step change in load current from 3.80 A to 0.89 A. As shown in Fig. 21(b), the voltage V_L remains well-regulated at 80 V, with an overshoot limited to less than 13%. The transient response demonstrates that the controller effectively compensates for sudden load variations without causing instability or excessive oscillations. Overall, the obtained experimental waveforms validate the effectiveness of the designed PI controller in maintaining stable and reliable output voltage regulation during step-down operation. These results confirm that the proposed E-BDC achieves satisfactory dynamic performance under both input voltage and load disturbances, thereby ensuring robust closed-loop operation in bidirectional modes.

VI. Conclusion

This paper presented an extendable bidirectional DC–DC converter, viz. E-BDC with a cascaded capacitor-based structure to achieve high voltage gain with reduced device stress. The proposed E-BDC topology ensures inherent inductor current sharing, thereby reducing switch current stress, while the cascaded configuration enables natural voltage distribution across capacitors and switches without additional balancing circuits. The converter exhibits a scalable quadratic-type gain, making it suitable for wide voltage range applications. A detailed steady-state analysis, including component design, voltage and current stress, and ripple characteristics, has been provided. The influence of practical non-idealities on performance has also been discussed. Comparative evaluation with existing topologies demonstrates that the proposed converter achieves an improved trade-off among voltage gain, component count, stress distribution, and control complexity. The voltage gain characteristics confirm that high gain is achieved at moderate duty ratios.

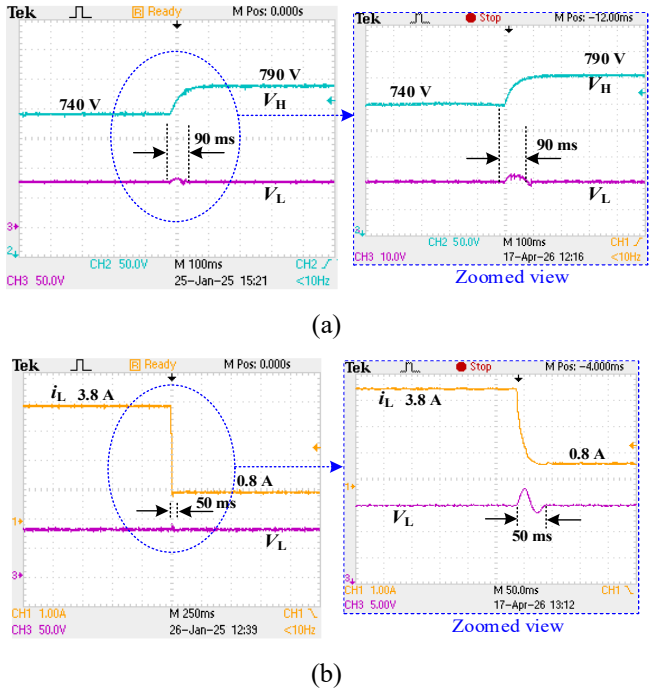


Fig. 21. Closed loop response during step-down mode (a) regulated V_L for disturbance in V_H (b) regulated V_L for disturbance in i_L

A 700 W, 800 V, 50 kHz prototype was developed to validate the proposed converter. Experimental results in both step-up and step-down modes closely match theoretical predictions. Phase-shifted operation reduces capacitor voltage ripple and enhances output stability. The pulsating high-voltage side current is effectively mitigated using an LC filter, ensuring suitability for practical applications. Small-signal modeling enabled the design of PI controllers, implemented on an FPGA platform. Closed-loop results demonstrate stable operation under input and load disturbances. Future work includes validation using regenerative setups for seamless bidirectional operation and extending the topology to higher power applications.

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