Electric Field Redistribution Driven SEGR Mitigation in a High-k Trench VDMOS with Floating Islands

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***Abstract*—Single-event gate rupture (SEGR) in trench-based power MOSFETs originates from transient oxide-normal electric fields generated during heavy-ion–induced charge transport, rather than from static breakdown limitations alone. Conventional mitigation approaches, such as stacked high-k gate dielectrics or drift-region field modulation using floating islands, address different aspects of the electric-field distribution but are typically examined independently. In this work, a TCAD-based study is presented to investigate how the co-integration of a high-k/SiO_2 stacked trench dielectric and P-type floating islands in the drift region modifies electric-field partitioning under both steady-state blocking and transient heavy-ion irradiation. The combined effect of dielectric field redistribution and drift-region charge modulation reduces the peak oxide-normal electric field and delays the onset of gate rupture. Calibrated simulations indicate an increase in breakdown voltage relative to a conventional trench Vertical double-diffused MOSFETs (VDMOS) while maintaining comparable specific on-resistance. Under heavy-ion irradiation, the reduced oxide field enables sustained operation up to a linear energy transfer of $40\ \mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$ at 35% of the rated breakdown voltage. These results clarify the role of coupled dielectric and drift-region field engineering in SEGR mitigation and provide physics-based guidance for radiation-tolerant silicon power MOSFET design.**

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***Index Terms*—Trench VDMOS, Single-Event Gate Rupture, high-k dielectric, floating islands, radiation effects.**

I. Introduction

POWER MOSFETs are widely used in aerospace and high-reliability electronic systems, where exposure to ionizing radiation can introduce single-event effects that challenge long-term device robustness [1]. The effective performance of these missions depends on how well power MOSFETs perform under extreme radiation conditions [1]–[4]. VDMOS is now important among other device architectures because they can conduct high voltages and high currents with minimal conduction loss. Their reliability, however, is highly dependent on the gate dielectric structure, which determines threshold voltage, breakdown voltage, and response to stressors, e.g., ionizing radiation and high electric fields. This is feasible in an environment where energetic protons and heavy ions induce single-event effects (SEEs) when in both active and idle states [5]–[8]. SEGR is typically characterized by the temporary build-up and transfer of radiation-induced charge at the Si/SiO_2 interface, which could cause temporary oxide-normal electric fields that are greater than the inherent dielectric strength [9]–[11]. Various structural and material-based approaches have been considered in order to alleviate SEGR in power MOSFETs, each addressing a different facet of electric-field development under radiation stress [13]–[15]. Specifically, methods of dielectric engineering, e.g., composite dielectric stacks, e.g., SiO_2 /Si_3N_4, have been shown to have better electric-field redistribution and radiation tolerance [12], [16]–[20]. Investigations of super-junction MOSFETs have elucidated the mechanisms of SEGR and proposed the advantages of using high-k or stacked dielectrics over traditional SiO_2. In parallel, structural modifications such as floating island MOSFETs have been investigated, where p-type floating islands are introduced into the drift region to reshape the electric field and increase breakdown voltage [21]–[27]. Several additional design techniques, spanning dielectric engineering, drift-region modification, and geometric optimization, have also been reported to enhance radiation tolerance in power MOSFETs [28]–[35]. The concepts of floating island and partially floating island structures have been extensively studied in both Si and SiC VDMOS technologies, primarily for improving breakdown voltage and reducing on-resistance [22]–[24], [36]–[38].

Recent studies have explored several approaches for electric-field engineering in power VDMOS structures. High-k dielectric integration has been investigated to improve electric-field distribution and enhance the breakdown voltage to on-resistance trade-off through dielectric field modulation [36], [37]. Similarly, floating-island-based approaches have demonstrated improved field redistribution within the drift region through charge balancing and electric-field spreading mechanisms [23], [29]. In parallel, radiation-hardening studies have investigated structural approaches to reduce oxide electric-field stress and mitigate SEGR susceptibility under heavy-ion irradiation [13], [15]. However, these approaches are generally investigated independently, with limited focus on simultaneously addressing electric-field optimization and radiation robustness.

Despite these advances, the interaction between dielectric

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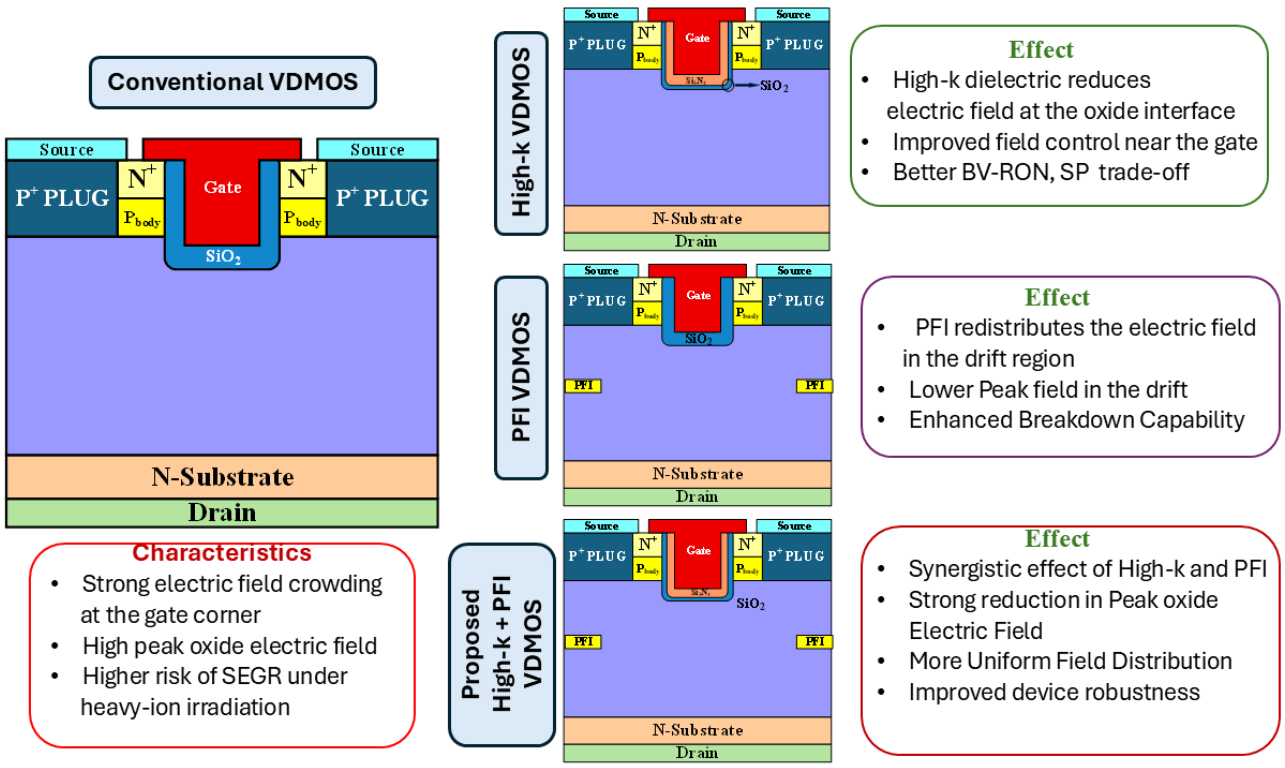

Fig. 1. Evolution of VDMOS structures: from conventional design to the proposed high-k + PFI structure for improved field control and SEGR mitigation.

TABLE I
SUMMARY OF RECENT FIELD-ENGINEERING AND RADIATION-HARDENING APPROACHES IN VDMOS STRUCTURES

Approach	Author and Year	Primary Objective	Reference
High-k dielectric engineering	Yao et al., 2025	Electric-field redistribution through dielectric modulation and improved BV–R_{on} trade-off	[36]
Extended high-k trench structures	Yao et al., 2024	Field spreading near trench interface and improved blocking performance	[37]
Floating-island field engineering	Krishnamurthy et al., 2020	Charge balancing and drift-region electric-field redistribution	[29]
Step-graded floating islands	Zhao et al., 2023	Field spreading and optimization of drift-region charge distribution	[23]
SEGR hardening structures	Wang et al., 2024	Reduction of oxide electric-field stress under heavy-ion irradiation	[13]
Termination-assisted SEGR mitigation	Chen et al., 2021	Mitigation of oxide stress through termination engineering	[15]
High-k + PFI VDMOS		**Simultaneous electric-field engineering and SEGR mitigation**	**This Work**

field partitioning and drift-region field modulation during heavy-ion irradiation has not been examined within a unified framework as shown in Fig. 1. As summarized in Table I, previous studies have predominantly focused on individual approaches for field engineering or radiation hardening. The proposed high-k with floating-island structure extends these efforts by combining dielectric and structural field engineering to simultaneously improve electric-field distribution and mitigate SEGR susceptibility.

In this work, we address this gap by systematically analyzing the combined effect of a high-k Si_3N_4/SiO_2 stacked dielectric and P-type floating islands, demonstrating that their co-integration results in a synergistic redistribution of the electric field, reducing peak oxide-normal electric field and mitigating SEGR under heavy-ion irradiation conditions. The device is analyzed using TCAD simulations to evaluate its electrical performance and radiation robustness. The results demonstrate that, compared to conventional designs, the proposed structure achieves improved breakdown characteristics along with reduced susceptibility to SEGR. To the best of the authors' knowledge, the combined use of dielectric engineering and structural field modulation to

simultaneously enhance performance and mitigate SEGR in trench VDMOS has not been comprehensively explored.

II. Device Structure and Field Control Concept

A. Device Design

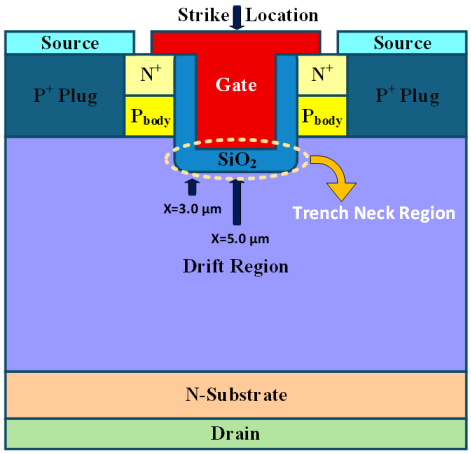

Fig. 2. Cross-sectional schematic of the conventional VDMOS structure highlighting the trench neck region used for electric-field and SEGR analysis.

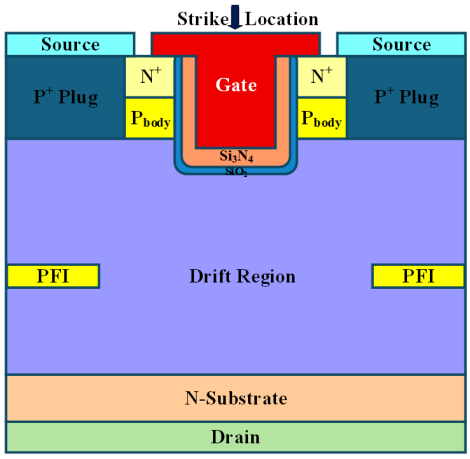

Fig. 3. Cross-sectional schematic of the proposed trench VDMOS structure showing the locations of electric-field extraction cutlines. The positions X = 3 µm, X = 5 µm, and X = 9.5 µm correspond to the trench sidewall (gate oxide region), intermediate drift region, and deep drift region toward the drain, respectively, with the heavy-ion strike location.

The conventional trench VDMOS structure considered in this study serves as the baseline for analyzing electric-field distribution and SEGR susceptibility with parameters shown in Table II. The device consists of a vertical trench gate formed in a p-type body region, with n^+ source regions at the surface, an n-type drift region supporting the blocking voltage, and an n-type substrate acting as the drain contact. A thin SiO_2 gate dielectric lines the trench sidewall and bottom, enabling vertical channel formation along the trench, as shown in Fig. 2. Electric field profiles are extracted along different lateral positions (X = 3 µm, 5 µm, and 9.5 µm), corresponding to the trench sidewall region, mid-drift region, and deep drift region, respectively, to capture spatial field variation across the device. Under blocking conditions, the applied drain voltage is primarily sustained by depletion of the n-type drift region. Owing to the vertical trench geometry, electric-field lines originating from the drain are forced to bend sharply near the trench sidewall and bottom corners, resulting in localized field crowding. The region where the trench gate, p-body, and drift region intersect is referred to as the trench neck. At this location, the abrupt change in geometry and doping profiles leads to a significant enhancement of the oxide-normal electric field along the trench sidewall, which is substantially higher than the average field in the drift region. This field concentration at the gate oxide is an inherent geometrical characteristic of trench-based VDMOS architectures and persists even in the absence of radiation-induced charge. Consequently, the gate oxide in the trench neck represents the most highly stressed region of the device and is therefore the most susceptible to degradation and fracture. For this reason, the conventional trench VDMOS is employed as a realistic reference structure to evaluate how structural and dielectric modifications can redistribute the electric field away from the gate oxide and improve resilience against radiation-induced gate failure mechanisms.

The proposed device structure is derived from the conventional trench VDMOS and introduces two complementary modifications to regulate the electric-field distribution around the trench gate, as shown in Fig. 3. These modifications consist of a stacked gate dielectric consisting of a thin SiO_2 interfacial layer and a high-k Si_3N_4 layer (10 nm SiO_2 / 180 nm Si_3N_4) along the trench sidewall and p-type floating islands (PFIs) embedded in the n-type drift region. The overall device geometry, including the trench gate, p-body, source regions, and the vertical current-conduction path, is preserved to ensure a fair comparison with the baseline structure.

The high-k Si_3N_4/SiO_2 stacked gate dielectric replaces the conventional single-layer SiO_2 along the trench sidewall, enabling redistribution of the electric field across the gate insulator through voltage partitioning between layers of different permittivities. This reduces the oxide-normal electric field within the SiO_2 interfacial layer under high-field operation. In parallel, electrically floating p-type islands are incorporated beneath the trench in the drift region. These islands are isolated from both source and drain contacts and are positioned to interact with the depletion region under blocking conditions, thereby diverting electric-field lines away from the trench neck through localized space-charge modulation without altering the fundamental conduction mechanism.

The placement of the PFIs is selected as a trade-off to ensure effective interaction with the depletion region while avoiding excessive coupling to the channel or gate oxide. Floating islands placed too close to the trench gate may increase parasitic coupling and oxide stress, whereas islands placed too deep in the drift region have limited influence on trench-neck field redistribution. With appropriate placement, dynamic charging of the floating islands under applied bias enables adaptive redistribution of the electric field, shifting the peak

TABLE II
KEY STRUCTURAL AND DOPING PARAMETERS OF CONVENTIONAL AND PROPOSED HIGH-k TRENCH PFI VDMOS STRUCTURES

Parameter	**Conventional Trench VDMOS**	**High-k Trench PFI VDMOS**
Trench width / depth	4 μm / 1.7 μm	Varied (oxide-dependent)
Substrate doping (N_{sub})	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
N^+ region doping	3×10^{19} cm^{-3}	3×10^{19} cm^{-3}
P-body doping	2.8×10^{16} cm^{-3}	2.8×10^{16} cm^{-3}
P^+ plug doping	2.26×10^{19} cm^{-3}	2.26×10^{19} cm^{-3}
N-drift width, length, doping	10 μm, 16 μm, 1.5×10^{15} cm^{-3}	10 μm, 16 μm, varied
Gate oxide Thickness	100 nm	10nmSiO_2 + 180nm Si_3N_4
Spacing between PFI	–	7 μm
P^+ plug to PFI spacing	–	4 μm
PFI thickness, length, doping	–	1 μm, 1.5 μm, varied

field from the gate oxide toward the drift region. Unlike the traditional trench VDMOS, where geometric field crowding concentrates a large fraction of the drain voltage at the trench neck, the proposed high-k trench PFI VDMOS distributes the electric field between the gate dielectric and the drift-region floating islands through structural design alone, forming the basis for the subsequent analysis of blocking behavior and transient radiation response.

B. Electric-Field Modulation via Gate Dielectric Stacking and Floating Island Architecture

In trench-based VDMOS architectures, gate-oxide reliability is primarily governed by the oxide-normal electric field rather than by the applied gate or drain voltage alone. Under high-field blocking conditions, coupling of the drain bias to the trench sidewall causes a localized enhancement of this field near the trench neck, which can trigger single-event gate rupture when it exceeds the intrinsic breakdown strength of SiO_2.

In conventional trench VDMOS devices employing a single-layer SiO_2 gate dielectric, the entire voltage drop across the gate insulator is supported by the SiO_2 layer. This restricts mitigation of oxide electric-field stress without increasing the physical oxide thickness, thereby degrading channel control and device performance. To address this limitation, the proposed architecture employs a stacked gate dielectric comprising a high-k layer with a thin interfacial SiO_2 layer on the trench sidewall.

In a multilayer dielectric stack, the continuity of the electric displacement requires that the electric field in each layer scale inversely with its permittivity, allowing a larger fraction of the applied voltage to be sustained by the high-k layer. Consequently, the oxide-normal electric field in the SiO_2 interfacial layer is reduced relative to a single-oxide configuration under the same bias, thereby enhancing the gate-oxide field margin without altering the channel formation mechanism or the vertical conduction path. Since SEGR originates from transient excursions of the oxide-normal electric field beyond the critical breakdown threshold of SiO_2, stacked dielectric engineering forms a key element of the proposed SEGR mitigation strategy and provides the foundation for analyzing combined dielectric and drift-region field modulation effects in subsequent sections.

In addition to dielectric field partitioning at the trench gate, the proposed structure incorporates P-type floating islands (PFIs) within the drift region to enable spatial redistribution of the electric field through space-charge modulation. Under blocking conditions, the depletion region extends into the drift region and interacts with the embedded PFIs, which dynamically influence the local electric potential. This interaction redistributes the electric-field intensity away from the trench neck and into the drift region. From an electrostatic perspective, the presence of PFIs introduces localized perturbations in the potential distribution, effectively intercepting and diverting electric-field lines that would otherwise terminate at the gate oxide interface. As a result, the peak electric field at the trench sidewall is reduced, while the electric field within the drift region becomes more uniformly distributed. When combined with the high-k Si_3N_4/SiO_2 stacked dielectric, which reduces the electric-field magnitude within the oxide through dielectric screening, the PFIs further contribute by modifying the direction and spatial distribution of the electric field lines. This coupled effect leads to both a reduction in the oxide-normal electric field and a redistribution of field lines away from critical oxide regions. Such coordinated control of electric-field magnitude and direction forms the basis for enhanced SEGR resilience in the proposed structure.

It is important to note that the susceptibility of trench VDMOS devices to Single-Event Gate Rupture (SEGR) is primarily governed by the peak oxide-normal electric field generated during heavy-ion irradiation. In conventional structures, electric field crowding near the gate oxide region leads to localized field enhancement, which can exceed the critical breakdown limit of the oxide under transient charge deposition. The introduction of a high-k dielectric reduces the electric field intensity at the oxide interface by modifying the dielectric coupling, while the incorporation of P-type floating islands (PFIs) promotes a more uniform electric field distribution within the drift region. Consequently, the combined high-k + PFI structure is expected to reduce peak oxide electric field, thereby improving the device robustness against SEGR.

To provide a clearer physical understanding of the elec-

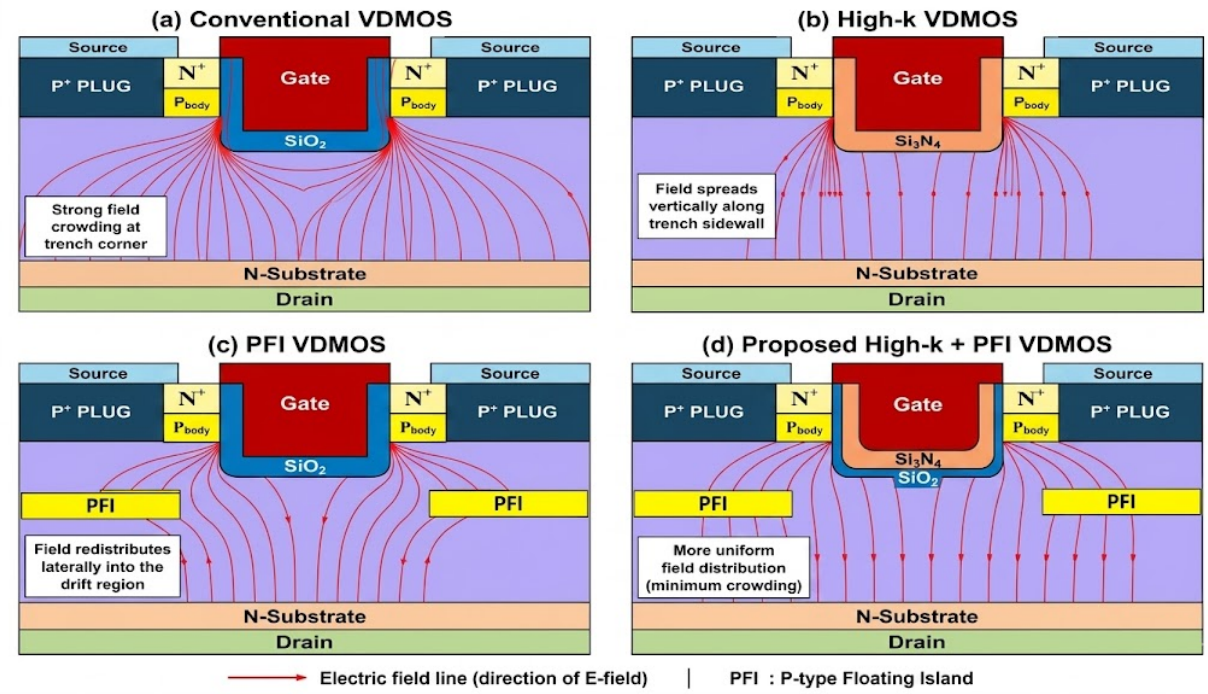

Fig. 4. Conceptual illustration of electric field distribution in different VDMOS structures: (a) Conventional VDMOS showing strong electric field crowding near the trench gate corner, (b) High-k VDMOS illustrating vertical electric field spreading along the trench sidewall,(c) PFI VDMOS demonstrating lateral redistribution of the electric field within the drift region, and (d) Proposed high-k + PFI VDMOS showing a more uniform electric field distribution with reduced peak field concentration.

tric field modulation introduced by the proposed design, a conceptual illustration of the electric field distribution for different device configurations is presented in Figure 4. In the conventional VDMOS structure, strong electric field crowding occurs near the trench gate corner, leading to high oxide stress. The incorporation of a high-k dielectric redistributes the electric field along the trench sidewall, reducing the peak oxide field. Similarly, the inclusion of P-type floating islands (PFIs) modifies the depletion profile within the drift region, enabling lateral spreading of the electric field. The combined high-k + PFI structure results in a more uniform electric field distribution, effectively mitigating peak electric field concentration and improving device robustness under high-field and radiation conditions.

The susceptibility of trench VDMOS devices to Single-Event Gate Rupture (SEGR) is primarily governed by the electric field across the gate oxide, particularly at the trench corner where field crowding is prominent. Under heavy-ion irradiation, the generated charge track within the drift region leads to a transient enhancement of the oxide-normal electric field (E_{ox}), which can exceed the critical breakdown field of SiO_2, resulting in catastrophic gate oxide failure.

The oxide-normal electric field component governing gate dielectric stress can be expressed as:

$$E_{ox} = \frac{Q_d + Q_{ion}}{\epsilon_{ox}} \tag{1}$$

where Q_d is the depletion charge and Q_{ion} represents the radiation-induced charge generated by heavy-ion strikes. This transient charge accumulation significantly increases the local electric field at the Si–SiO_2 interface. where E_{OX} represents the oxide-normal component of the electric field across the gate dielectric rather than the complete electric-field vector. Since SEGR is primarily governed by the electric-field intensity normal to the oxide interface, the oxide-normal field distribution is used throughout this work as the principal metric for evaluating oxide stress and rupture susceptibility. Consequently, Eq. (1) represents a scalar distribution approach for oxide-field analysis, whereas vector electric-field behavior is separately illustrated through field-line distributions and electric-field magnitude contours. In the proposed structure, the introduction of a high-k dielectric layer in conjunction with SiO_2 modifies the electric field distribution at the gate interface according to the dielectric displacement continuity condition:

$$\epsilon_{ox} E_{ox} = \epsilon_{hk} E_{hk} \tag{2}$$

Since $\epsilon_{hk} > \epsilon_{ox}$, the electric field within the SiO_2 layer is reduced for a given electric displacement. This leads to a reduction in the peak oxide electric field, particularly at the trench corner where SEGR is most likely to initiate.

Furthermore, the presence of P-type floating islands (PFI) enhances lateral depletion within the drift region, redistributing the electric field away from the gate oxide and reducing the effective charge coupling to the oxide interface. The combined effect of dielectric modulation and charge redistribution results in a significant suppression of transient electric field spikes at the gate oxide.

As a result, the proposed high-k + PFI structure improves the resilience of the device against heavy-ion-induced SEGR by lowering the peak oxide electric field and mitigating localized field enhancement at the gate interface.

To further understand the role of the gate dielectric interface, the electric field distribution can be analyzed using Poisson's equation:

$$\nabla \cdot (\epsilon \nabla \phi) = -\rho \tag{3}$$

where ϵ is the permittivity, ϕ is the electrostatic potential, and ρ represents the space charge density. In a one-dimensional approximation near the gate oxide interface, this reduces to:

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} \tag{4}$$

indicating that the electric field gradient is inversely proportional to the dielectric permittivity.

For a conventional SiO_2 gate dielectric, the relatively low permittivity results in a higher electric field concentration for a given charge density. Under heavy-ion irradiation, the additional radiation-induced charge (Q_{ion}) significantly increases the local electric field, particularly at the trench corner, thereby increasing the probability of SEGR.

In contrast, when a high-k dielectric is introduced, the increased permittivity reduces the electric field magnitude for the same charge distribution, as governed by Poisson's relation. This effectively suppresses the peak electric field at the Si–dielectric interface.

From an energy band perspective, the dielectric interface modifies the potential distribution across the gate stack, leading to a smoother band bending at the semiconductor–dielectric interface. This reduces localized field enhancement and minimizes the likelihood of impact ionization and oxide breakdown under transient radiation conditions. Fig. 5 provides a conceptual illustration of the dielectric interface modification introduced by the proposed stacked dielectric structure. The incorporation of the Si_3N_4/SiO_2 stack modifies the electrostatic potential distribution near the trench interface and influences electric-field redistribution across the dielectric region. Under heavy-ion irradiation, transient charge accumulation enhances local band bending and oxide stress, which directly influences SEGR susceptibility.

Under heavy-ion exposure, the transient charge deposition introduces a localized perturbation in the electrostatic potential, which can be represented as:

$$\phi(x,t) = \phi_0(x) + \Delta\phi_{ion}(x,t) \tag{5}$$

The presence of a high-k dielectric reduces the sensitivity of the electric field to this perturbation due to its higher permittivity, while the inclusion of P-type floating islands (PFI) redistributes the charge within the drift region, further reducing the effective electric field coupling to the gate oxide.

Therefore, the combined high-k + PFI structure not only modifies the static electric field distribution but also provides enhanced immunity against radiation-induced transient field spikes, thereby improving resistance to SEGR.

C. Radiation Modeling Framework and SEGR Criterion

The response of the device structures to heavy-ion irradiation is analyzed using a physics-based radiation modeling framework implemented in the TCAD environment with parameters shown in Table III. Heavy-ion strikes are modeled using the SINGLE EVENT UPSET formulation, in which an ion with a specified linear energy transfer (LET) deposits charge along a defined track as it traverses the device. The LET determines the density of electron–hole pairs generated. Spatially, the charge deposition follows a radial Gaussian distribution characterized by the track radius and roll-off parameters, enabling realistic lateral carrier spreading, while temporally it is described by a Gaussian time profile defined by the strike time and characteristic time constant. A highly refined mesh is employed along the ion track to accurately resolve carrier generation and transport during irradiation events [39], [40]. The carrier generation profile associated with heavy-ion interaction is represented through a position- and time-dependent formulation given by Equation (6).

To model heavy-ion-induced carrier generation within the semiconductor volume, the transient generation rate is represented using a separable formulation that captures radial charge distribution, ion-track penetration, and temporal evolution independently. This approach enables spatial and temporal decomposition of the ionization profile while maintaining computational efficiency during transient simulations.

$$G(r,l,t) = G_{\mathrm{LET}}(l)\, S(r,l)\, T(t) \tag{6}$$

where $G(r,l,t)$ denotes the volumetric carrier generation rate induced by heavy-ion interaction as a function of radial distance r, ion-track position l, and time t. The term $G_{LET}(r)$ describes the radial carrier distribution associated with the deposited linear energy transfer (LET), $S(r,l)$ represents the spatial dependence of carrier generation along the ion trajectory, and $T(t)$ defines the temporal evolution of the ion strike event. The multiplicative formulation allows the transient ionization process to be decomposed into independent radial, spatial, and temporal components for improved numerical implementation within the TCAD framework.

Single-event gate rupture is identified based on the evolution of the oxide-normal electric field at the trench gate rather than on the magnitude of the gate current. SEGR is considered to occur when the transient oxide-normal electric field exceeds the critical breakdown strength of SiO_2 10 MV/cm [18]. Although a sharp increase in gate current is observed following oxide rupture, this current surge is treated as a consequence rather than the cause of dielectric failure. This field-based failure criterion provides a geometry-independent and industry-consistent definition of SEGR onset. The established radiation modeling framework and failure criterion enable systematic analysis of how structural and dielectric design choices influence transient oxide electric-field behavior under heavy-ion irradiation. While the present study relies on TCAD simulations, the adopted modeling approach and SEGR criterion are consistent with experimentally reported SEGR behavior in vertical power MOSFETs, including trench-gate devices, employing stacked dielectrics and field-modulating structures reported in the literature [6], [7], [9], [12], [28]–[30], [39], [41], [42]. To ensure a consistent evaluation of device behavior under radiation conditions, a standardized simulation testbench

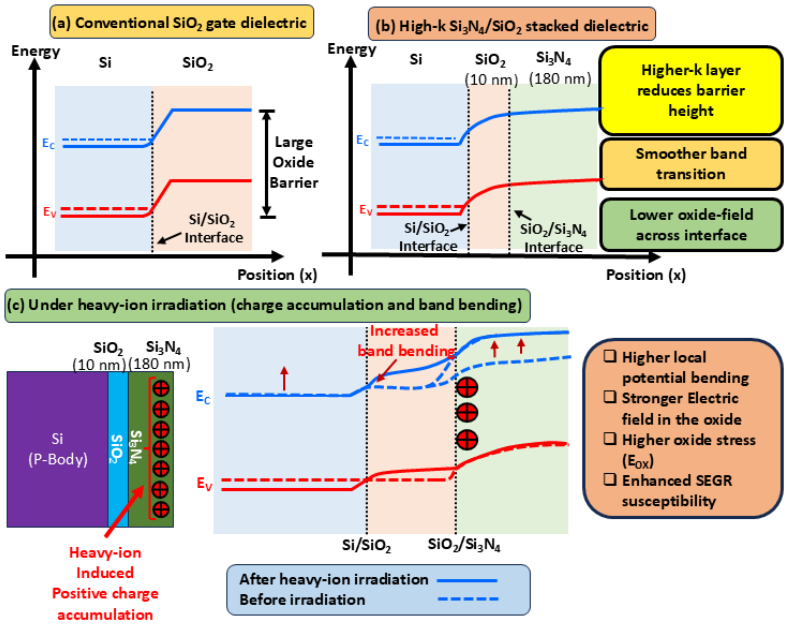

Fig. 5. Conceptual energy-band representation of (a) conventional SiO_2 dielectric, (b) proposed Si_3N_4/SiO_2 stacked dielectric, and (c) dielectric response under heavy-ion-induced charge accumulation illustrating the mechanism of oxide-field modulation and SEGR susceptibility.

TABLE III
PARAMETERS USED FOR HEAVY-ION RADIATION SIMULATION

Parameter	Value
Radius of the ion track (ω_0)	$0.07\ \mu$m
Peak charge generation time (t_0)	1×10^{-14} s
Characteristic time constant (t_c)	1×10^{-15} s
Linear energy transfer (LET)	$20, 37, and\ 40\ \mathrm{MeV \cdot cm^2/mg}$
Ion track length (l_0)	Full device thickness

has been employed. The device is biased under off-state (blocking) conditions with a high drain voltage while the gate and source terminals are grounded. Heavy-ion strikes are modeled using a Gaussian charge deposition profile along a vertical track passing through the device structure. The Linear Energy Transfer (LET) values considered in this study include 20, 37, and $40\ \mathrm{MeV \cdot cm^2/mg}$, representing low, moderate, and high radiation stress conditions. The strike location is selected near the trench gate region, which is known to be the most sensitive area for SEGR initiation. Transient simulations are performed to capture the dynamic evolution of electric field and charge distribution following the ion strike.

D. Model Calibration and Validation

The TCAD framework employed in this work incorporates multiple physical models to accurately capture carrier transport, impact ionization, mobility degradation, recombination processes, and heavy-ion-induced transient phenomena. The selected models were chosen to ensure reliable prediction of breakdown behavior, electric-field redistribution, and radiation-induced degradation mechanisms under both static and transient operating conditions. The Shockley-Read-Hall (SRH) recombination model is incorporated to account for carrier trapping and recombination effects during transient charge generation following heavy-ion irradiation. Concentration-dependent mobility models are employed to accurately capture carrier transport behavior within highly doped regions and under strong electric-field conditions. Impact-ionization models are included to accurately predict avalanche multiplication and breakdown behavior under high drain-bias conditions. Heavy-ion strike models are employed to reproduce transient carrier generation profiles associated with LET-induced charge deposition and SEGR susceptibility.

To ensure the reliability of the simulation framework, a two-step validation approach has been adopted. First, the TCAD model is calibrated against experimentally reported breakdown characteristics of a conventional trench VDMOS device [13]. As shown in Fig. 6, the simulated drain current closely follows the experimentally observed trend, accurately capturing the onset and progression of avalanche breakdown. The slight deviation near the breakdown region is attributed to process-dependent variations and measurement conditions not explicitly included in the simulation. This agreement confirms the validity of the physical models and parameter set used in this work.

Following calibration, the same set of physical models

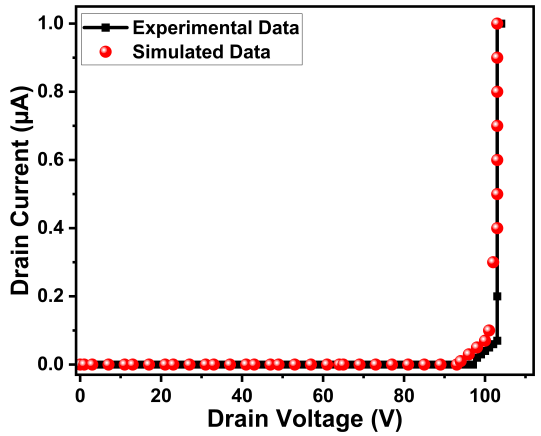

Fig. 6. Calibration of the TCAD simulation framework through comparison of simulated and experimentally reported breakdown characteristics of a conventional trench VDMOS device [13]. The simulated results show good agreement with experimental data in terms of breakdown voltage and current behavior. Minor deviations near the breakdown region arise due to idealized modeling assumptions and the absence of process-induced nonuniformities.

is consistently applied to all device structures analyzed in this work. To further support the validity of the simulation results, the obtained electrical characteristics and electric field distributions are compared with trends reported in prior experimental and simulation-based studies on trench VDMOS and high-k dielectric integration [43]. In particular, previously reported works demonstrate that (i) electric field crowding near trench corners governs breakdown behavior [32], (ii) high-k dielectric stacks redistribute the electric field and reduce peak oxide stress [30], and (iii) embedded structures such as floating regions can modulate the internal field profile [44]. The trends observed in the present work are consistent with these established findings, thereby reinforcing the reliability of the simulation-based analysis. The calibrated framework is therefore used to systematically investigate the impact of high-k Si_3N_4/SiO_2 stacked gate dielectric and P-type floating islands on electric field redistribution and SEGR mitigation.

III. Result and Discussion

A. Electric-Field Engineering Under Blocking Conditions

The PFI's various lengths, positions, and doping levels are intended to shield the device from radiation spikes. The objective is to increase the electric-field margin within the oxide layer rather than lower resistance or increase voltage limits. Structural field engineering effects on device behavior are initially studied at the conditions of static blocking, where the geometry of devices, doping profiles and dielectric configuration are the primary determinants of the distribution of the electric-fields. The analysis first addresses how the device redistributes electrical stress away from the gate oxide, providing a baseline prior to considering radiation-induced damage. Fig. 7 is used to depict the distribution of the electric-field in the high-k trench PFI VDMOS at various PFI doping concentrations. In the case of no PFI in the structure, the electric field is concentrated around the neck of the trench as a result of geometric field crowding at the oxide of the gate. The electric field in the vicinity of the gate oxide decreases gradually with the increased PFI doping concentration whereas the same rises in the PFI region. This action shows the shift of the intensity of the electric-fields between the trench gate and the floating islands, which comes in agreement with the increase in space-charge modulation in the drift region.

The analysis presented in this section is divided into two

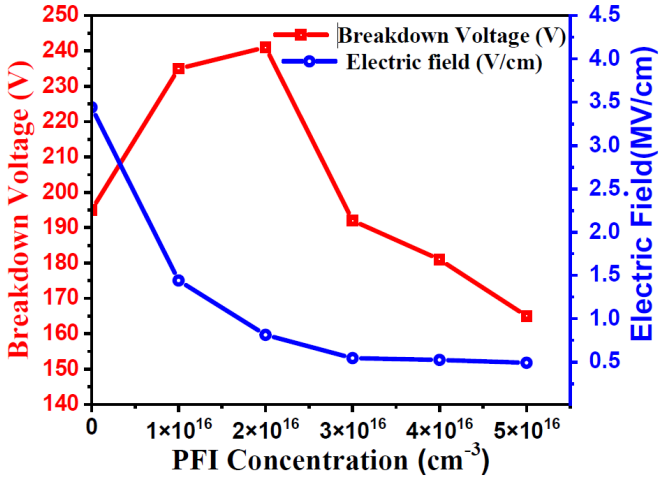

Fig. 7. Breakdown voltage and peak electric field response of the high-k trench PFI VDMOS as the PFI doping concentration is varied under blocking conditions.

parts: (i) static electric field distribution under blocking conditions, and (ii) transient behavior under heavy-ion irradiation leading to SEGR. The static analysis provides insight into the baseline electric field distribution within the device, while the transient analysis captures the dynamic response of the device under radiation-induced charge injection. The electric field in semiconductor devices is inherently a vector quantity, expressed as $\nabla\phi$, comprising both magnitude and directional components. In this work, the contour plots represent the magnitude of the electric field $|\mathbf{E}|$, which is commonly used to identify regions of peak electric stress relevant to breakdown and Single Event Gate Rupture (SEGR) phenomena. To complement this, electric field-line distributions are also presented, which provide qualitative insight into the direction and flow of the electric field within the device structure. The combined use of field magnitude contours and field-line plots enables a comprehensive understanding of both the intensity and directionality of the electric field. The analysis of the electric field distribution is critical for understanding the radiation response of the proposed device. Since SEGR is strongly driven by peak oxide electric field under heavy-ion irradiation, any structural modification that reduces or redistributes the electric field near the oxide interface directly contributes

to improved radiation hardness. Therefore, the following analysis focuses on evaluating how the proposed high-k and PFI integration modifies the electric field profile compared to the conventional structure. To clearly distinguish the contribution of each design element, a comparative analysis is first performed across four device configurations: (i) conventional trench VDMOS, (ii) trench VDMOS with high-k stacked gate dielectric, (iii) trench VDMOS with P-type floating islands (PFI), and (iv) the proposed structure combining high-k dielectric and PFI. This comparison enables isolation of the individual and combined effects of dielectric field partitioning and drift-region field modulation on electric-field distribution. To further illustrate the mechanism of electric-field redistribution, Fig. 8 presents two-dimensional electric field contour plots along with electric field line distributions in Fig. 9 for the conventional, high-k, PFI, and combined high-k + PFI VDMOS structures under blocking conditions.

In the conventional device, strong electric-field crowding is observed at the trench neck, where field lines converge sharply toward the gate oxide interface. This localized concentration of electric field results in a high oxide-normal electric field, which is a primary contributor to SEGR susceptibility. With the introduction of a high-k dielectric, the magnitude of the electric field near the trench sidewall is reduced due to dielectric screening, leading to a more distributed field profile. However, the field lines still exhibit a tendency to terminate near the oxide interface. In the PFI-based structure, the electric field distribution is altered due to space-charge modulation in the drift region, resulting in partial redistribution of field lines away from the trench. Nevertheless, localized regions of field concentration still persist. In contrast, the proposed high-k + PFI structure demonstrates a significantly improved field distribution. The electric field magnitude at the trench corner is reduced, and the field lines are more uniformly distributed into the drift region, with reduced convergence at the oxide interface. This indicates that the combined structure effectively redistributes both the magnitude and direction of the electric field, thereby reducing the oxide-normal component and improving SEGR resilience. Each contour plot uses an independent color scale to highlight the spatial distribution of the electric field. The absolute peak values are indicated in the legend for quantitative comparison. The peak electric field reduces from 0.81 MV/cm (conventional) to 0.20 MV/cm (high-k) and 0.18 MV/cm (combined). The electric-field contour and vector distributions clearly demonstrate distinct roles of the individual design modifications. In the conventional device, strong electric-field crowding is observed at the trench corner, resulting in a localized peak stress at the oxide interface. The introduction of a high-k dielectric reduces this peak through enhanced permittivity, resulting in moderate field smoothing near the gate region. In contrast, the P-type floating island effectively redistributes the electric field deeper into the drift region, shifting the peak away from the oxide interface and promoting lateral spreading. The combined structure integrates both mechanisms, leading to a more uniform electric-field profile with reduced peak intensity and improved spatial distribution. This cooperative field modulation is critical for mitigating SEGR susceptibility.

Compared with the standard trench VDMOS, depicted in Fig. 10, it is evident that the baseline structure is not very flexible in redistributing the electric-field stress. In the conventional device, the oxide-normal electric field at the trench sidewall approaches the intrinsic breakdown strength of SiO_2 under blocking conditions, leaving a narrow margin for additional transient stress. This intrinsic field concentration explains the heightened susceptibility of the conventional structure to gate-oxide failure. The contour plots shown in this work represent electric-field magnitude distributions, whereas field-line plots are used to visualize electric-field directionality and vector behavior.

The effect of PFI length on blocking behavior is examined in Fig. 11 and Fig. 12. As the PFI length is increased, the breakdown voltage initially improves due to more effective interception of electric-field lines within the drift region. Beyond a certain length, however, excessive field compression near the floating islands leads to a reduction in breakdown voltage, indicating a trade-off between field redistribution and drift-region depletion efficiency. Corresponding electric-field profiles confirm that longer PFI structures reduce the oxide-normal electric field at the trench gate while increasing the field intensity within the floating islands.

The sensitivity of electric-field redistribution to PFI placement is further explored in Figs. 13–15. Shifting the PFI position along the drift region modifies the spatial distribution of the electric field, with certain placements providing a more favorable balance between reduced gate-oxide field and sustained breakdown voltage.

In order to factor the effect of dielectric and drift-region field redistribution on the behavior of SEGR, the background n-drift doping concentration is deliberately maintained constant during this experiment, and no combined optimization of drift doping and floating-island control is sought. These findings prove that the successful field control not only requires PFI doping but also, its spatial alignment with the depletion region developed under blocking bias. Fig. 16 and Fig. 17 summarize the effect of the incorporation of PFI on the conduction properties. PFI existence brings about the moderate augmentation of individual on-resistance owing to the geometrical constriction of current flow in the drift area. The difference in the PFI doping and the vertical position with respect to the trench bottom is found to have a relatively lower effect on the precise on-resistance, and the largest effect is the physical impediment of the floating islands. Increasing the number of PFI regions leads to an approximately linear increase in on-resistance, reflecting cumulative conduction path narrowing.

Overall, the static blocking analysis demonstrates that the combined use of a high-k gate dielectric and PFI-based drift-region engineering enables controlled redistribution of electric-field stress away from the trench gate. This redistribution is achieved with a bounded penalty in conduction performance and forms the foundation for improved oxide-field margin under transient radiation conditions, which is examined in the following subsection.

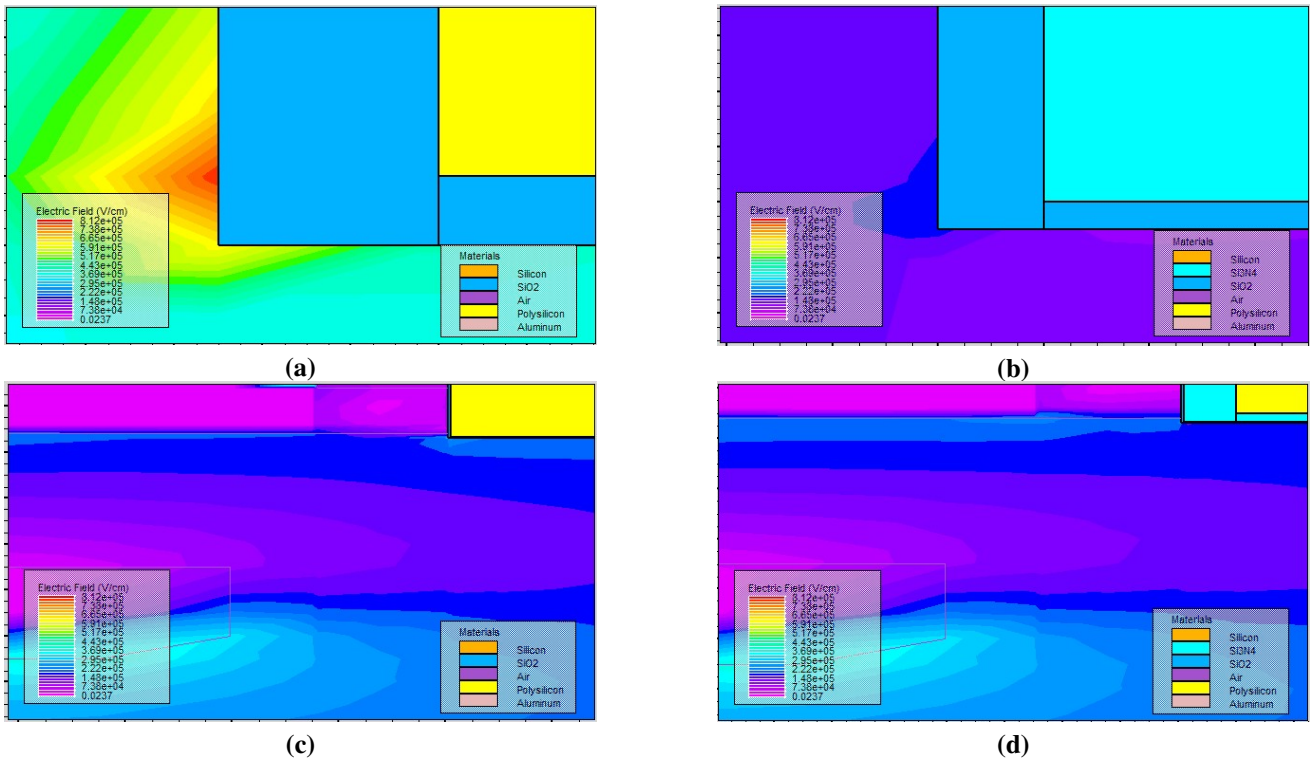

Fig. 8. Electric field contour for different device configurations under blocking conditions: (a) Conventional VDMOS, (b) High-k VDMOS, (c) PFI VDMOS, and (d) Proposed High-k + PFI VDMOS.

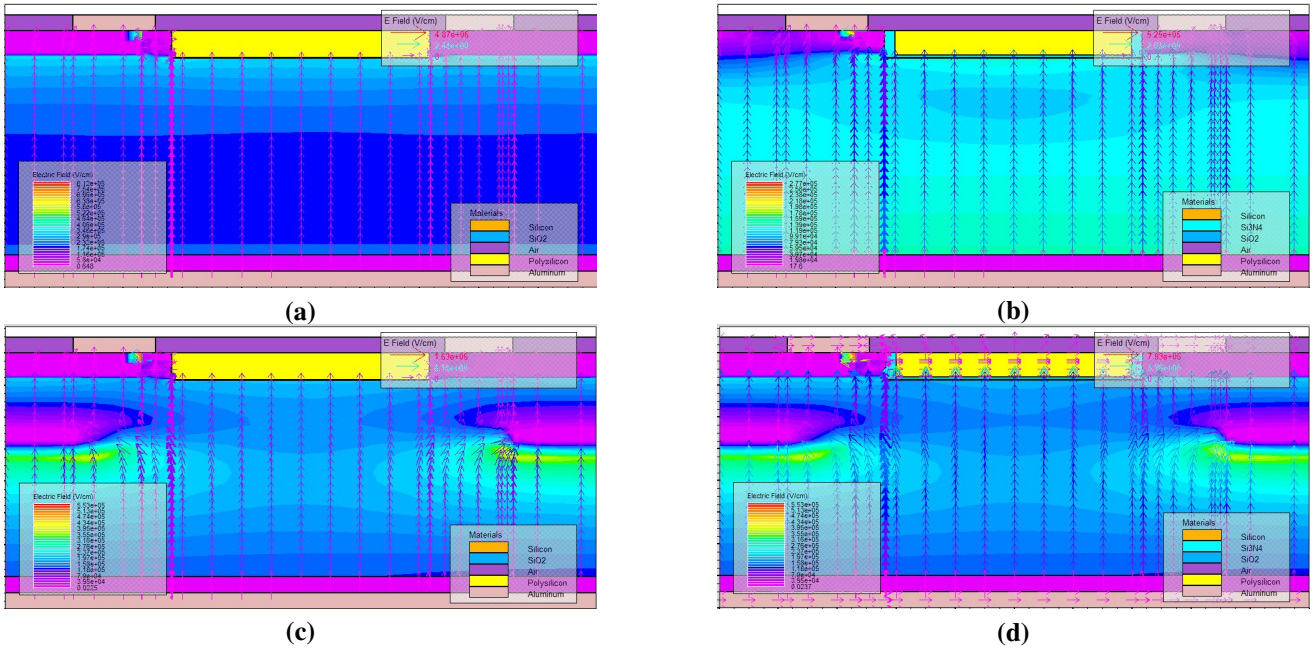

Fig. 9. Field-line distribution for different device configurations under blocking conditions: (a) Conventional VDMOS, (b) High-k VDMOS, (c) PFI VDMOS, and (d) Proposed High-k + PFI VDMOS.

The ranges of parameters investigated in this paper are chosen to reflect the main electric-field redistribution processes that should be involved in the process of SEGR mitigation, but not to exhaustively identify a worldwide multi-objective optimum.

B. Electric Field Redistribution Mechanism

To establish a clear physical understanding of the proposed design, a comparative analysis of the electric-field distribution is performed using two-dimensional contour plots and electric field line distributions for the conventional, high-k, PFI, and combined high-k + PFI VDMOS structures. At the

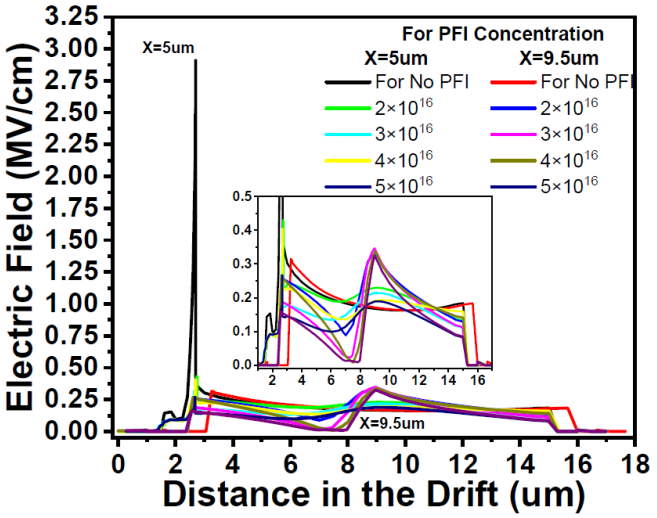

Fig. 10. Electric-field distribution along the drift region comparing the high-k trench PFI VDMOS and the conventional trench VDMOS under blocking conditions.

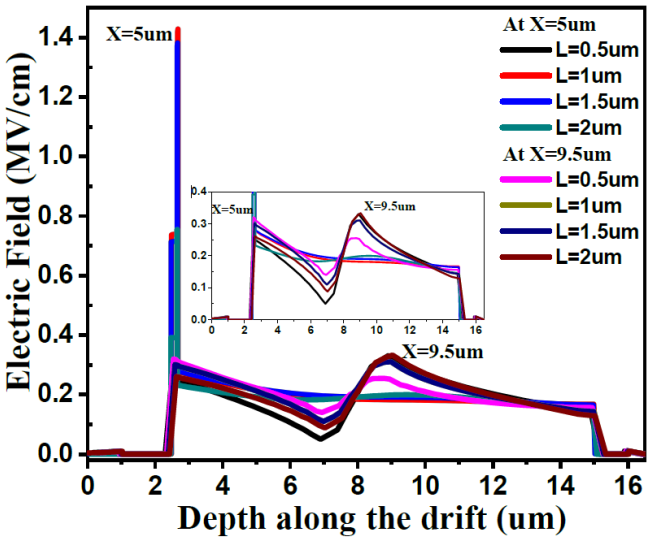

Fig. 12. Electric-field distribution across the gate oxide (X = 5 μm) and at the PFI location (X = 9.5 μm) for different PFI lengths.

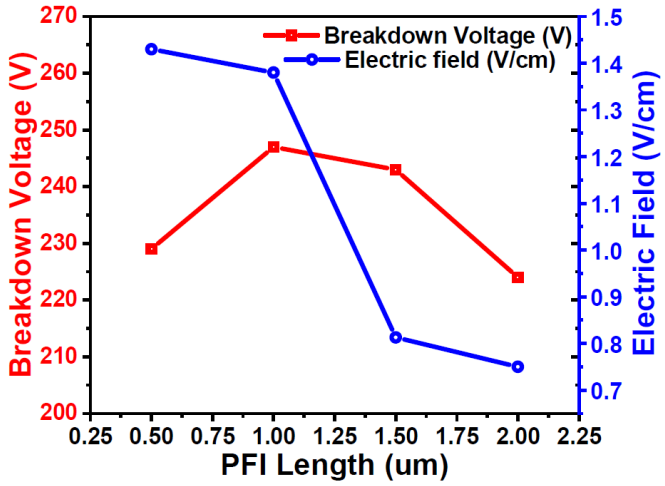

Fig. 11. Variation of breakdown voltage and peak electric field as a function of PFI conduction section for different PFI lengths.

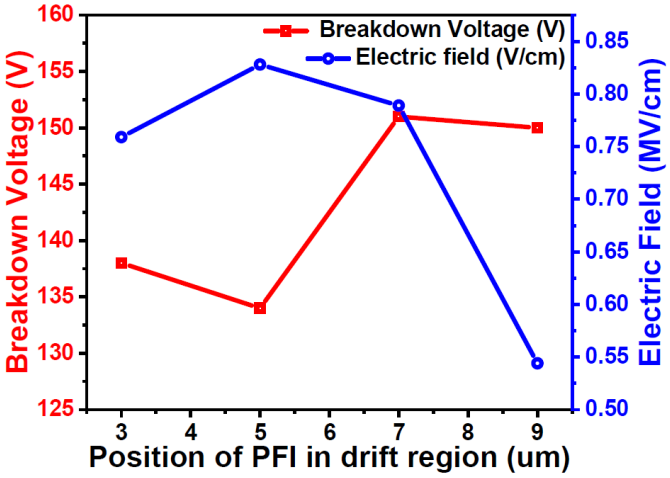

Fig. 13. Electric-field distribution across the gate oxide (X = 5 μm) and at the PFI location (X = 9.5 μm) for different PFI positions in the drift region.

trench corner, the conventional VDMOS exhibits pronounced electric-field crowding, with peak field intensity localized near the trench neck, as shown in Fig. 9(a). The contour plots show a sharp gradient in this region, while the field-line distribution indicates strong convergence of electric-field lines toward the gate oxide interface, as shown in Fig. 8(a). This behavior results in a high oxide-normal electric field, making the structure highly susceptible to SEGR. In high-k VDMOS, the peak electric field near the trench sidewall is reduced due to dielectric screening. The contour distribution becomes more uniform compared to the conventional structure, as shown in Fig. 8(b); however, as shown in Fig. 9(b), the electric field lines still tend to terminate at the oxide interface, indicating that field redirection is limited despite the reduction in magnitude. For the PFI-based structure, the electric field is redistributed due to space-charge modulation introduced by the floating islands, as shown in Fig. 9(c). The contour plots indicate a shift of the electric field into the drift region, and the field-line distribution shows partial diversion of electric-field lines away from the trench corner, as shown in Fig. 8(c). However, localized regions of field concentration are still observed, indicating that PFI alone does not fully suppress field crowding at critical oxide regions. In contrast, the proposed high-k + PFI structure demonstrates a significantly improved electric-field profile as shown in Fig. 9(d). The contour plots show a substantial reduction in peak electric field at the trench corner, along with a more uniform distribution across the drift region, as shown in Fig. 8(d). More importantly, the electric field lines are redistributed, becoming less concentrated at the oxide interface and more evenly distributed across the drift region. This indicates that the combined structure effectively modifies both the magnitude and direction of the electric field. A similar trend is observed at the trench bottom. The conventional structure exhibits a non-uniform field distribution

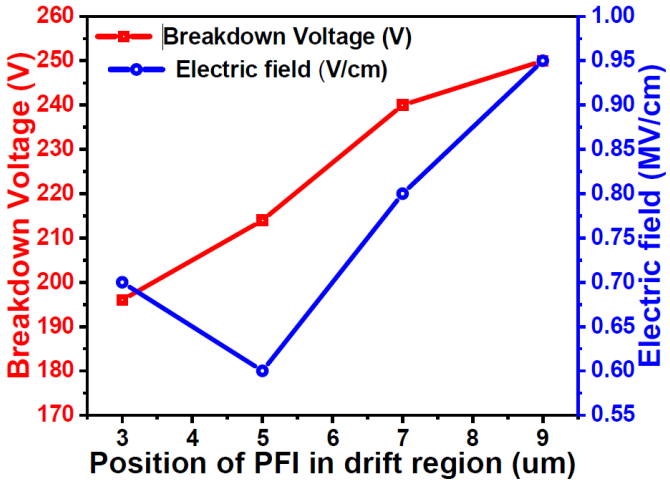

Fig. 14. Variation of breakdown voltage and peak electric field for different PFI positions at a fixed PFI length of 1.5 μm and doping concentration of $2 \times 10^{16}\ \mathrm{cm}^{-3}$.

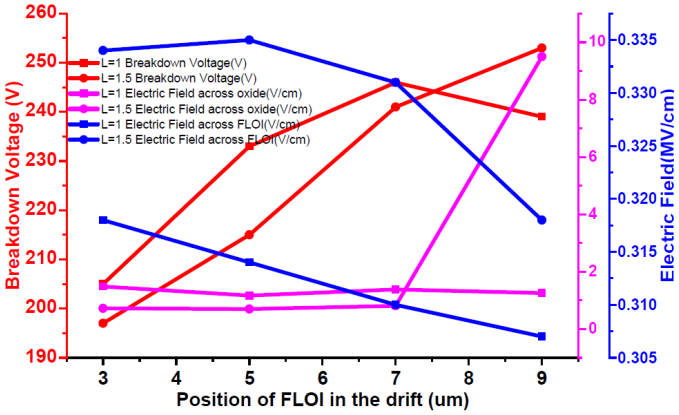

Fig. 15. Combined effect of PFI length and position on breakdown voltage and electric-field distribution.

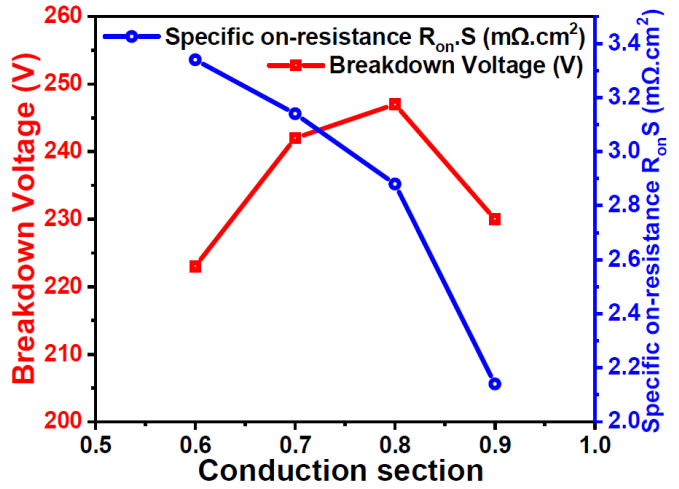

Fig. 16. Breakdown voltage and specific on-resistance as functions of the PFI conduction section for various PFI lengths.

with localized high-field regions, while the high-k and PFI structures provide partial improvement. The combined structure, however, results in a more uniform potential drop and reduced field concentration, indicating improved electrostatic stability across the device. These results confirm that the reduction of oxide-normal electric field is achieved not only through magnitude suppression but also through directional redistribution of electric field lines away from the gate oxide interface. This combined electrostatic effect plays a critical role in enhancing SEGR robustness under heavy-ion irradiation conditions. The observed reduction in peak electric field near the gate oxide region in the proposed structure directly impacts the device behavior under radiation conditions. During heavy-ion events, the transient increase in electric field is superimposed on the steady-state field. By lowering the initial peak electric field and redistributing it across the device, the proposed structure reduces the likelihood of exceeding the oxide breakdown threshold. This establishes a direct link between electric field engineering and SEGR mitigation in the proposed device. After establishing static electric-field behavior, transient heavy-ion-induced electric-field evolution is investigated to evaluate SEGR susceptibility.

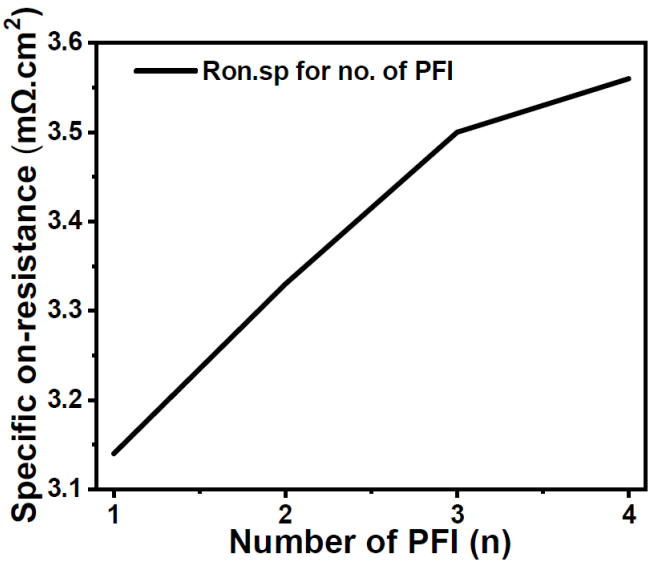

Fig. 17. Specific on-resistance as a function of the number of PFI regions incorporated in the drift layer.

C. SEGR Response of Conventional and Proposed Devices

The transient response of the device structures to heavy-ion irradiation is analyzed next to evaluate the impact of electric-field engineering on single-event gate rupture behavior. In all cases, SEGR onset is assessed using the oxide-normal electric field criterion defined in Section II-C, with gate current treated as a secondary indicator of dielectric rupture.

Fig. 18 and Fig. 19 present the transient oxide-normal electric field response of the conventional trench VDMOS under heavy-ion irradiation at a fixed linear energy transfer (LET) of $20\ \mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$, with the gate voltage held at $V_{GS} = 0$ V. Two drain-voltage regimes are examined to assess device behavior under both high-field blocking and reduced electric-stress conditions. At elevated drain voltages ($V_{DS} = 80$–130 V), the oxide-normal electric field at the trench sidewall

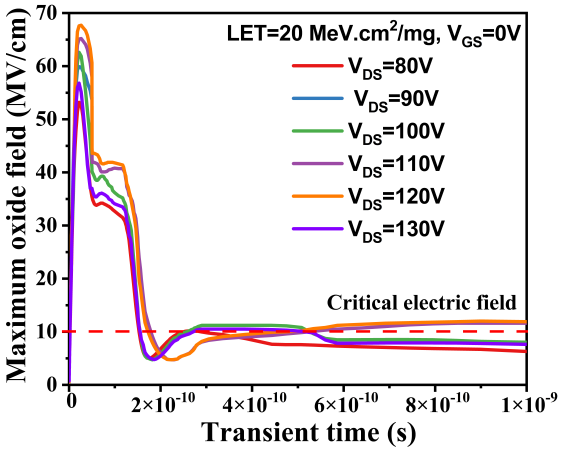

Fig. 18. Transient oxide-normal electric field response of the conventional trench VDMOS under heavy-ion irradiation for LET = 20 $\mathrm{MeV \cdot cm^2/mg}$, V_{GS} = 0 V, and V_{DS} ranging from 80 V to 130 V. The dashed line indicates the approximate critical electric field of SiO_2 used as the SEGR failure threshold.

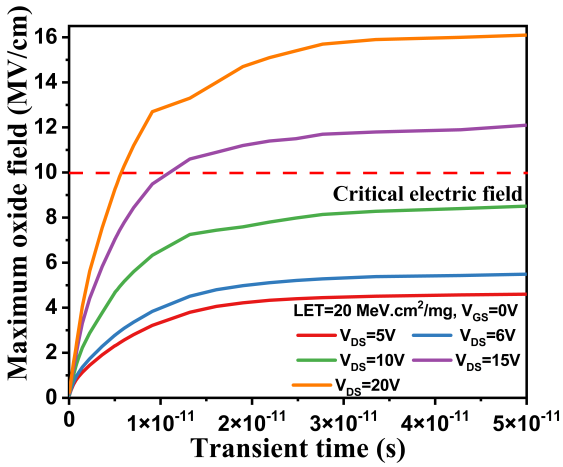

Fig. 19. Transient oxide-normal electric field response of the conventional trench VDMOS under heavy-ion irradiation for LET = 20 $\mathrm{MeV \cdot cm^2/mg}$, V_{GS} = 0 V, and V_{DS} ranging from 5 V to 20 V. The dashed line indicates the approximate critical electric field of SiO_2 used as the SEGR failure threshold.

exceeds the critical breakdown strength of SiO_2 immediately following the ion strike, indicating an absence of available oxide field margin in the conventional structure.

When the drain voltage is reduced to lower values ($V_{DS} = 5$–20 V), the oxide electric field remains below the SEGR failure threshold only up to a limited bias range, beyond which it rapidly approaches or exceeds the critical field. This narrow operating window reflects the intrinsic electric-field crowding at the trench neck and the limited ability of the baseline structure to accommodate transient radiation-induced charge.

Under heavy-ion irradiation, a dense track of electron–hole pairs is generated within a very short time scale (on the order of picoseconds). The rapid deposition of charge leads to a transient increase in local electric field, particularly near the gate oxide region. The transport of these carriers toward the terminals and the subsequent redistribution of potential occur over a finite transit time, during which the peak electric field may exceed the oxide breakdown threshold. The proposed high-k + PFI structure reduces the initial electric field magnitude and redistributes the electric field within the device, thereby limiting the magnitude of transient field spikes. This reduces the likelihood of exceeding the critical oxide field during the carrier transit period, resulting in improved resistance to SEGR. To systematically evaluate the radiation response, simulations are performed for multiple LET values (20, 37, and 40 MeV·cm²/mg) across conventional VDMOS, and the proposed combined structure. This enables a comparative analysis of the impact of electric field engineering on SEGR susceptibility under varying radiation intensities.

Fig. 20 (a)-(f) shows the transient oxide-normal electric field response of the proposed high-k trench PFI VDMOS under progressively increasing radiation and electrical stress conditions. The simulations are performed for LET values of 20, 37, and 40 $\mathrm{MeV \cdot cm^2/mg}$, with V_{DS} varied from 80 V to 130 V and V_{GS} set to 0 V and −10 V. At moderate LET values, the proposed structure maintains oxide-normal electric fields below the SEGR failure threshold over a wide range of drain voltages for both zero and negative gate bias, demonstrating effective suppression of peak oxide field excursions following the ion strike. With increasing LET to higher levels, the increasing range of drain voltage at which the oxide-normal electric field does not exceed the failure threshold is seen, an indication of enhanced radiation-created charge density and enhanced transient field perturbations. The alternative technique of immunizing oxide electric-field stress by using negative gate bias which augments the vertical field component at the trench sidewall is additionally important. Though under these compounded stress conditions, the proposed structure still demonstrates a far larger oxide field margin than at the conventional device, and the initiation of SEGR only at higher drain voltages or LET. The differences of reaction of the two structures help emphasize the key position of redistribution of the electric field in the control of SEGR behavior. Only stacked gate dielectrics or floating islands are also capable of reducing the oxide electric-field stress in structures to some degree. But the findings of this experiment indicate that successful suppression of electric-field crowding with transient conditions of the radiation necessitates the joint effort of the redistribution of the dielectric fields in the gate and charging modulation in the drift region. With the traditional trench VDMOS, holes created by radiations concentrate around the trench neckline and directly enhance the high oxide-normal electric field, a process which results in oxide rupture. This dielectric failure is the cause of the sudden rise in the current at the gate which follows. Dielectric field partitioning at the trench gate and space-charge modulation in the drift region in the proposed device, together, limit the strength of the transient oxide field enhancement, and therefore, postpone the occurrence of gate rupture.

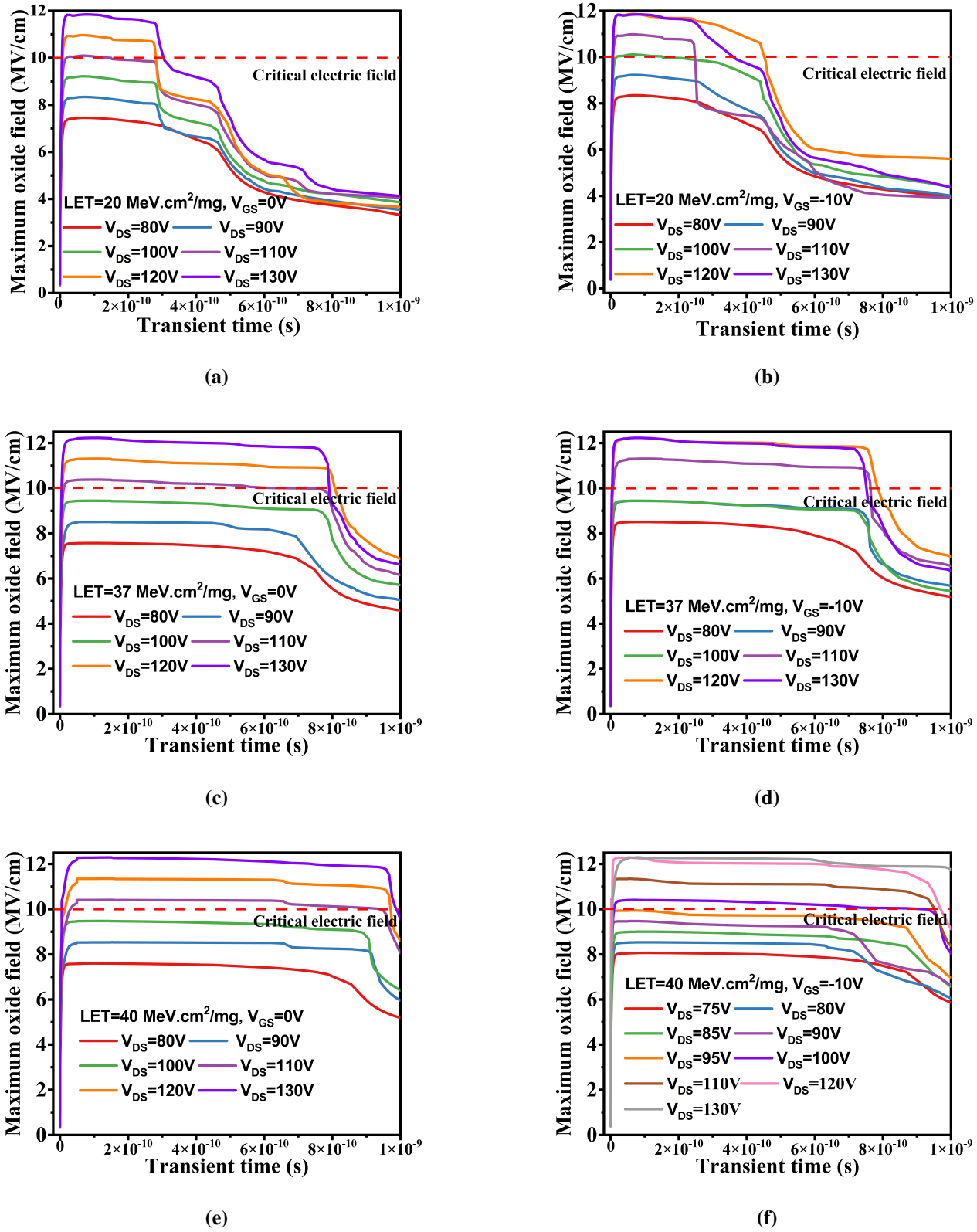

Fig. 20. Transient oxide-normal electric-field response of the proposed high-k trench PFI VDMOS under heavy-ion irradiation at different LET conditions. (a) LET = 20 MeV·cm^2/mg with $V_{GS} = 0$ V; (b) LET = 20 MeV·cm^2/mg with $V_{GS} = -10$ V; (c) LET = 37 MeV·cm^2/mg with $V_{GS} = 0$ V; (d) LET = 37 MeV·cm^2/mg with $V_{GS} = -10$ V; (e) LET = 40 MeV·cm^2/mg with $V_{GS} = 0$ V; and (f) LET = 40 MeV·cm^2/mg with $V_{GS} = -10$ V. In all cases, the plots show the transient maximum oxide electric field for different V_{DS} bias conditions. The dashed line indicates the approximate critical electric field of SiO_2 used as the approximate SEGR failure threshold.

TABLE IV
COMPARISON OF RECENT FIELD-ENGINEERED AND SEGR-AWARE VDMOS STRUCTURES

Ref.	**Device Structure**	$R_{\mathrm{on,sp}}$ **(mΩ·cm^2)**	**BV (V)**	**FOM (MW cm^{-2})**	**Peak $\lvert E\rvert$ Behavior**	**SEGR Considered**
Luo et al. [41]	High-k pillar below trench	1.2	179	26.7	High-k weakens the lateral electric field and enhances the vertical field strength	No
Krishnamurthy et al. [29]	Trench shielded UMOSFET	1.2	179	26.7	Reduced field peaks in drift region	No
Chen et al. [15]	Trench VDMOS with termination	0.809	230	0.083	Partial reduction near termination oxide	Yes
Zhao et al. [23]	Step floating-island VDMOS	7.77	326	13.68	Multiple electric-field peaks for optimized field distribution	No
Yao et al. [37]	SiC trench MOSFET with extended high-k	2.1	1600	1219	Redistributed electric field near trench gate	No
Wang et al. [13]	Radiation-hardened trench VDMOS	14	100	–	Reduced peak oxide electric field	Yes
Zhang et al. [14]	Stepped source and optimized LOCOS	–	–	–	Partial reduction near gate oxide	Yes
Yao et al. [36]	4H-SiC SJ MOSFET with high-k split gate	2.13	1814	1545	Reduced electric field at Si–SiO_2 interface	No
This Work	**High-k with floating-island VDMOS**	**3.1**	**242**	**18.65**	**Significant reduction in peak electric field near Si–SiO_2 interface**	**Yes**

TABLE V
HIGH-VOLTAGE AND SIC DEVICES (CONTEXTUAL REFERENCE ONLY)

Author	Material / method	Device type	$R_{\mathrm{on,sp}}$ (mΩ·cm^2)	BV (V)	FOM (MW cm^{-2})
Saito et al., [42]	Si / Simulation	Superjunction MOSFET	15.5	680	1.8
Muthuseenu et al., [28]	Si / Experiment	SJ MOSFET (SEGR-hardened)	450	650	–
Zhang et al., [33]	Si / Experiment	SiC trench MOSFET	2.1	1600	1219
Infineon SPA15N60C3 [45]	Si / Datasheet	Commercial SJ MOSFET	0.25	600	1440
Microchip ARF461A/BG [46]	Si / Datasheet	RF power MOSFET	7.69	1000	130

These findings indicate that the susceptibility of SEGR under transient conditions in trench VDMOS devices is largely determined by the accessibility of an oxide field margin. Physically effective approaches to reducing SEGR without changing the underlying conduction mechanism of the device structural and dielectric design selections that redistribute electric-field stresses that are off the gate oxide. More complicated radiation cases, such as oblique ion incidence, multiple strike case and cumulative thermal effects are not considered in the current research but will be determined in the future study.

D. Comparative Discussion and Design Implications

The aforementioned findings demonstrate that SEGR behavior in trench-based power MOSFETs is largely dependent on how the electric field redistributes within the device. While direct quantitative comparison across different device technologies is often complicated by variations in geometry, voltage rating, and material system, a qualitative comparison with previously reported silicon-based trench VDMOS structures provides useful context for interpreting the present findings. Although the proposed structure adds more dielectric interfaces and embedded floating region, the issues of interface traps density, thermal budgets management, and process variability are admitted and are major areas of experimental research in the future.

It must be pointed out that no direct quantitative comparison of various voltage classes and device technologies is intended, the data in Tables III and IV is presented to put in perspective the SEGR-oriented design trade-offs and not to compare absolute measures of performance. To quantitatively evaluate the performance of the proposed structure, a figure of merit (FoM) is considered. In power MOSFETs, a commonly used FoM is the trade-off between breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$), which reflects the efficiency of the device in handling high voltage with minimal conduction loss. This is often expressed as:

$$\mathrm{FoM}_1 = \frac{\mathrm{BV}^2}{R_{on,sp}} \tag{7}$$

In addition, for switching applications, the product of gate charge (Q_g) and on-resistance (R_{on}) is often used as a switching FoM, representing the balance between conduction loss and switching speed:

$$\mathrm{FoM}_2 = Q_g \times R_{on} \tag{8}$$

A lower value for FoM_2 indicates improved overall device performance. In the context of this work, the FoM is used not only to evaluate electrical performance but also to ensure that the proposed SEGR mitigation strategy does not degrade the fundamental performance characteristics of the device. As summarized in Table III and IV, previously reported SEGR mitigation strategies typically emphasize either dielectric engineering or drift-region field modification as isolated approaches. High-k or stacked gate dielectrics primarily reduce oxide electric-field stress through dielectric field partitioning, whereas structural techniques such as floating islands or super-junction architectures reshape the electric-field profile within the drift region. While each method provides partial mitigation, residual electric-field crowding near the trench neck can persist under transient radiation conditions.

In the present structure, the combined use of a stacked high-k Si_3N_4/SiO_2 gate dielectric and p-type floating islands

enables concurrent control of dielectric field partitioning at the trench gate and space-charge modulation within the drift region. This coupled field-engineering approach increases the available oxide field margin under heavy-ion irradiation without relying on excessive oxide thickness or substantial alteration of the vertical conduction path. A corresponding heightened on-resistance is limited, and a natural yet controllable compromise between the control of electric-fields and conductivity. In a larger design viewpoint, these findings demonstrate that the susceptibility of SEGR of a trench VDMOS device is controlled not only by the properties of dielectric materials, but also by the presence of transient oxide electric-field margin under joint electrical and radiation stress conditions. Structural design strategies that redistribute electric-field stress away from the gate oxide, while remaining compatible with conventional silicon power MOSFET fabrication, offer a physically grounded pathway for SEGR mitigation in radiation-exposed and high-reliability applications.

In this work, we address this gap by systematically analyzing the combined effect of a high-k Si_3N_4/SiO_2 stacked gate dielectric and P-type floating islands, demonstrating that their co-integration results in a synergistic redistribution of the electric field, reducing peak oxide-normal electric field and mitigating SEGR under heavy-ion irradiation conditions. From a fabrication perspective, the proposed high-k + PFI trench VDMOS introduces additional structural complexity compared to conventional trench devices; due to the integration of P-type floating islands within the drift region and the use of a high-k Si_3N_4/SiO_2 stacked gate dielectric. The realization of floating islands requires precise control over implantation and diffusion processes to achieve the desired spatial distribution and charge balance [47]. Similarly, integrating high-k materials requires careful management of interface quality, fixed charges, and the thermal budget [48]. However, the individual process modules required for its realization are compatible with modern power semiconductor manufacturing technologies. Trench etching, dielectric deposition, ion implantation, and epitaxial growth are already well established in contemporary trench-MOSFET and superjunction fabrication processes. The integration of high-k dielectric materials within trench-gate structures has been widely investigated in advanced power devices to improve electric-field control and breakdown characteristics. Similarly, floating-island and charge-balancing concepts have been experimentally demonstrated through localized implantation and multi-epitaxial growth techniques. Therefore, the proposed structure does not rely on fundamentally new fabrication steps, but rather on the controlled integration of existing process technologies [49]–[51].

Nevertheless, precise control of dielectric interfaces, floating-island alignment, thermal budget, and process-induced interface traps remains important for practical implementation. These factors may influence oxide reliability and electric-field uniformity under radiation conditions and should be investigated further through experimental fabrication studies. The proposed design, therefore, represents a physically realizable extension of existing trench power MOSFET technologies toward radiation-resilient applications [52], [53]. So, the proposed structure is considered feasible from a technological standpoint, although process optimization and experimental validation remain subjects for future work.

To further validate the effectiveness of the proposed structure, the obtained results are compared with previously reported works on high-k-based and field-engineered VDMOS devices. Prior studies have demonstrated improvements in breakdown voltage and on-resistance trade-offs through dielectric engineering and structural modifications. However, these works primarily focus on static performance metrics and do not explicitly address radiation-induced degradation mechanisms such as SEGR. Table III gives the comparison of the recent field-engineered and SEGR-aware VDMOS Structure. In contrast, the proposed structure achieves improved electric field distribution and reduced peak oxide electric field under radiation conditions, while maintaining competitive electrical performance. This highlights the advantage of the combined high-k+ PFI approach in simultaneously addressing both performance and radiation reliability, which has not been extensively explored in prior works.

As summarized in Table III, previously reported works primarily focus on either dielectric engineering or structural field modulation as independent approaches to improve electrical performance in power MOSFETs. High-k dielectric integration mainly reduces electric-field intensity near the trench gate, whereas floating-island techniques redistribute the electric field within the drift region to improve the BV–Ron trade-off. SEGR-oriented approaches, on the other hand, primarily target localized oxide-field suppression through structural hardening. In contrast, the proposed high-k + PFI VDMOS combines dielectric field modulation and drift-region charge redistribution within a single structure. This coupled field-engineering approach simultaneously reduces the peak electric-field magnitude near the gate oxide and improves electric-field uniformity under heavy-ion irradiation conditions. As a result, the proposed device establishes a balanced benchmark between electrical performance optimization and SEGR robustness."

IV. Conclusion

SEGR in trench VDMOS devices is governed by transient excursions of the oxide-normal electric field at the trench neck rather than by steady-state breakdown considerations alone. In conventional trench structures, geometric field crowding near the gate oxide leaves a limited margin to accommodate radiation-induced charge transport, making the device inherently vulnerable to SEGR under combined electrical and radiation stress.

In this work, a coupled electric-field engineering approach has been examined through TCAD simulations by integrating a stacked high-k Si_3N_4/SiO_2 gate dielectric with p-type floating islands embedded in the drift region. The stacked dielectric redistributes the voltage drop across the gate insulator, reducing the electric-field stress within the SiO_2 layer, while the floating

islands modulate the space-charge distribution in the drift region and intercept electric-field lines originating from the drain. Together, these mechanisms redistribute electric-field intensity away from the trench gate under both static blocking and transient heavy-ion irradiation. The results show that this coupled field-control strategy substantially increases the available oxide field margin under heavy-ion strikes, delaying the onset of SEGR over a wide range of drain bias, gate bias, and linear energy transfer conditions. This improvement is achieved without altering the fundamental vertical conduction mechanism of the device, and with a bounded trade-off in specific on-resistance.

More broadly, the present study highlights that effective SEGR mitigation in silicon trench power MOSFETs requires coordinated control of dielectric field partitioning and drift-region electric-field shaping. Combining the two offers a workable, physics-based method for enhancing radiation tolerance in power devices for high-reliability settings. Furthermore, the proposed structure is compatible with existing trench-based fabrication technologies, making it a promising candidate for practical implementation in radiation-hardened power devices.

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