Crosstalk Reduction in High-Speed Microstrip Interconnects Using a Greek Key Guard Trace

Gobinath Arumugam, Suresh Kumar Natarajan, Rajeswari Packianathan, and Mohamed Salah Karoui, *Senior Member, IEEE*

***Abstract*— This paper presents a compact technique for suppressing near-end crosstalk (NEXT) and far-end crosstalk (FEXT) in high-speed microstrip interconnects using a Greek key patterned defective microstrip guard trace. The proposed structure modifies the electromagnetic coupling between adjacent transmission lines by reducing mutual inductive coupling while increasing capacitive coupling, thereby improving signal isolation without increasing the spacing between signal traces. A comprehensive parametric study was performed using ANSYS HFSS to investigate the influence of slot width and unit-cell spacing on crosstalk behavior. Practical slot widths ranging from 0.1 mm to 0.25 mm were considered to ensure compatibility with standard PCB fabrication processes. The optimized configuration, with a slot width of 0.1 mm and unit-cell spacing of 1.0 mm, achieves significant crosstalk suppression, providing approximately −54.4 dB NEXT and −48.23 dB FEXT at 10 GHz. The extracted inductive and capacitive parameters confirm that the proposed guard trace effectively balances inductive and capacitive coupling mechanisms, leading to substantial reduction of electromagnetic interference in high-density high-speed PCB interconnects.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/10483

***Index Terms*— Crosstalk reduction, Greek key guard trace, High-speed PCB, Microstrip interconnects, Near-end crosstalk, Far-end crosstalk, Signal integrity**

I. Introduction

HIGH-SPEED electronics depend on a densely packed microstrip routing system that provides high data rates and a compact printed circuit board (PCB) design. The simulation data shows that when the trace spacing is decreased, the near-end and far-end electromagnetic coupling from the aggressor signal on microstrip lines increases, resulting in near-end crosstalk (NEXT) and far-end crosstalk (FEXT), respectively. Traditional methods like trace spacing increase, via-fenced trace, and controlled impedance routing can be used to counter the crosstalk issues to a certain extent. But its effectiveness is negligible when dealing with a high-density PCB design where routing space is limited [1–4].

To overcome these constraints, a substantial number of studies have explored the purposeful alteration of the local electromagnetic environment around the coupled interconnects by the use of transmission line structures. The improvement and use of patterned ground planes, defected microstrip lines, and impedance-optimized geometries have explored the possibility to optimize the pathway to couple without adding to the routing area [5]. Despite the existence of various switch capacitor and resistor switch crosstalk cancelations presented previously within the current literature, most are efficient solely within a certain frequency range and make use of complex geometries, hence requiring an advanced generalized crosstalk compensation to lessen the impact of crosstalk within a miniaturized high-speed PCB.

Crosstalk in coupled microstrip lines originates from inherent inductive and capacitive coupling between adjacent traces. The effectiveness of conventional mitigation techniques, such as increased line spacing and guard traces, has been widely validated. However, as operating speeds and routing densities continue to increase, the effectiveness of spacing-based approaches gradually diminishes, limiting overall signal integrity performance [6 – 9]. Experimental studies have shown that introducing additional conductors between coupled lines can improve crosstalk isolation by enhancing grounding and current return paths [10]. In particular, via-based guard trace structures have been extensively studied and validated, demonstrating that via placement and density play a critical role in achieving effective electromagnetic isolation in RF and high-speed PCB designs [11]. Even though bandwidth via-stitched guard trace solutions provide better suppression performances for bandwidth, inappropriate spacing for via lines and high discontinuity can affect signal transmission performances [12]. More complex transmission line topologies have been explored for electromagnetic coupling. Serpentine or stepped impedance and non-uniform lines change current and magnetic-field distribution principles in an modest increase in NEXT and FEXT suppression levels [13]. Serpentine micro-strip lines

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have been proposed for suppressing far-end crosstalk and jitter in high-speed interfaces for DRAM modules based on the principle of vertical coupling; these lines do not increase suppression levels for reduction in near-end crosstalk or couplings in copper interconnects used in high-speed interfaces for DRAM modules [14].

Wide band delay lines, material-based solutions, and structured or corrugated transmission lines have been proposed and have better high frequency characteristics with increased complexity in layout [15] to [18].

More recently, defected, resonating microstrips have also been explored for broadband crosstalk reduction. Periodic line transmits lines, as well as discontinuous guard line configurations, have also reduced far-end crosstalk in the microwave and millimeter wave range through the modulation of modal propagation [19]. Various defected microstrips, such as the T-defect microstrips, meandered microstrips, to mention a few, have also exhibited isotropic crosstalk reduction without packing trace density, although saturation in performance has been noted, as well as imbalances in NEXT, FEXT, particularly within the higher frequencies. Various comparisons also showcase the complexity in bandwidth, balance, and masking technique in crosstalk reduction [20-24].

In general, the existing solutions can be expected to account for either the near-end or the far-end crosstalk convincingly but certainly not the simultaneous effect on a broad frequency band. Most guard trace solutions involve a complex geometry such as a dense VIA fence or increased routing area; thus, their practicability in a small PCB is limited. These limitations motivate the development of a compact, pattern-based guard structure capable of enhancing capacitive coupling while reducing relative inductive coupling, thereby enabling balanced and broadband suppression of both NEXT and FEXT, as illustrated in Fig. 1.

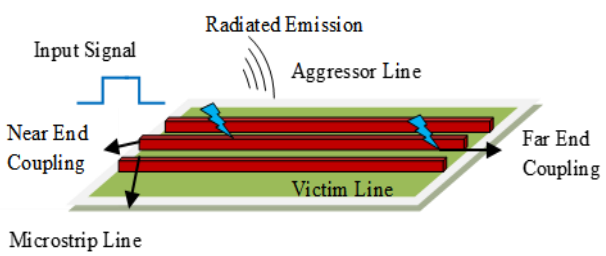

Fig. 1. Illustration of signal integrity degradation in high-speed PCB interconnects due to crosstalk.

In this work, a Greek key patterned defected microstrip guard trace is proposed to intentionally modify the electromagnetic coupling between adjacent microstrip lines. Unlike conventional guard traces or defected signal-line structures, the proposed design introduces patterned defects directly within the guard trace to reduce mutual inductive coupling while enhancing capacitive coupling between the signal lines. This approach enables balanced suppression of both near-end and far-end crosstalk without increasing the spacing between signal traces or introducing complex via fences. The proposed structure is analyzed using full-wave electromagnetic simulations, and its effectiveness is validated through parametric analysis, extraction of inductive–capacitive coupling parameters, and signal integrity evaluation, demonstrating significant broadband crosstalk reduction while preserving compact PCB routing. This work differs from prior defected structures by introducing patterning in the guard trace instead of the signal line, enabling simultaneous NEXT and FEXT suppression without affecting signal integrity

II. Crosstalk Analysis and Coupling Mechanisms in High-Speed PCB Interconnects

In modern combined electronic circuits, the unceasing striving for a higher bandwidth and a smaller size has resulted in reducing the distances between microstrip transmission lines. The result of holding the microstrips close to each other is that the electromagnetic fields of the fast transmission signals can easily induce in the nearby lines, thus causing a degradation of the signal quality due to parasitic couplings. Overall, the undesired effect of the parasitic couplings of the electromagnetic fields of the transmission signals, commonly known as crosstalk, increases when dealing with a dense PCB. In turn, crosstalk affects the signal quality due to the distortion of the signal timing, the reduction of the noise margin, as well as the appearance of misleading logic. Crosstalk arises from the mutual capacitance and mutual inductance.

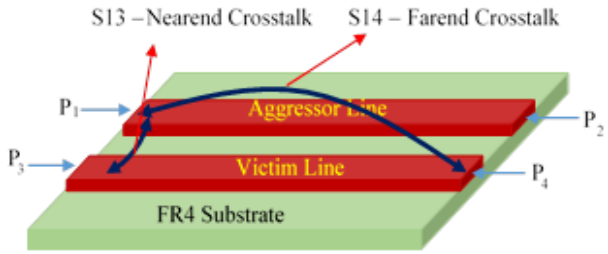

Fig. 2. Parallel microstrip lines illustrating near-end crosstalk (S_{13}) and far-end crosstalk (S_{14}).

Fig. 2 illustrates a typical parallel microstrip configuration used to explain the origin of near-end and far-end crosstalk. In closely spaced microstrip lines, one line acts as an aggressor carrying the high-speed signal and the adjacent line as a victim that suffers from interference due to electromagnetic coupling. Crosstalk appears at two observation points along the victim line: near the source of the aggressor line, called near-end crosstalk (NEXT), and near the load of the aggressor line, called far-end crosstalk (FEXT). While NEXT appears locally near the transmitter, FEXT accumulates along the coupling length and appears at the receiving end, where it may further deteriorate system performance by distorting the received signal and causing errors in interpretation.

From an electromagnetic standpoint, capacitive coupling is caused by the electric field between adjacent lines, while

inductive coupling arises from the magnetic field created by the current flowing through the aggressor line. In the end, the total crosstalk that may appear on the victim line is determined by the combination of these two mechanisms; both of its components increase with frequency and decrease with line spacing. Common remedies for crosstalk in high-speed PCBs are spacing, guard traces, and odd- and even-mode routing; all such methods may turn out to be poor performers in densely packed boards and usually don't offer broadband suppression. Full-wave electromagnetic simulation tools, such as Ansys HFSS, therefore play a critical role in accurately modeling these coupling mechanisms and evaluating advanced crosstalk-reduction structures for high-speed interconnect applications.

III. Proposed Greek Key Patterned Guard Trace: Methodology and Operating Principle

Effective crosstalk suppression in closely spaced microstrip lines requires increasing capacitive coupling while simultaneously reducing magnetic-field interaction responsible for far-end interference. Based on this principle, a Greek key patterned defected microstrip guard trace is introduced between two parallel microstrip lines to modify the electromagnetic coupling characteristics without increasing trace spacing. The proposed structure enhances mutual capacitance and alters the current return path along the coupling region, enabling simultaneous reduction of near-end and far-end crosstalk.

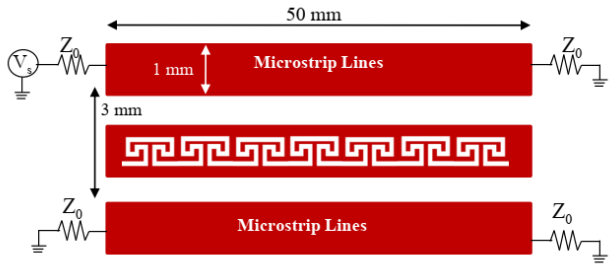

Fig. 3. Geometry of the proposed Greek key patterned defected microstrip guard trace inserted between parallel microstrip lines.

TABLE I
Geometrical Parameters of the Proposed Greek Key Patterned Guard Trace Structure

Parameter	Value
Microstrip width (W)	1mm
Guard trace width (Wg)	1mm
Spacing between lines	3 mm
Microstrip Length (L)	50 mm
Slot width	0.1–0.25 mm
Unit cell spacing	0.2–1 mm
Substrate width	1.6 mm
Substrate	FR4

The proposed Greek key patterned guard trace is shown in Fig. 3. The detailed geometrical parameters used in the simulation and fabrication are summarized in Table I. The slot width was selected between 0.1 mm and 0.25 mm, which is compatible with standard PCB fabrication processes. Typical commercial PCB manufacturing supports minimum feature sizes of approximately 0.1 mm, ensuring that the proposed structure can be practically implemented. The structure is implemented as a planar metallic resonator placed between the aggressor and victim lines, with a thickness equal to that of the signal traces to ensure field continuity and compatibility with standard PCB fabrication. The interlocking geometry increases the effective interaction area between the guard trace and the signal lines, leading to an increase in mutual capacitance while avoiding a proportional increase in mutual inductance.

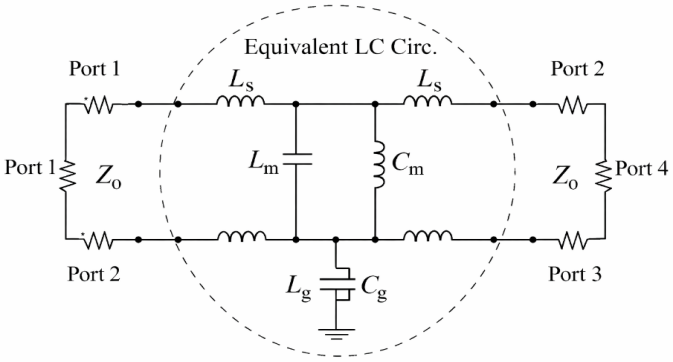

Fig. 4. Four-port lumped-element LC equivalent circuit model of the proposed Greek key patterned guard trace illustrating self and mutual inductive–capacitive coupling mechanisms.

The electromagnetic behavior of the proposed structure is explained using the four-port lumped-element LC equivalent circuit shown in Fig. 4. In this model, the series inductances represent the self-inductance of the microstrip lines, while the mutual inductance accounts for magnetic coupling between adjacent traces. The mutual capacitance models electric-field coupling between the lines, and the Greek key patterned guard trace is represented by a shunt resonant branch composed of an inductance and capacitance. This resonant branch modifies the local field distribution by enhancing capacitive interaction and disrupting magnetic-field continuity, thereby suppressing both near-end and far-end crosstalk.

The folded geometry of the Greek key pattern increases the effective current path length within the guard trace, redistributing return currents and reducing magnetic-field coupling responsible for far-end crosstalk. At the same time, the increased surface area strengthens electric-field confinement, improving capacitive balancing and mitigating near-end crosstalk. These combined effects enable broadband suppression of crosstalk without introducing narrowband resonance or additional layout complexity.

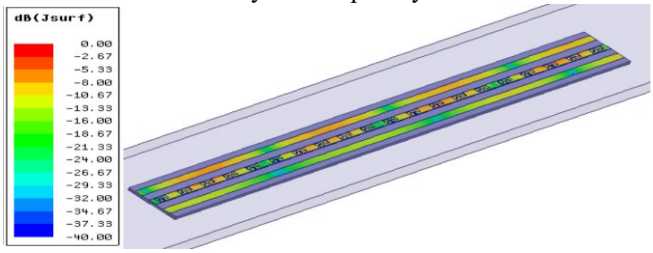

Fig. 5. Simulated surface current density (Jsurf) distribution of the proposed Greek key patterned guard trace at 10 GHz.

Fig. 5. illustrates the simulated surface current distribution of the proposed Greek key patterned guard trace at 10 GHz. Compared with a conventional straight guard trace, the folded geometry forces the induced currents to follow an extended and nonuniform path within the guard trace, effectively redistributing return currents away from the victim line. This current spreading weakens magnetic-field coupling between adjacent signal traces while enhancing electric-field confinement, thereby reducing far-end crosstalk and improving capacitive balance. The observed current behavior provides direct physical insight into the electromagnetic mechanism responsible for the simultaneous suppression of near-end and far-end crosstalk.

To achieve uniform performance over the entire coupling length, multiple Greek key unit cells are periodically inserted between the microstrip lines. This periodic arrangement introduces distributed resonant discontinuities that modify even- and odd-mode propagation characteristics along the transmission path, limiting the accumulation of far-end interference while maintaining consistent isolation across the operating frequency range.

The proposed Greek key patterned defected microstrip guard trace provides a compact and fabrication-friendly solution for crosstalk mitigation. By enhancing mutual capacitance and reducing relative magnetic coupling through controlled resonant behavior, the structure achieves effective and broadband suppression of both NEXT and FEXT, making it suitable for high-speed and high-density PCB interconnect applications.

Unlike conventional straight or via-stitched guard traces that primarily provide electrostatic shielding, the proposed Greek key patterned defected microstrip guard trace intentionally reshapes both capacitive and inductive coupling paths. The interlocking geometry simultaneously enhances mutual capacitance and disrupts magnetic-field continuity along the coupling length, enabling balanced and broadband suppression of both near-end and far-end crosstalk without increasing routing area or fabrication complexity.

IV. Results and Discussion

The proposed Greek key patterned guard trace was analyzed using full-wave electromagnetic simulations in ANSYS HFSS over the 0.01–10 GHz frequency range. The three-dimensional simulation model used in this study is shown in Fig. 6. The structure consists of two parallel microstrip lines of length 50 mm and width 1 mm, separated by a spacing of 3 mm and implemented on an FR4 substrate with relative permittivity ε_r = 4.6 and thickness 1.6 mm. A guard trace of identical width is positioned between the signal lines, into which periodic Greek key patterned DMS unit cells are embedded. Parametric variations of the unit-cell spacing (**D**) and defect width (**W**) were carried out to evaluate their influence on electromagnetic coupling. Near-end and far-end crosstalk were quantified using the scattering parameters S_{13} and S_{14}, respectively.

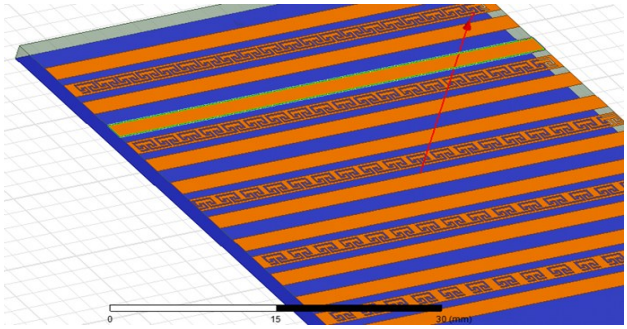

Fig. 6. Three-dimensional HFSS simulation model of the proposed Greek key patterned DMS guard trace embedded between parallel microstrip lines.

A. Frequency-Domain Crosstalk Analysis Using S-Parameters

The coupled microstrip structures with and without the proposed Greek key patterned DMS guard trace were evaluated using full-wave electromagnetic simulations in ANSYS HFSS over the 0.01–10 GHz frequency range.

The baseline configuration consisted of two parallel microstrip lines of length 50 mm and width 1 mm, separated by a spacing of 3 mm and implemented on an FR4 substrate with relative permittivity ε_r = 4.6 and thickness 1.6 mm.

The guard-trace width was maintained at 1 mm. Parametric sweeps of the defect width (**W**) and unit-cell spacing (**D**) were performed to examine their influence on near-end and far-end crosstalk.

Figs. 7 through 14 illustrate the simulated NEXT (S_{13}) and FEXT (S_{14}) responses for various combinations of defect width and unit-cell spacing. For a defect width of W = 0.1 mm, Figs. 7 and 8 indicate that increasing the spacing D leads to a significant enhancement in both NEXT and FEXT suppression, with optimal performance achieved at D = 1.0 mm. Similar trends are observed for defect widths of 0.15 mm, 0.2 mm, and 0.25 mm, as shown in Figs. 7 through 14.

However, as the defect width increases, the improvement gradually saturates and slightly degrades, suggesting that excessive widening of the patterned structure no longer contributes effectively to coupling mitigation and may disturb the intended capacitive–inductive balance.

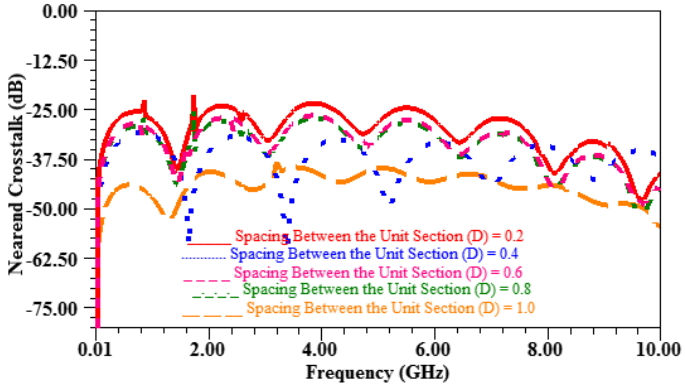

Fig. 7. NEXT (S_{13}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.1 mm.

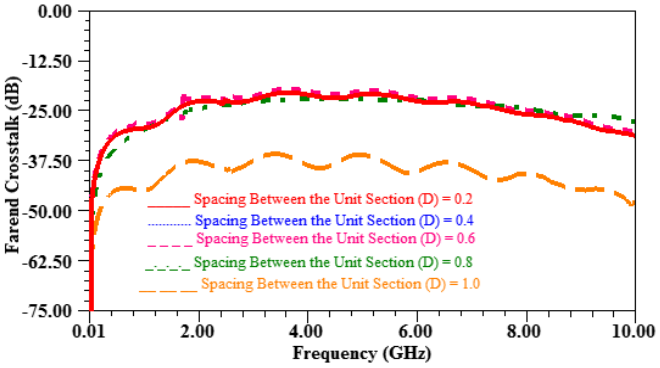

Fig. 8. FEXT (S_{14}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.1 mm.

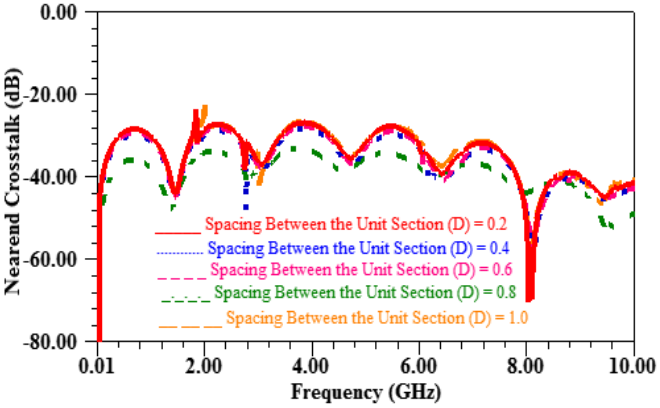

Fig. 9. NEXT (S_{13}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.15 mm.

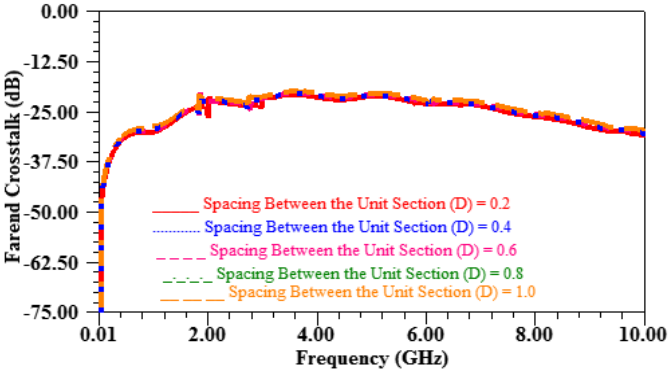

Fig. 10. FEXT (S_{14}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.15 mm.

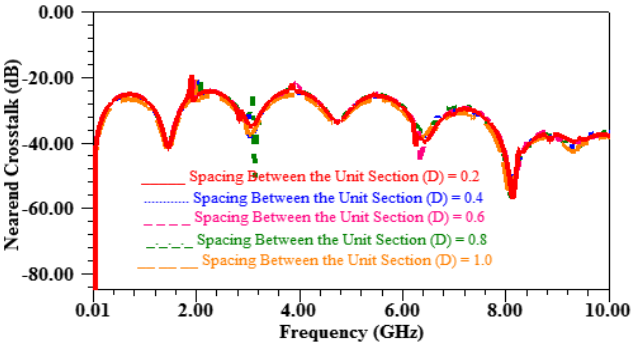

Fig. 11. NEXT (S_{13}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.2 mm.

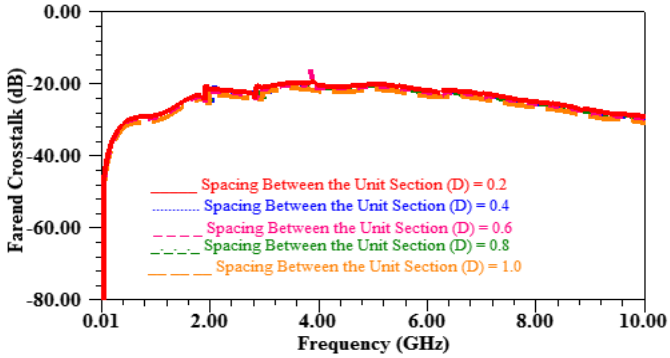

Fig. 12. FEXT (S_{14}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.2 mm.

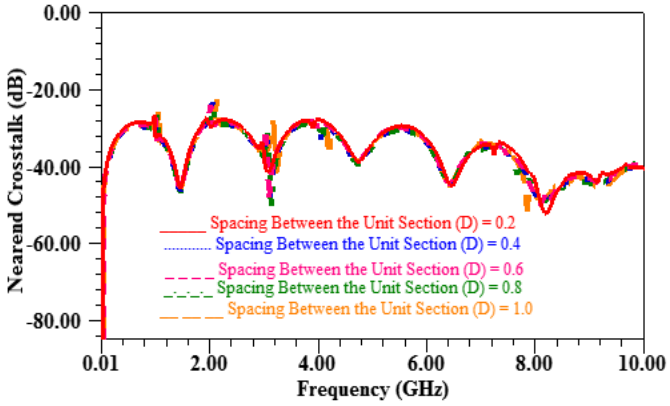

Fig. 13. NEXT (S_{13}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.25 mm.

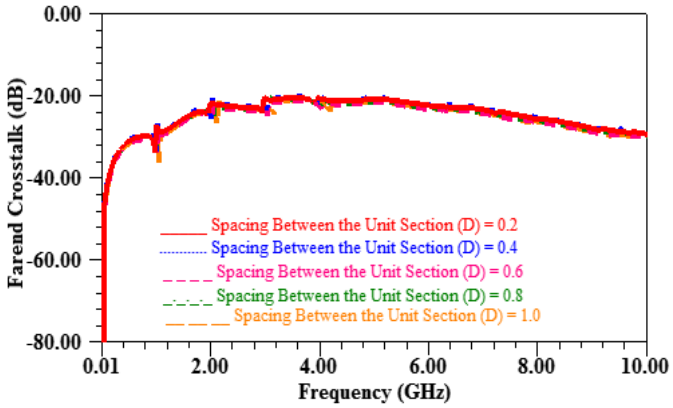

Fig. 14. FEXT (S_{14}) versus frequency for the proposed Greek key patterned DMS guard trace with different unit-cell spacing (D) at W = 0.25 mm.

The quantitative results of the parametric study are summarized in Table II. The strongest crosstalk suppression is obtained for W = 0.1 mm and D = 1.0 mm, where the proposed structure achieves NEXT of -54.40 dB and FEXT of -48.23 dB at 10 GHz. This represents the best isolation observed across all configurations. For larger defect widths, although moderate suppression is maintained, the NEXT and FEXT levels remain relatively constant with spacing, confirming the presence of a saturation effect in the capacitive–inductive modification mechanism.

TABLE II
NEXT AND FEXT PERFORMANCE OF THE PROPOSED GREEK KEY PATTERNED DMS GUARD TRACE FOR VARIOUS DEFECT WIDTHS AND UNIT-CELL SPACING

Width of DMS in mm	Spacing Between the Unit Cell in mm	NEXT (S_{13}) in dB	FEXT (S_{14}) in dB
W=0.1	0.2	-40.94	-31.19
	0.4	-36.88	-30.45
	0.6	-45.88	-27.84
	0.8	-44.68	-29.58
	1.0	-54.40	-48.23
W=0.15	0.2	-41.54	-31.07
	0.4	-43.35	-30.67
	0.6	-42.96	-30.46
	0.8	-48.86	-30.98
	1.0	-40.71	-29.83
W=0.2	0.2	-37.89	-29.28
	0.4	-36.98	-29.82
	0.6	-37.73	-29.85
	0.8	-37.16	-29.64
	1.0	-39.06	-30.86
W=0.25	0.2	-40.65	-29.50
	0.4	-40.72	-29.48
	0.6	-39.99	-30.40
	0.8	-40.27	-29.86
	1.0	-40.42	-30.23

This comparison confirms that the improvement is primarily due to the Greek key patterned defect rather than the presence of the guard trace alone. Compared with unguarded parallel microstrip lines (NEXT: −14.45 dB and FEXT: −10.83 dB), the optimized Greek key patterned guard trace significantly improves crosstalk suppression, achieving −54.4 dB NEXT and −48.23 dB FEXT at 10 GHz. The proposed design demonstrates superior broadband performance, highlighting its effectiveness in reshaping even- and odd-mode propagation characteristics.

To further emphasize the advantage of the proposed approach, Figs. 15 and 16 compare the NEXT and FEXT responses of the Greek key patterned guard trace with no guard trace and a conventional straight guard trace for identical spacing (S = 3 mm) and trace widths (W = W_g = 1 mm). The proposed structure consistently exhibits lower crosstalk levels across the entire frequency band, confirming its enhanced ability to suppress both near-end and far-end interference without increasing routing area.

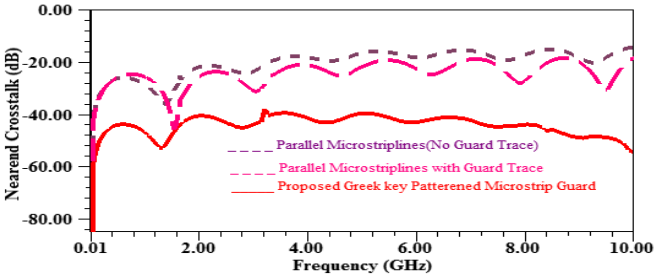

Fig. 15. NEXT (S13) comparison between the proposed Greek key patterned guard trace, No Guard Trace and a conventional guard trace for S = 3 mm and W = W_g = 1 mm.

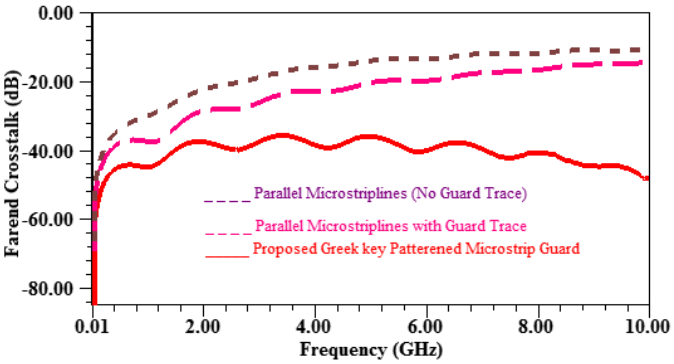

Fig. 16. FEXT (S14) comparison between the proposed Greek key patterned guard trace and a conventional straight guard trace for S = 3 mm and W = W_g = 1 mm.

B. Inductive and Capacitive Coupling Analysis

To further investigate the electromagnetic mechanisms responsible for the observed crosstalk suppression, the per-unit-length inductive and capacitive parameters were extracted from full-wave electromagnetic simulations for both conventional parallel microstrip lines and the proposed Greek key patterned guard trace. The extracted parameters include the self-inductance L_s, mutual inductance L_m, total capacitance C_T, and mutual capacitance C_m, which collectively determine near-end and far-end coupling behavior. These values provide quantitative insight into the modification of electric- and magnetic-field interactions introduced by the proposed structure and are summarized in Table III.

TABLE III
EXTRACTED INDUCTIVE AND CAPACITIVE PARAMETERS FOR CONVENTIONAL AND PROPOSED GUARD STRUCTURES

Parameter	Parallel Microstrip Lines (No Guard)	Greek Key Patterned Guard Trace
L_s (nH/m)	370	595
L_m (nH/m)	8.18	6.12
C_T (pF/m)	132	201
C_m (pF/m)	0.91	2.31
L_m / L_s	0.022	0.010
C_m / C_T	0.0069	0.0115
$C_m/C_T - L_m/L_s$	−0.0152	0.0012
$C_m/C_T + L_m/L_s$	0.0290	0.0218

For the parallel microstrip lines without a guard, the self-inductance L_s is 370 nH/m and the mutual inductance L_m is 8.18 nH/m. When the Greek key patterned guard trace is introduced, Ls increases significantly to 595 nH/m due to the elongated and folded current path created by the interlocking geometry. At the same time, the mutual inductance L_m is reduced to 6.12 nH/m, indicating effective disruption of magnetic-field coupling between the aggressor and victim lines. This reduction in relative magnetic coupling directly contributes to far-end crosstalk suppression.

A similar improvement is observed in the capacitive

parameters. The total capacitance C_T increases from 132 pF/m for the unguarded structure to 201 pF/m for the proposed configuration, reflecting the increased electric-field interaction introduced by the patterned guard. More importantly, the mutual capacitance C_m nearly doubles, increasing from 0.91 pF/m to 2.31 pF/m. The enhanced mutual capacitance improves electric-field balancing between adjacent lines, which is essential for reducing near-end crosstalk.

To evaluate coupling balance, normalized ratios were analyzed. The ratio L_m/L_s decreases from 0.022 to 0.010, confirming a substantial reduction in relative inductive coupling. Conversely, the ratio C_m/C_T increases from 0.0069 to 0.0115, indicating stronger capacitive interaction relative to the total capacitance.

The difference term ($C_m/C_T - L_m/L_s$), which is closely associated with far-end crosstalk generation, shifts from −0.0152 in the conventional structure to 0.0012 in the proposed design, demonstrating improved balance between inductive and capacitive coupling. Similarly, the summation term ($C_m/C_T + L_m/L_s$), related to near-end crosstalk behavior, decreases from 0.0290 to 0.0218, confirming effective NEXT suppression.

These extracted inductive and capacitive parameters clearly explain the superior frequency- and time-domain performance of the Greek key patterned guard trace. By increasing self-inductance, enhancing mutual capacitance, and reducing relative mutual inductance, the proposed structure achieves a balanced modification of the electromagnetic coupling mechanisms. This balance is consistent with the significant reductions in NEXT and FEXT observed in the S-parameter and eye-diagram analyses, validating the effectiveness of the Greek key patterned guard trace for high-speed, high-density PCB interconnects.

C. Time-Domain Signal Integrity and BER Analysis

Time-domain analysis was conducted to assess signal integrity and transmission reliability and to validate the effectiveness of the proposed Greek key patterned guard trace under high-speed operation. Eye diagrams and bit error rate (BER) performance were obtained using S-parameters exported from ANSYS HFSS with a 10-Gb/s NRZ PRBS7 data stream applied to the aggressor line. The victim-line voltage response was reconstructed via time-domain convolution, enabling direct comparison between the conventional parallel microstrip configuration and the proposed structure. The resulting eye diagrams and BER results are shown in Figs. 17–19.

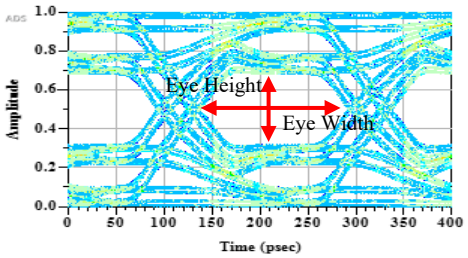

Fig. 17. Eye diagram of the conventional parallel microstrip interconnect at 10-Gb/s data rate.

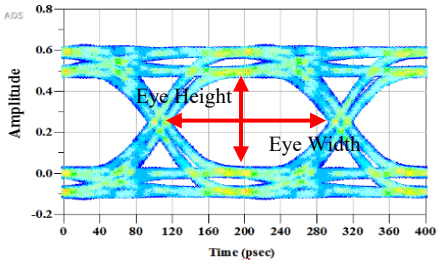

Fig. 18. Eye diagram of the parallel microstrip with conventional guard interconnect at 10-Gb/s data rate.

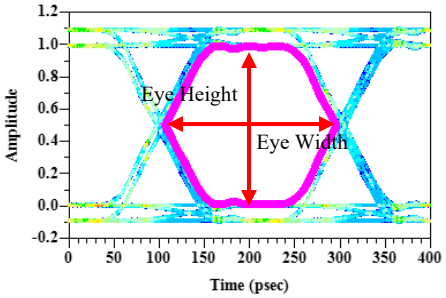

Fig. 19. Eye diagram of the proposed Greek key patterned guard trace at 10-Gb/s data rate.

The eye diagram corresponding to the conventional parallel microstrip lines, shown in Fig. 17, exhibits severe degradation, characterized by pronounced eye closure, reduced vertical opening, and significant timing jitter. The extracted eye height is approximately 0.32 V, with an eye width of about 0.42 unit intervals (UI).

In addition, the RMS jitter is approximately 18.6 ps, indicating substantial timing uncertainty caused by strong near-end and far-end crosstalk as well as inter-symbol interference. This degraded eye opening results in unstable sampling instants at the receiver and yields a BER on the order of 10^{-6}, indicating unreliable data transmission under high-speed conditions. The eye diagram for the conventional guard trace configuration, shown in Fig. 18, demonstrates moderate improvement in signal integrity. The extracted eye height is approximately 0.48V, and the eye width is about 0.55 UI**,** indicating partial recovery of noise margin and timing margin. However, residual eye closure is still present due to incomplete suppression of coupling effects.

In contrast, the eye diagram obtained for the proposed Greek key patterned guard trace, shown in Fig. 19, demonstrates a marked improvement in signal integrity. The eye height increases to approximately 0.78 V, representing an improvement of nearly 144% compared to the conventional structure, while the eye width expands to about 0.68 UI. The RMS jitter is significantly reduced to approximately 6.9 ps, confirming improved timing stability and reduced inter-symbol interference. As a direct consequence of the widened eye opening and reduced jitter, the BER performance is significantly improved and is suppressed to below 10^{-12}, indicating error-free operation within the simulated observation window.

The strong correlation between eye-diagram quality and BER performance highlights the effectiveness of the proposed

Greek key patterned guard trace in mitigating crosstalk-induced impairments. By improving the balance between capacitive and inductive coupling, the proposed structure reduces noise injection and limits far-end interference accumulation, thereby stabilizing both signal amplitude and timing at the receiver. These results confirm that the proposed design not only enhances frequency-domain isolation but also translates these improvements into reliable time-domain performance, making it well suited for multi-gigabit high-speed PCB interconnect applications.

D. Experimental Validation

Experimental evaluation was carried out to validate the crosstalk suppression capability of the proposed Greek key patterned guard trace under practical conditions. Near-end crosstalk (NEXT) and far-end crosstalk (FEXT) were measured over the 0.01–10 GHz frequency range and compared with conventional parallel microstrip lines employing a straight guard trace.

The fabricated test structures corresponding to the three configurations are shown in Fig. 20. To ensure a fair comparison, identical substrate properties, trace dimensions, and inter-trace spacing were maintained for all measurements.

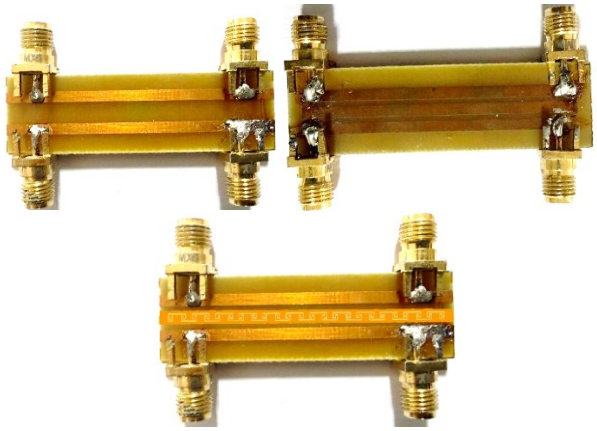

Fig. 20. Fabricated conventional parallel microstrip line, parallel microstrip with conventional guard and proposed Greek key patterned guard trace structure.

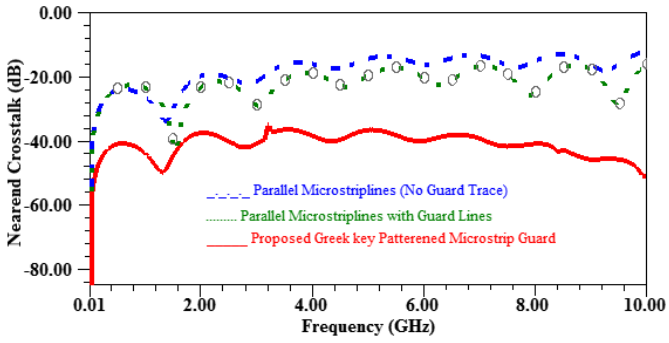

Fig. 21. Measured near-end crosstalk (NEXT) comparison between the conventional guard trace and the proposed Greek key patterned guard trace.

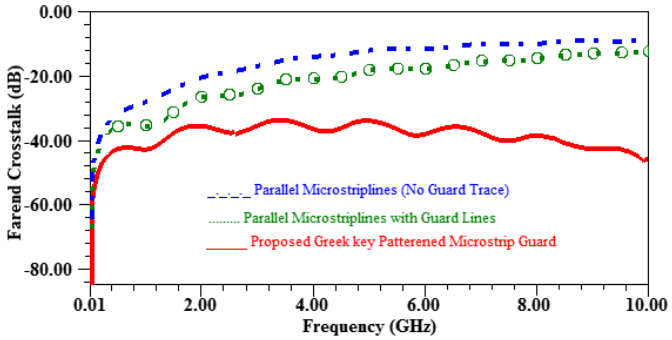

Fig. 22. Measured far-end crosstalk (FEXT) comparison between the conventional guard trace and the proposed Greek key patterned guard trace.

Fig. 21 presents the measured near-end crosstalk (NEXT) performance for the three configurations: parallel microstrip lines without a guard trace, a conventional straight guard trace, and the proposed Greek key patterned guard trace. The unguarded structure exhibits relatively high crosstalk levels, with NEXT around −12.32 dB. The introduction of a conventional straight guard trace provides only a modest improvement, reducing NEXT to approximately −16.25 dB. In contrast, the proposed Greek key patterned guard trace achieves a significant reduction in near-end crosstalk, with measured NEXT reaching −51.39 dB. This substantial improvement confirms that the patterned guard structure effectively enhances capacitive coupling balance and suppresses near-end noise coupling between adjacent traces.

The measured far-end crosstalk (FEXT) performance is shown in Fig. 22. For the unguarded configuration, FEXT is measured at approximately −8.98 dB, indicating strong coupling between adjacent lines. The conventional straight guard trace improves the isolation slightly, reducing FEXT to around −12.60 dB. However, the proposed Greek key patterned guard trace significantly suppresses far-end crosstalk, achieving −46.26 dB. This reduction demonstrates that the proposed structure effectively mitigates inductive coupling along the transmission path.

Quantitatively, the measured results are in good agreement with the simulation-based S-parameter analysis and the extracted inductive–capacitive coupling parameters. At 10 GHz, the proposed Greek key patterned guard trace improves NEXT from −16.25 dB to −51.39 dB and FEXT from −12.60 dB to −46.26 dB compared with the conventional straight guard trace. Across the measured frequency range, the proposed structure consistently maintains significantly lower crosstalk levels, demonstrating robust broadband performance under practical conditions.

The agreement between experimental and simulated results confirms the effectiveness and practical feasibility of the proposed structure for high-speed, high-density PCB interconnects. Furthermore, the measured results indicate that the proposed design maintains stable performance despite minor fabrication tolerances, highlighting its robustness for real-world implementation.

In addition to crosstalk reduction, the impact of the proposed structure on signal integrity was evaluated. Compared with the conventional straight guard trace, the proposed Greek key patterned guard trace improves the insertion loss (S21) from −3.63 dB to −1.36 dB, corresponding to an improvement of approximately 2.27 dB across the operating band, indicating reduced signal attenuation. This improvement is attributed to better field confinement and optimized current distribution introduced by the patterned geometry. Furthermore, improved return loss (S11) is observed, indicating enhanced impedance matching and reduced reflections across the measured frequency range.

As a result, the proposed guard trace not only suppresses near-end and far-end crosstalk but also enhances overall signal transmission quality. The combined improvement in insertion loss, return loss, and frequency-domain isolation is consistent with the observed time-domain signal integrity enhancement, including wider eye openings, reduced timing jitter, and error-free operation with BER below 10^{-12}. The strong agreement between experimental and simulated results confirms the robustness and practical feasibility of the proposed Greek key patterned guard trace for high-speed, high-density PCB interconnect applications.

Table IV compares reported crosstalk reduction techniques and highlights the superior performance of the proposed Greek key patterned defected microstrip guard trace. Conventional approaches such as stepped impedance, serpentine lines, and stub- or miter-based guard traces typically achieve NEXT and FEXT suppression between -25 dB and -35 dB up to 10 GHz, while some defected and meandered structures offer limited or unbalanced improvement. In contrast, the proposed design achieves the strongest overall isolation, with NEXT of -54.40 dB and FEXT of -48.23 dB at 10 GHz.

This improvement results from the Greek key geometry simultaneously enhancing mutual capacitance and reducing relative mutual inductance, enabling balanced and broadband crosstalk suppression in a compact, fabrication-compatible structure suitable for high-speed PCB interconnects.

From a practical standpoint, the proposed Greek key patterned guard trace provides a favorable balance between performance, layout complexity, and fabrication cost. Unlike via-stitched guard traces, it is fully planar and implemented on a single copper layer using standard PCB etching, resulting in manufacturing effort comparable to that of a conventional straight guard trace. The compact geometry avoids excessive layout complexity while delivering substantially improved crosstalk suppression. Moreover, because the mitigation mechanism is based on broadband modification of capacitive and inductive coupling rather than narrowband resonance, the proposed approach is well suited for higher data-rate applications. Although demonstrated for single-layer microstrip interconnects, the underlying principle can be extended to multilayer PCB structures, such as stripline or embedded microstrip configurations, through appropriate adaptation of the guard geometry and reference planes.

TABLE IV
COMPARISON OF REPORTED CROSSTALK REDUCTION TECHNIQUES AND THE PROPOSED GREEK KEY PATTERNED GUARD TRACE

Ref	Work	Frequency (GHz)	S_{13} (dB)	S_{14} (dB)
[1]	Cross-shape resonators Structure	10	-40.36	- 13.16
[2]	TL-shaped defected microstrip structures	8	-33.25	-25.51
[3]	PLTL with discontinuous structured guard lines	20	-35.76	-39.81
[4]*	Spiral resonator DMS	10	-41.25	-34.49
[5]*	Defected Microstripline Structure	8	-9.42	-33.08
[6]*	Meander Defected Microstripline	12	-26.04	-14.82
[7]*	Mitered Guard Trace	10	-33.16	-32.23
This work	**Greek Key Patterned Defective Microstrip Guard Trace (W=0.1, D=1.0)**	**10**	**-54.40**	**-48.23**

*Authors previous Work

V. CONCLUSION

This research presents a Greek key patterned defected microstrip guard trace for suppressing near-end and far-end crosstalk in high-speed microstrip interconnects through intentional modification of capacitive and inductive coupling mechanisms. The folded geometry increases the effective interaction area and extends the current path within the guard trace, enhancing mutual capacitance while disrupting magnetic-field coupling without increasing line spacing. Parametric analysis identified an optimal defect width of 0.1 mm and unit-cell spacing of 1.0 mm, beyond which performance saturation occurs. Under these conditions, the proposed structure reducing NEXT by approximately 35 dB and FEXT by approximately 32 dB compared with conventional parallel microstrip lines with straight guard traces. Inductive–capacitive analysis quantitatively confirmed the underlying mechanism, showing an increase in self-inductance from 370 nH/m to 595 nH/m, an enhancement of mutual capacitance from 0.91 pF/m to 2.31 pF/m, and a reduction in relative mutual inductance, leading to improved coupling balance. Time-domain analysis further demonstrated enhanced signal integrity, with increased eye

height and eye width, reduced RMS jitter, and error-free operation with BER below 10^{-12}. Experimental measurements closely followed the simulated trends, confirming the robustness and practical feasibility of the proposed approach. Overall, the proposed guard trace provides a compact and fabrication-friendly solution for mitigating crosstalk in dense, high-speed PCB interconnects.

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