A High step-up Single Switch based Cubic gain DC-DC converter for PV Applications

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***Abstract*—The growing use of renewable energy sources (RES's), particularly photovoltaic(PV) systems, has increased the need for efficient high step-up DC–DC converters. This paper proposes a single switch cubic-gain (SSCG) converter capable of achieving a high voltage gain with minimal circuit complexity. The proposed converter achieves cubic voltage gain through the integration of a quadratic boost converter(QBC) combined with a voltage-lift technique, enabling substantial voltage boosting using only a single switch. Detailed steady-state analysis are carried out under both continuous and discontinuous conduction modes, along with an evaluation of the influence of non-ideal components on practical voltage gain and efficiency. The comparison results with the existing converter topologies highlight the distinctive advantages of the SSCG converter, including the simple structure, minimum total component count, continuous input current, common ground configuration, and high step-up capability. A 48/400 V, 50 kHz, 200 W hardware prototype is developed and experimentally verified, demonstrating close agreement with theoretical analysis. The results confirm that the proposed SSCG converter is a promising solution for high-gain photovoltaic energy conversion applications.**

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***Index Terms*—Common ground configuration, Cubic voltage gain, high step-up topology, PV applications, voltage-lift technique, Single-switch DC-DC converter**

I. Introduction

THE increasing global emphasis on clean and sustainable energy has driven a major transition from conventional fossil fuels to renewable energy systems. The 2030 agenda of the Economic Commission of the United Nations for Latin America and the Caribbean (ECLAC) underscores that clean energy technologies are crucial to achieve long-term environmental and economic sustainability [1]–[2]. Among the various renewable energy options, solar PV systems have attracted significant attention due to their modular structure, scalability, and eco-friendly characteristics. However, the output voltage of PV panels is typically low and fluctuates with variations in solar irradiance and temperature. Therefore, an efficient DC–DC converter is required to boost and regulate the PV voltage for integration with DC microgrids, electric vehicle (EV) chargers and inverter-fed renewable energy systems [3]–[4]. DC–DC converters play a key role in maintaining voltage stability and ensuring compatibility between different stages of power conversion. These converters are generally categorized into isolated and non-isolated types. Isolated converters can provide high voltage gain by adjusting the turns of the transformer, but suffer from leakage inductance, voltage stress on switches, electromagnetic interference (EMI) and reduced power density [5]. Furthermore, the use of transformers increases system complexity, cost, and size, making isolated topologies less suitable for compact RES. Conversely, non-isolated converters eliminate the transformer, resulting in a lighter, low-cost, and more efficient design ideal for medium-power PV and battery applications where electrical isolation is not required. The conventional boost converter offers a simple structure and a voltage gain of $\frac{1}{(1-D)}$; however, a high voltage gain demands large duty ratios, leading to increased conduction losses, device stress, and reduced efficiency [6].

To overcome these limitations, researchers have developed numerous high-gain non-isolated converters that can be broadly classified into coupled and noncoupled inductor-based topologies. Coupled inductor converters can achieve high voltage gain, but produce voltage spikes due to leakage inductance, requiring additional clamping or snubber circuits [7]. These auxiliary networks not only increase cost and component count but also reduce overall efficiency. On the other hand, Non-coupled inductor converters avoid such complications and provide a simple, cost-effective, and efficient alternative for RE systems. Various gain extension techniques have been introduced to improve the voltage conversion ratio, including switched inductor (SI) [8]–[11], voltage multiplier cell (VMC) [12], diode–capacitor networks [13]–[14], switched capacitor (SC) [15], and hybrid switched inductor (HSL) topologies [16]. Although these topologies achieve better gain, they often experience high current stress, increased number of components, and common-ground issues. Quadratic and cubic converters have recently gained popularity for their ability to achieve higher voltage gains with moderate duty ratios [17]–[25]. However, many reported designs still suffer from large component counts, higher order due to multiple passive elements and non-common-ground structures [26]–[29], [31]. gain enhancement through multi level (or) cascaded voltage-lift stages, which increases inductor current circulation and that rely on multiple energy processing stages, which complicate PV integration and sensing [30], [32].

To address these challenges, this paper proposes a SSCG DC–DC converter suitable for PV and battery-powered appli-

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cations. The proposed topology is derived from a quadratic boost converter (QBC) combined with a voltage-lift technique as illustrated in Fig. 1. The primary contribution of this work is the realization of a high voltage gain i.e. $\frac{1}{(1-D)^3}$ using a single switch without the need for transformers, coupled inductors, or multi-stage cascaded structures. Due to its cubic gain characteristic, the proposed converter achieves a high voltage gain at moderate duty ratios, which helps switching losses and overall control complexity. In addition, SSCG converter maintains a continuous input current thereby minimizing input current ripple at the source side, common ground structure, improving overall efficiency, compactness, and easy-to-implement for next-generation PV-based DC energy systems.

The remaining sections of this paper are organized as follows. Section II presents the conceptual design and operating modes of the proposed converter under Continuous conduction mode (CCM) and Discontinuous conduction mode (DCM). Section III provides a detailed analysis of the voltage gain characteristics in CCM, DCM, and Boundary Conduction Mode (BCM), along with parameter design, evaluation of voltage and current stresses on switches and diodes, efficiency estimation considering component nonidealities, and Power loss assessment. Section IV focuses on the dynamic modeling and a Small-signal analysis of the proposed converter. Section V discusses the performance evaluation of the SSCG converter through experimental validation. Finally, Section VI concludes the paper by summarizing the key findings.

II. Conceptual Design of the Proposed Converter

The SSCG converter is composed of a single switch, five diodes, and three pairs of inductors and capacitors, forming a compact non-isolated structure as shown in Fig. 1. The proposed converter is designed to operate in CCM during steady state. It operates in two modes as shown in Fig. 2, based on the inductor and capacitor charging-discharging cycles.

A. Operation of CCM:

The CCM consists of two distinct intervals: Mode-1 corresponding to the switch ON state and Mode-2 associated with the switch OFF state as shown in Fig. 2. The switching intervals $(t_0 - t_2)$ define these modes, which are indicated by the key waveforms illustrated in Fig. 3(a).

Mode-I ***(t_0–t_1):***

During this interval, the switch (S) remains in the ON state. Consequently, diodes $(d_1, d_3$ and $d_0)$ are reverse-biased whereas diodes $(d_2$ and $d_4)$ conduct. In this mode, the input source voltage (V_{in}) energizes inductor L_1. Simultaneously, capacitors $(C_1$ and $C_2)$ transfer energy to inductors L_2 and L_3 respectively. while, capacitor (C_0) continues to supply power to the load. Applying Kirchhoff's voltage law (KVL) and Kirchhoff's Current Law (KCL), the corresponding mathematical equations are derived.

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C1} \\ V_{L3} = V_{C1} + V_{C2} \end{cases} \tag{1}$$

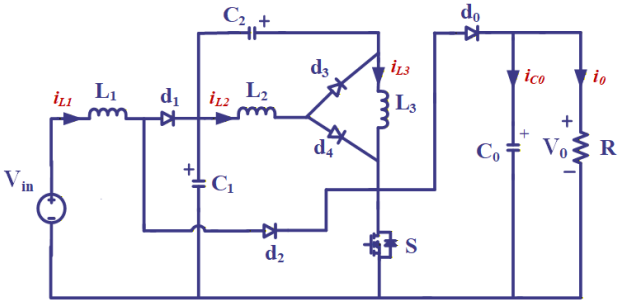


Fig. 1. Proposed SSCG converter.

$$\begin{cases} i_{c1} = C_1\left(\frac{dv_{c1}}{dt}\right) = -i_{L2} - i_{L3} \\ i_{c2} = C_2\left(\frac{dv_{c2}}{dt}\right) = -i_{L3} \\ i_{c0} = C_0\left(\frac{dv_{c0}}{dt}\right) = -i_0 \end{cases} \tag{2}$$

Mode-II ***(t_1–t_2):***

Throughout this interval, the switch (S) is turned OFF. Consequently, diodes $(d_1, d_3$ and $d_0)$ are forward-biased while diodes $(d_2$ and $d_4)$ remain non-conducting. In this mode, the inductor (L_1) releases its stored energy by charging the capacitor (C_1). Similarly, the demagnetization of inductors $(L_2$ and $L_3)$ transfers energy to the capacitors C_2 and C_0, with C_0 continues to supply the load. The corresponding equations are formulated by applying KVL and KCL as given below.

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_{L2} = -V_{C2} \\ V_{L3} = V_{C1} + V_{C2} - V_0 \end{cases} \tag{3}$$

$$\begin{cases} i_{c1} = C_1\left(\frac{dv_{c1}}{dt}\right) = i_{L1} - i_{L3} \\ i_{c2} = C_2\left(\frac{dv_{c2}}{dt}\right) = i_{L2} - i_{L3} \\ i_{c0} = C_0\left(\frac{dv_{c0}}{dt}\right) = i_{L3} - i_0 \end{cases} \tag{4}$$

B. Operation of DCM:

Figure. 3(b). shows the theoretical waveforms and operating modes of the proposed SSCG converter in DCM.

The operation of mode-I and mode-II is closely resembles that in CCM and the equivalent circuit is depicted in Figs. 2(a) and 2(b). D_x is the duty ratio of DCM mode that can be calculated by solving equations (5) and (6) as shown in Fig. 3(b). The maximum inductor current of L_3 in mode-I and mode-II is given by:

$$[(i_{L3})_p]^1 = \frac{(V_{C1} + V_{C2})\, D}{L_3 f_s} \tag{5}$$

$$[(i_{L3})_p]^{II} = \frac{(V_{C1} + V_{C2} - V_0)\, D_x}{L_3 f_s} \tag{6}$$

$$D_x = \frac{D}{1 - \left(\frac{V_0}{V_{in}}\right)(1-D)^2} \tag{7}$$

Mode-III $(t_2 - t_3)$*:*

During this mode, all the devices are OFF, and the current flows through the storage elements is zero As shown in Fig.

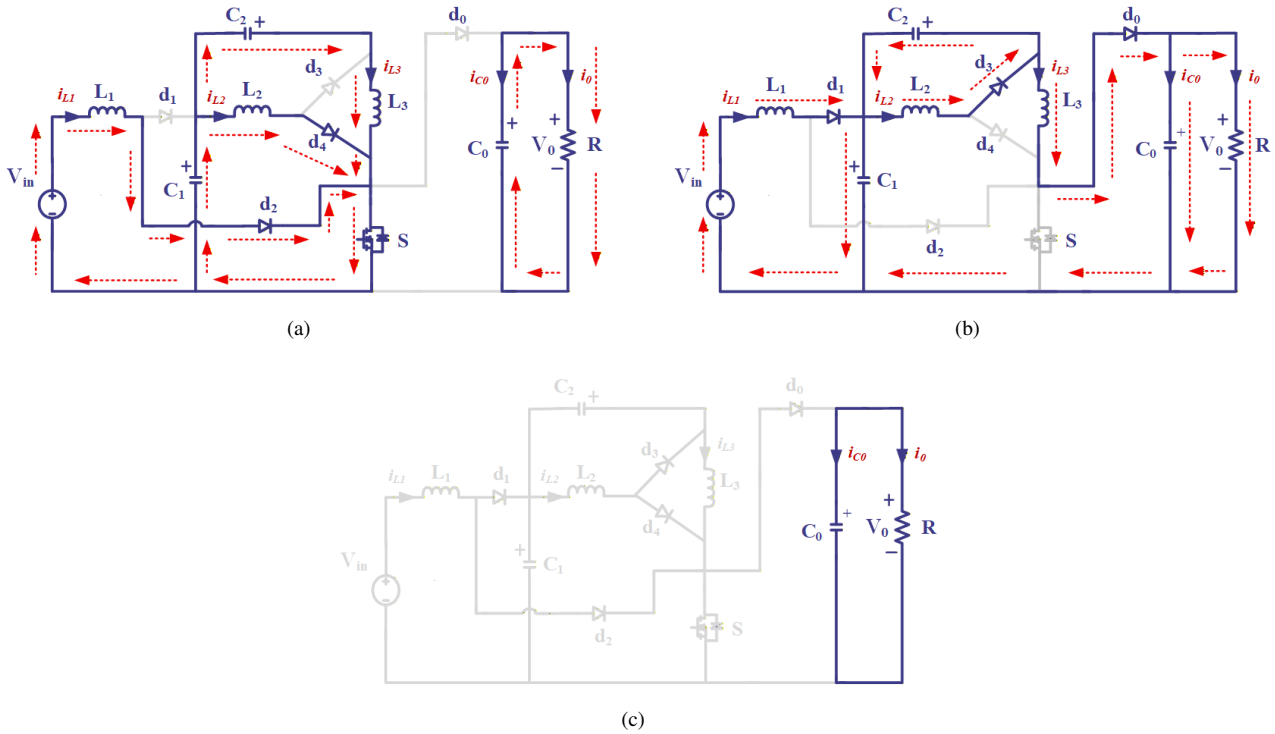


Fig. 2. (a) Operating mode-I (b) Operating mode-II (c) Operating mode-III of Proposed SSCG converter.

2(c). the output capacitor (C_0) provides current through the load side.

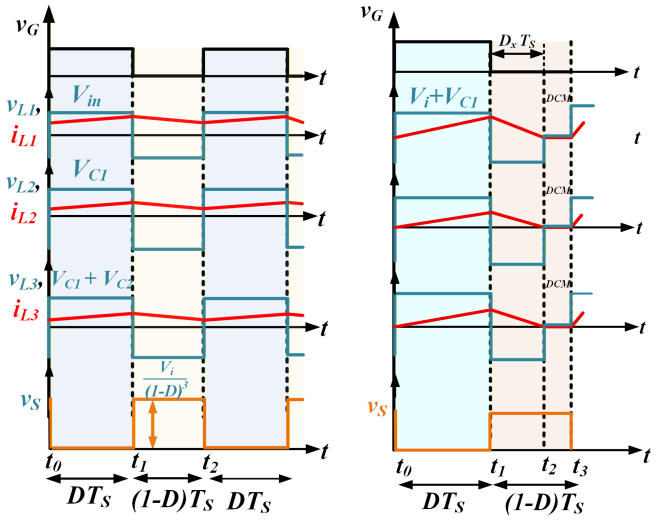


Fig. 3. Typical operating waveforms of the proposed SSCG converter (a) CCM (b) DCM.

III. Steady-State Analysis Of Proposed Converter

A. Voltage Gain in CCM:

In CCM, the voltage gain of the SSCG converter is formulated by applying the volt–sec balance principle to the inductor voltage expressions in (1) and (3) resulting in the gain expression shown in (8), $'D'$ is the Duty ratio of CCM mode.

$$G_{CCM} = \frac{V_0}{V_i} = \frac{1}{(1-D)^3} \tag{8}$$

$$V_{C1} = \frac{V_{in}}{(1-D)}\,;\; V_{C2} = \frac{V_{in}\cdot D}{(1-D)^2}\,;\; V_{C0} = V_0 \tag{9}$$

Applying the ampere–sec balance principle to the capacitor equations in (2) and (4) yields the CCM current gain of the SSCG converter as summarized in (10):

$$G_{CCM} = \frac{I_{in}}{I_0} = \frac{1}{(1-D)^3}, \tag{10}$$

$$I_{in} = I_{L1} = \frac{I_0}{(1-D)^3};\; I_{L2} = \frac{I_0}{(1-D)^2};\; I_{L3} = \frac{I_0}{(1-D)} \tag{11}$$

B. Voltage Gain in DCM:

During DCM operation, the ampere–sec balance principle is employed for the capacitor C_0 as shown in Fig. 2(c). The expression is given in equation (12):

$$I_{C_0} = \tfrac{1}{2} I_{L_{3p}} D_x - I_0 = 0 \tag{12}$$

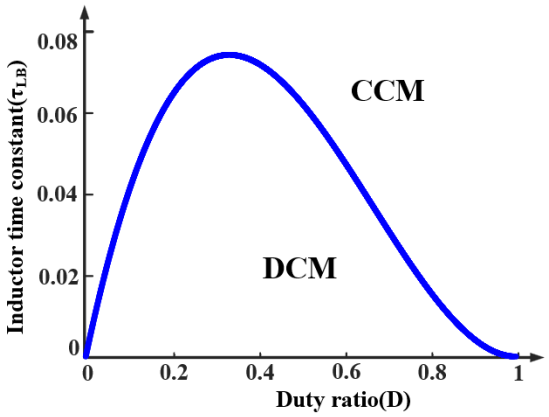


Fig. 4. Boundary conditions of the proposed converter.

The voltage gain of the proposed converter in DCM is expressed as in (13).

$$G_{\text{DCM}} = \frac{1 \pm \sqrt{1 - \frac{4(1-D)^4 D^2}{2r}}}{2(1-D)^4} \tag{13}$$

C. Operation of BCM:

The magnitudes of the charging and discharging currents of capacitor (C_0) are identical. therefore, their voltage gains are equal i.e, $G_{CCM} = G_{DCM}$ (or) Alternatively, this condition can also be obtained by equating the inductor ripple currents to twice their average values. The time constant of the inductor (L_3) at the boundary are expressed as:

$$\tau_{LB} = \frac{D \cdot (1-D)^2}{2} = \frac{L_3 f_s}{R_{\text{crit}}} \tag{14}$$

Figure. 4. illustrates how τ_{LB} varies as a function of the duty ratio (D). The following expression yields output critical resistance (R_{crit}) and is obtained in equation (15).

$$R_{\text{crit}} = \frac{2L_3 f_s}{D \cdot (1-D)^2} \tag{15}$$

D. Parameter Design and Selection for Converter:

i) Inductor design: The selection of inductors plays a crucial role in PV applications. The inductor design depends mainly on key operating parameters such as the maximum current ripple ($\%x_{L1}I_L$) allowable inductor current ripple (Δi_L), supply voltage (V_{in}), switching frequency (f_s) and duty cycle (D). Typically, the current ripple for inductors (L_1, L_2 and L_3) is maintained within 20%–40% ($\%x_{L1}$, $\%x_{L2}$ and $\%x_{L3}$) of the average inductor current. Consequently, the proposed converter uses inductors with a value of $L_1 = 500\,\mu$H, $L_2 = 1.5\,$mH, and $L_3 = 3\,$mH to sustain the continuous conduction mode (CCM) under all operational circumstances given by equation(16).

$$\begin{aligned}
L_1 &\geq \frac{V_{in}D}{(\%x_{L1})\, i_{L1_{avg}}\, f_s} \geq \frac{V_{in}^2 D}{(\%x_{L1})\, P_0\, f_s} \\
L_2 &\geq \frac{V_{C1}D}{(\%x_{L2})\, i_{L2_{avg}}\, f_s} \geq \frac{V_{in}^2 D}{(\%x_{L2})\,(1-D)^2\, P_0\, f_s} \\
L_3 &\geq \frac{(V_{C1}+V_{C2})D}{(\%x_{L3})\, i_{L3_{avg}}\, f_s} \geq \frac{V_{in}^2 D}{(\%x_{L3})\,(1-D)^4\, P_0\, f_s}
\end{aligned} \tag{16}$$

ii) Capacitor design: In addition to the inductor design, selecting suitable capacitors is a critical aspect of the converter's performance. The selection capacitors is influenced by parameters such as the maximum permitted voltage ripple(Δv_c) i.e.($\%y_{C1}V_C$), the operating voltage and the current that passes through each capacitor. Generally, the allowable voltage ripple is maintained between 1%–5%, represented as ($\%y_{C1}$,$\%y_{C2}$ and $\%y_{C0}$) as given in equation (17). Consequently, the design of the capacitors C_1, C_2 and C_0 is carried out based on the average voltage in each respective capacitor.

$$\begin{aligned}
C_1 &\geq \frac{I_{C1}D}{(\%y_{C1})\, V_{C1}\, f_s} \geq \frac{P_0(2-D)(1-D)^2}{(\%y_{C1})\, V_{in}^2\, f_s} \\
C_2 &\geq \frac{I_{C2}D}{(\%y_{C2})\, V_{C2}\, f_s} \geq \frac{P_0(1-D)^4}{(\%y_{C2})\, V_{in}^2\, f_s} \\
C_0 &\geq \frac{I_{C0}D}{(\%y_{C0})\, V_{C0}\, f_s} \geq \frac{P_0 D(1-D)^6}{(\%y_{C0})\, V_{in}^2\, f_s}
\end{aligned} \tag{17}$$

E. Voltage and Current stress on Switch and diodes:

During mode-II operation, the voltage stress represents the maximum blocking voltage across the switch and diodes (V_s) and (V_d) are subjected to it. In mode-I diodes (d_1, d_3 and d_0) experience voltage stress determined by using KVL. The corresponding equations are provided in equation(18).

$$\begin{aligned}
V_{d1} &= V_{C1} = \frac{V_{in}}{(1-D)} \\
V_{d2} &= V_{C1} - V_0 = \frac{V_{in}D(2-D)}{(1-D)^3} \\
V_{d3} &= V_{C1} + V_{C2} = \frac{V_{in}}{(1-D)^2} \\
V_{d4} &= V_{C1} + V_{C2} - V_0 = \frac{V_{in}D}{(1-D)^3} \\
V_{d0} &= V_s = V_0 = \frac{V_{in}}{(1-D)^3}
\end{aligned} \tag{18}$$

The voltage and current gain expressions of the SSCG converter include the term $(1-D)$ in the denominator, which may cause magnetic flux density and a risk of core saturation at high duty ratios as reported in [33]–[34]. A 200 W hardware prototype was developed with careful magnetic design, appropriate core material selection, proper air-gap configuration, and operation within safe flux density limits. No saturation effects were observed during experimental validation.

Similarly, current stress represents the highest current level that the device is required to carry while it remains in the ON state. By applying KCL at specific nodes, the current stresses on devices (S, d_2 and d_4) are derived for mode-1 while those on (d_1, d_3 and d_0) are obtained for mode-2. The current stress of switch (I_s) and diodes (I_d) are provided in equation(19).

$$\begin{aligned}
I_s &= D\,(I_{L1} + I_{L2} + I_{L3}) \\
I_{d1} &= (1-D)I_{L1}, \qquad I_{d2} = DI_{L1} \\
I_{d3} &= (1-D)I_{L2}, \qquad I_{d4} = DI_{L2} \\
I_{d0} &= (1-D)I_{L3}
\end{aligned} \tag{19}$$

F. Proposed SSCG Converter Efficiency Considering Component Nonidealities

Every component of the proposed converter contains parasitic elements that affect its performance. To evaluate their impact on voltage gain and efficiency, a non-ideal analysis is performed. The equivalent circuit incorporating these non-idealities is presented in Fig. 5(a). where, r_d and r_s represents the equivalent series resistance(ESR) of diodes and switch. Likewise, r_L and r_c represents the ESR's of the inductors and capacitors. Using CCM, the inductor voltage (V_{L1}) in mode-I and mode-II and output voltage of the SSCG converter are determined considering non-idealities as illustrated in Fig. 5(b), and it's efficiency is as shown in Fig. 5(c). The resulting expression provided in equations (20)–(22).

$$\begin{aligned}[V_{L1}]^{I} &= V_{in} - I_{L1}\left(r_{L1} + r_d + r_s\right) - V_d, \\ [V_{L1}]^{II} &= V_{in} - I_{L1}\left(r_{L1} + r_d + r_{C1}\right) - V_d - V_{C1}.\end{aligned} \tag{20}$$

$$V_{\text{0-parasitic}} = \frac{\frac{V_{in}}{(1-D)^3} - \frac{V_d}{(1-D)^3}}{1 + a\left(\frac{r_d}{R_0}\right) + b\left(\frac{r_s}{R_0}\right) + c\left(\frac{r_{L1}}{R_0}\right) + d\left(\frac{r_{c1}}{R_0}\right)} \tag{21}$$

$$a = \frac{1}{(1-D)^6}, \quad b = \frac{D}{(1-D)^6}, \quad c = \frac{1}{(1-D)^6}, \quad d = \frac{(1-D)}{(1-D)^6}$$

$$\eta = \frac{1 - \frac{V_d}{V_{in}}}{1 + a\left(\frac{r_d}{R_0}\right) + b\left(\frac{r_s}{R_0}\right) + c\left(\frac{r_{LL}}{R_0}\right) + d\left(\frac{r_{cL}}{R_0}\right)} \tag{22}$$

G. Power Loss Evaluation and Overall Efficiency:

Evaluation of Power Losses in Inductors and Capacitors:

The power losses on inductors and capacitors are mainly due to the inherent parasitic resistances (r_L) and (r_C). where as I_L, rms represents the RMS current flowing through the inductors and also it can be expressed as follows:

$$P_L = I^2_{L1\text{rms}} r_{L1} + I^2_{L2\text{rms}} r_{L2} + I^2_{L3\text{rms}} r_{L3} = 0.397W \tag{23}$$

I_C, rms represents the RMS current flowing through the capacitors.

$$P_C = \left(I^2_{C1\text{rms}} + I^2_{C2\text{rms}} + I^2_{C0\text{rms}}\right) r_C = 0.283W \tag{24}$$

Evaluation of Power losses in Diodes:

The power loss in the diodes arises primarily from their diode internal resistance (r_d) and the forward voltage drop (V_F). Where as $I_d(\text{avg})$ and $I_d(\text{rms})$ describes diodes average and RMS currents. Based on the equations (25) and (26), the following expressions can be represented by the power loss in diodes is as follows:

$$P_{di}-FV = V_{F(1,2,3,4,5)} I_d(1,2,3,4,5)(\text{avg}) = 5.75W \tag{25}$$

The power loss produced by the diode's forward ON-state resistance can be described as follows:

$$P_{di-rd} = I_d 1,2,3,4,5(\text{rms})^2 r_d = 1.08W \tag{26}$$

The total power losses in the diodes can be determined as

$$P_{di} - T = P_{di} - FV + P_{di-rd} = 6.83W \tag{27}$$

Evaluation of Power losses in MOSFET switches:

Power losses in MOSFET switches are primarily caused by switching and conduction losses.

where, f_{SW} is Switching frequency, V_{DS} is Peak voltage of switch, and $I_{S(pk)}$ is Peak current. The switching losses in the MOSFET switch can be given as:

$$P_{\text{S-switching}} = \frac{1}{2}(t_r + t_f) f_{\text{SW}} V_{DS} I_{S(\text{pk})} = 1.21W \tag{28}$$

Conduction losses in the switches are mainly caused by the on-state resistance $r_{s(on)}$ of the switch and I_{Srms} is RMS switch current can be given as:

$$P_{\text{S-conduction}} = I^2_{S\text{rms}} r_{s(\text{on})} = 0.66W \tag{29}$$

from equations (28) and (29),The total power losses of the MOSFET switch is

$$P_{\text{S-Total}} = P_{\text{S-conduction}} + P_{\text{S-switching}} = 1.87W \tag{30}$$

Total power losses can be calculated as follows:

$$P_T = P_L + P_C + P_{\text{S-Total}} + P_{di-T} = 9.38W \tag{31}$$

IV. Dynamic Modelling of SSCG Converter:

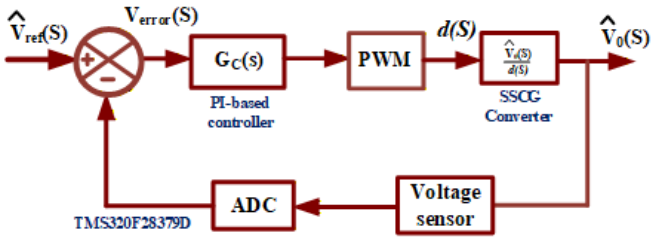
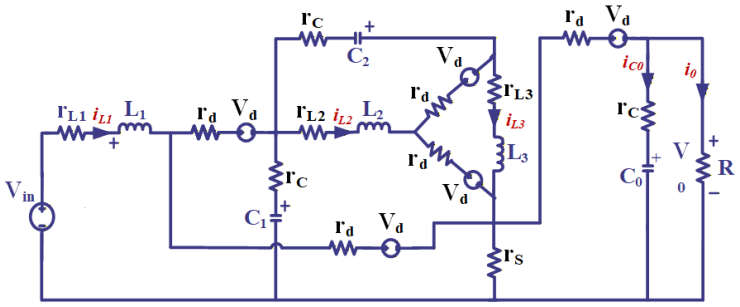
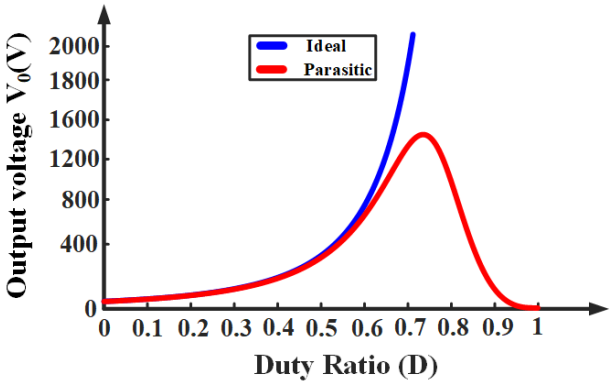


Fig. 7. Schematic diagram of dynamic voltage controller of the proposed SSCG converter.

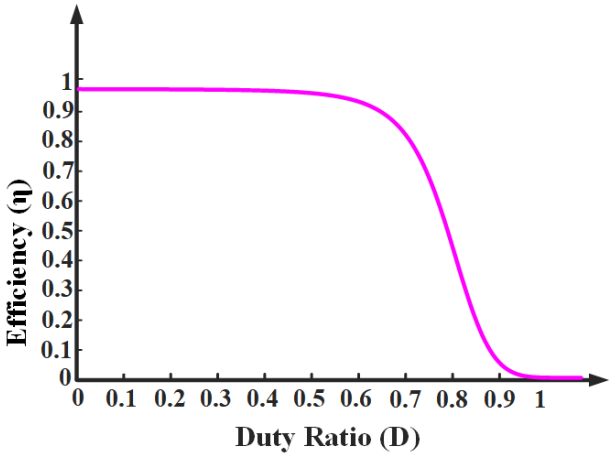
The dynamic model of the SSCG converter is formulated using the state-space averaging (SSA) method to describe its behavior in CCM. The converter operates over two switching intervals: Interval I (Switch ON) and Interval II (Switch OFF), each defined by distinct differential equations governing the inductor currents and capacitor voltages. The SSCG converter contains three inductors (L_1, L_2, L_3) and three capacitors (C_1, C_2, C_0), resulting in six state variables, includes inductor currents (i_{L1}, i_{L2}, i_{L3}) and capacitor voltages (V_{C1}, V_{C2}, V_{C0}). The system input is the source voltage $V_{in}(t)$, the output is the load voltage $V_0(t)$, and the control variable of the system is $d(t)$. The SSA technique linearizes the nonlinear switching behavior of the SSCG converter into a small-signal model by introducing small perturbations around the steady-state operating point while maintaining a constant duty cycle. The below state equations (32) and (33) are derived



(a)

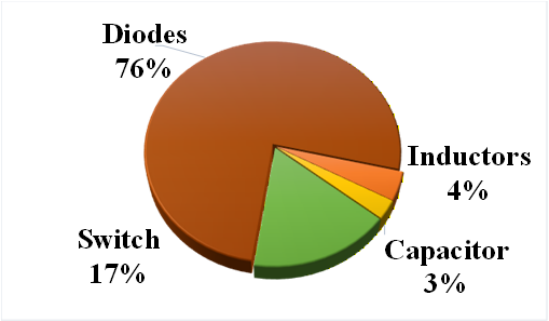


(b)

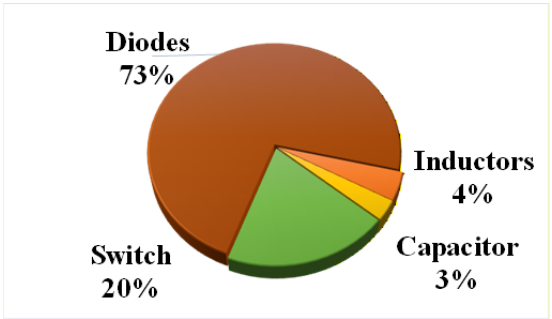


(c)

Fig. 5. Equivalent circuit of the SSCG converter including parasitic components (a) Parasitic circuit (b) $V_{0-(parasitic)}$vs$D$ (c) η vs D.



(a)



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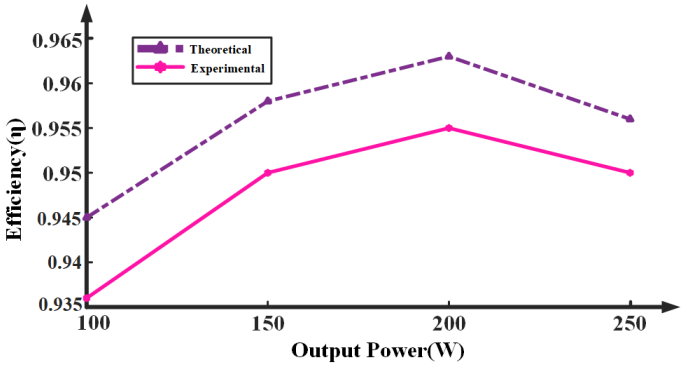


(c)

Fig. 6. Loss analysis of SSCG converter (a) Ideal (b) Practical (c) efficiency(η) Vs Output power(W).

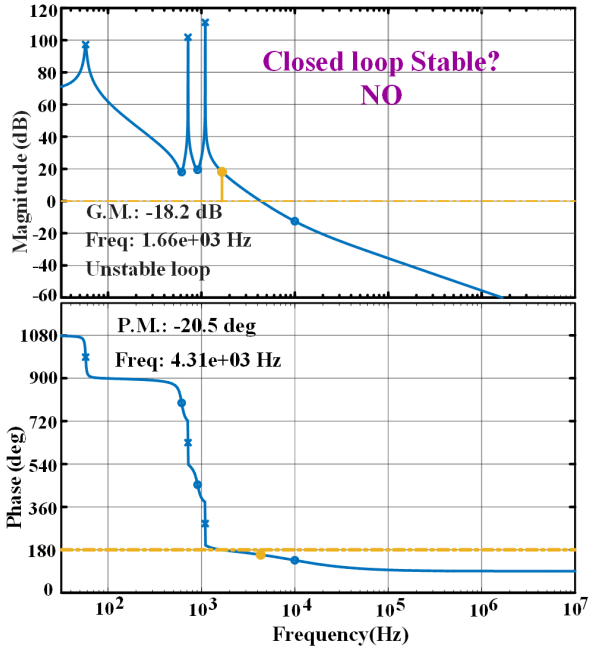
using the proposed SSCG converter corresponding to the ON and OFF time intervals.

$$\begin{cases} \dfrac{di_{L1}(t)}{dt} = \dfrac{V_{in}}{L_1} \\ \dfrac{di_{L2}(t)}{dt} = \dfrac{V_{C1}}{L_2} \\ \dfrac{di_{L3}(t)}{dt} = \dfrac{V_{C1}}{L_3} + \dfrac{V_{C2}}{L_3} \\ \dfrac{dv_{C1}(t)}{dt} = -\dfrac{i_{L2}}{C_1} - \dfrac{i_{L3}}{C_1} \\ \dfrac{dv_{C2}(t)}{dt} = -\dfrac{i_{L3}}{C_2} \\ \dfrac{dv_{C3}(t)}{dt} = -\dfrac{v_{C0}}{R_0 C_0} \end{cases} \quad \text{(S 'ON' time)} \qquad (32)$$

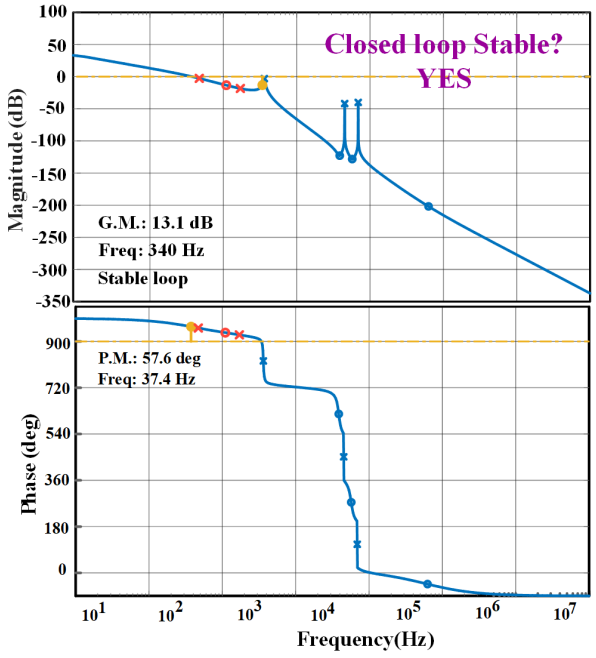
$$\begin{cases} \dfrac{di_{L1}(t)}{dt} = \dfrac{V_{in} - V_{C1}}{L_1} \\ \dfrac{di_{L2}(t)}{dt} = -\dfrac{V_{C2}}{L_2} \\ \dfrac{di_{L3}(t)}{dt} = \dfrac{V_{C1}}{L_3} + \dfrac{V_{C2}}{L_3} - \dfrac{V_{C0}}{L_3} \\ \dfrac{dv_{C1}(t)}{dt} = \dfrac{i_{L1}}{C_1} - \dfrac{i_{L3}}{C_1} \\ \dfrac{dv_{C2}(t)}{dt} = \dfrac{i_{L2}}{C_2} - \dfrac{i_{L3}}{C_2} \\ \dfrac{dv_{C0}(t)}{dt} = \dfrac{i_{L3}}{C_0} - \dfrac{v_{C0}}{R_0 C_0} \end{cases} \quad \text{(S 'OFF' time)} \qquad (33)$$

The small-signal model of the SSCG converter is developed by introducing perturbations to its state variables and separating them into steady-state and dynamic components. assuming no disturbances on the input side, the corresponding control-to-output transfer function is derived and presented in equation (37). To ensure stable output voltage regulation, a PI controller is incorporated into the system as shown in Fig.7.

where it maintains the output voltage(V_0) under varying operating conditions. The output voltage is regulated by using a PI controller with K_P= 0.00048023 and K_I= 0.0023441, respectively. These parameters were obtained by using the closed-loop Ziegler–Nichols tuning approach, which offers systematic procedure to achieve a satisfactory compromise between dynamic response and stability margins. The stability of the SSCG converter under closed-loop operation is assessed through Bode plot analysis of both the open-loop and closed-loop systems are presented in Fig. 8(a) and Fig. 8(b) respectively, which compare the system response with and without the controller. The gain and phase margins reported in the plots further verify that the PI-controlled SSCG converter exhibits enhanced stability and robust dynamic characteristics.



(a)



(b)

Fig. 8. Bode plot of SSCG converter (a) Using without controller (b) Using with controller.

V. Performance Evaluation

The performance of the proposed SSCG converter is evaluated and compared with various existing topologies reported in the literature [20]–[30] to highlight its advantages and efficiency (η) at the specified duty ratio. A detailed comparative analysis considering parameters such as voltage gain, total component count, circuit order, TCVS and the frequency, power, and efficiency ($f/P/\eta$) are presented in Table II.

The proposed SSCG converter achieves cubic voltage gain, similar to [28], [29]. Although converters [21], [23], [28] employ similar number of total devices and converters that achieves a quadratic or high voltage gain compared to the converters mentioned in [20]–[27] and [30] they rely on mul-

The state-space model equations (34) and (35) are derived from (32) and (33), respectively, for ON and OFF time intervals and are expressed as follows:

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{i}_{L3}(t))}{dt} \\ \frac{d\hat{i}_{C1}(t)}{dt} \\ \frac{d\hat{i}_{C1}(t)}{dt} \\ \frac{d\hat{i}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_3} & \frac{1}{L_3} & 0 \\ 0 & -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_0C_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ -\frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_i n(t)$$

$$V_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{i}_{L3}(t) & \hat{v}_{C1}(t) & \hat{v}_{C2}(t) & \hat{v}_{C0}(t) \end{bmatrix}^T \tag{34}$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{i}_{L3}(t))}{dt} \\ \frac{d\hat{i}_{C1}(t)}{dt} \\ \frac{d\hat{i}_{C1}(t)}{dt} \\ \frac{d\hat{i}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{1}{L_3} & 0 & -\frac{1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_0} & 0 & 0 & -\frac{1}{R_0C_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ -\frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_i n(t)$$

$$V_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{i}_{L3}(t) & \hat{v}_{C1}(t) & \hat{v}_{C2}(t) & \hat{v}_{C0}(t) \end{bmatrix}^T \tag{35}$$

The state variable matrix of the SSCG converter is represented in equation (36). The SSA model was obtained from

$$A = A_1 D + A_2(1-D)$$
$$B = B_1 D + B_2(1-D)$$
$$C = C_1 D + C_2(1-D)$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{i}_{L3}(t))}{dt} \\ \frac{d\hat{i}_{C1}(t)}{dt} \\ \frac{d\hat{i}_{C1}(t)}{dt} \\ \frac{d\hat{i}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{(1-d)}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{d}{L_2} & -\frac{(1-d)}{L_2} & 0 \\ 0 & 0 & 0 & \frac{1}{L_3} & \frac{1}{L_3} & -\frac{(1-d)}{L_3} \\ \frac{(1-d)}{C_1} & -\frac{d}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{(1-d)}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{(1-d)}{C_0} & 0 & 0 & -\frac{1}{R_0C_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{i}_{L3}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ -\frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in}(t) + [F]\hat{d}$$

$$V_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{i}_{L3}(t) & \hat{v}_{C1}(t) & \hat{v}_{C2}(t) & \hat{v}_{C0}(t) \end{bmatrix}^T \tag{36}$$

$$G_{vd}\left(\frac{\hat{v}_{out}(s)}{\hat{d}_s}\,\middle|\,\hat{v}_{in}(s)=0\right) = \frac{-1.041\times10^4 s^5 + 6.667\times10^8 s^4 - 1.337\times10^{12} s^3 + 3.157\times10^{16} s^2 - 2.287\times10^{19} s + 3.175\times10^{23}}{s^6 + 12.50\,s^5 + 6.808\times10^7 s^4 + 8.415\times10^8 s^3 + 9.786\times10^{14} s^2 + 1.186\times10^{16} s + 1.271\times10^{20}} \tag{37}$$

tistage energy transfer mechanism involving a larger number of passive components and intermediate energy storage stages. These configurations may increase circuit order, conduction losses, and consequently result in lower efficiency and slower dynamic response. First of all, the proposed SSCG converter is assessed in terms of voltage gain and compared with other converters as illustrated in Fig. 9(a). it is clear that the proposed SSCG converter achieves high voltage gain at moderate duty ratios through a simple energy transfer path, thereby improving overall efficiency compared with other existing converters. Some of the converters [22], [23], [26], [27], [29], [30] employ two switches, which increase conduction losses and the circuit becomes complex. Additionally, several compared converters [23], [24], [26]–[28] do not provide a common ground

TABLE I
SUMMARY OF PROPOSED AND EXISTING CONVERTER TOPOLOGIES

Ref	Year	Voltage Gain $\left(\frac{V_o}{V_{in}}\right)$	TCVS $\left(\frac{\sum V_C}{V_o}\right)$	Duty (D)	d/L/C/S	SO	C.G	f(kHz)/P (W)	η (% @200W)
20	2023	$\frac{1-2D^2+2D}{(1-D)^2}$	$\frac{3+5D-5D^2}{1-2D^2+2D}$	$D=\frac{G+1-\sqrt{G+3}}{G+2}$	5/4/6/1 = 16	10	Yes	50/200	90%
21	2024	$\frac{1+D}{(1-D)^2}$	$\frac{2+3D-D^2}{1+D}$	$D=\frac{(2G+1)-\sqrt{8G+1}}{2G}$	4/3/4/1 = 12	7	Yes	50/200	90%
22	2024	$\frac{4}{(1-D)^2}$	$\frac{(D-3)^2}{4}$	$D=\frac{\sqrt{G-4}}{\sqrt{G}}$	6/4/4/2 = 16	8	Yes	50/200	93.5%
23	2024	$\frac{(2-D)^2}{(1-D)^2}$	$\frac{3D^2-10D+8}{(2-D)^2}$	$D=\frac{\sqrt{G}-2}{\sqrt{G}-1}$	4/2/4/2 = 12	6	No	50/200	92.8%
24	2025	$\frac{3-D}{(1-D)^2}$	$\frac{10-5D}{3-D}$	$D=\frac{(2G-1)-\sqrt{8G+1}}{2G}$	6/2/6/1 = 15	8	No	50/100	NS
25	2024	$\frac{3}{(1-D)^2}$	$\frac{6-D}{3}$	$D=\frac{\sqrt{G}-\sqrt{3}}{\sqrt{G}}$	7/3/5/1 = 16	8	Yes	50/120	NS
26	2025	$\frac{4-2D}{(1-D)^2}$	$\frac{7-4D}{4-2D}$	$D=\frac{(G-1)-\sqrt{2G+1}}{G}$	5/2/5/2 = 14	7	No	50/200	92%
27	2024	$\frac{3-D}{(1-D)^2}$	$\frac{D(5D^2-14D+9)}{(3-D)(1-D)}$	$D=\frac{(2G-1)-\sqrt{8G+1}}{2G}$	5/2/5/2 = 14	7	No	50/200	95%
28	2023	$\frac{D}{(1-D)^3}$	$\frac{D^2-2D+2}{D}$	$D=\sqrt[3]{\left(\frac{1}{2G}-\sqrt{\frac{27G+4}{108G^3}}\right)}$	5/3/3/1 = 12	6	No	50/200	89%
29	2021	$\frac{1}{(1-D)^3}$	$(D-2)^2$	$D=1-\frac{1}{\sqrt[3]{G}}$	5/3/4/2 = 14	7	Yes	40/280	91%
30	2023	$\frac{1}{(1-D)^2}$	$2-D^2$	$D=\frac{\sqrt{G-1}}{\sqrt{G}}$	2/2/2/2 = 8	4	Yes	20/200	NS
Proposed	SSCG	$\frac{1}{(1-D)^3}$	$2-D$	$D=1-\frac{1}{\sqrt[3]{G}}$	5/3/3/1 = 12	6	Yes	50/200	95.5%

Ref = Reference, TCVS = total capacitor voltage stress, d = diodes, L = inductors, C = capacitors, S = switch, SO = system order, C.G = Common ground, f = switching frequency (kHz), P = Power (W), η = efficiency, NS = Not Specified.

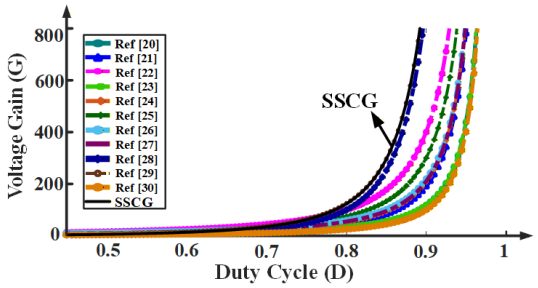
structure, which complicates system performance. The next parameter considered for comparison is TCVS as shown in Fig. 9(b). the proposed SSCG converter maintains lower TCVS among all the compared converters. Another parameter used for comparison is the Effectiveness Index (EI), which ensures consistency among the selected topologies. The EI represents the voltage gain obtained per component, thereby correlating the voltage gain with the total number of components, as shown in Fig. 9(c). The EI analysis further confirms that the proposed SSCG topology exhibits a higher EI compared to most existing converters. It is observed that, the SSCG

converter achieves high voltage gain, lower TCVS, common-ground operation, and improved efficiency (95.5% at 200 W), indicating a superior trade-off between performance and implementation complexity.

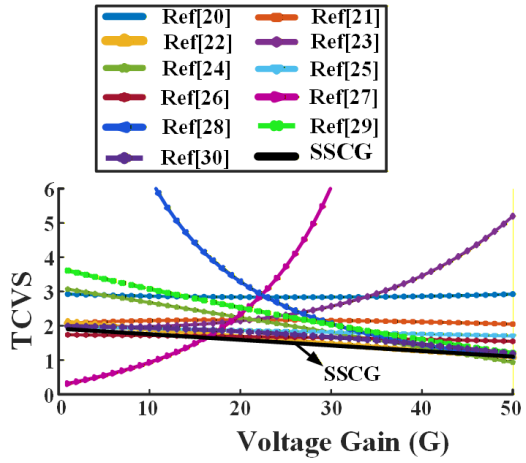
VI. PROTOTYPE VALIDATION

A 200 W, 50 kHz hardware prototype of the SSCG converter was implemented to experimentally validate steady-state performance and conversion efficiency, as depicted in Fig. 10. The detailed design parameters and component specifications are summarized in Table II. gate pulse for the switch is generated using a DSP controller (TMS320F28379D), enabling precise duty cycle control and stable operation.

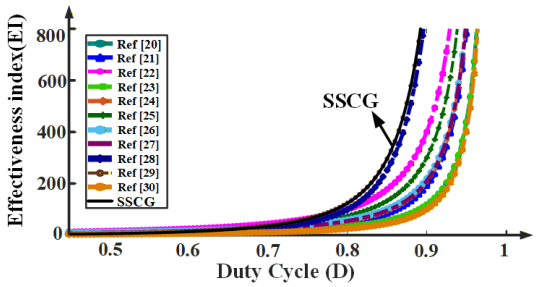
The prototype was evaluated at an input voltage of 48 V with a duty ratio of $D = 0.508$. Under these operating conditions, the converter delivers an output voltage of 390 V and an output current of 0.49 A, as shown in Fig. 11(a). The measured efficiency at the rated output power of 200 W is 95.5%, which confirms the high step-up capability and effectiveness of the proposed topology. Fig. 11(b) and 11(c) present the experimentally obtained inductor voltages V_{L1},



(a)



(b)



(c)

Fig. 9. Performance comparison of Proposed SSCG converter(a) Voltage gain(G) vs Duty ratio(D), (b) Total capacitor voltage stress($TCVS$) vs Gain(G), (c) Effectiveness index(EI) vs. D

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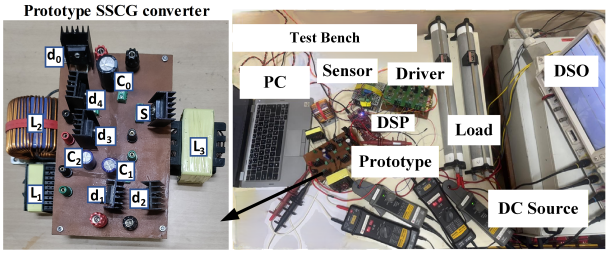

Fig. 10. Hardware prototype of proposed SSCG converter.

V_{L2}, V_{L3} along with their respective currents i_{L1}, i_{L2} and i_{L3} respectively, recorded during the switching intervals. The measured capacitor voltages C_1 and C_2 are shown in Fig. 11(d). In addition, Figs. 11(e),11(f) and 11(g) depict the measured voltage stresses across switch and diodes. The

TABLE II
DESIGN AND OPERATING PARAMETERS

Parameter	Rating
Input voltage	48 V
Output voltage	400 V
Output Power (P_o)	200 W
Inductors	$L_1 = 500\,\mu$H
	$L_2 = 1.5$ mH, $L_3 = 3$ mH
	$r_{L1} = r_{L2} = r_{L3} = 0.01\,\Omega$
Capacitors	$C_1 = 22\,\mu$F, $C_2 = 22\,\mu$F
	$C_0 = 100\,\mu$F
	$r_{C1} = r_{C2} = r_{C0} = 0.01\,\Omega$
Diode (d_1)	MBR10100
	$r_{d1} = 0.01\,\Omega$
Diodes (d_2, d_3, d_4, d_0)	MUR840G
Switch	STW28N65M2
	$r_{s_on} = 150\,$mΩ

experimental results obtained are in close agreement with the theoretical analysis and confirms the high efficiency and reliable steady-state performance of the proposed SSCG converter.

The dynamic performance of the proposed SSCG converter was examined under sudden load disturbances and input voltage variations. As shown in Fig. 11(h). the converter successfully regulates the output voltage at 400 V during step changes between half-load and full-load conditions. Fig. 11(i). illustrates the response of the converter to sudden input voltage variations in the sequence of 48 V– 58 V–48 V–38 V–48 V. In all cases, the implemented PI controller ensures minimal overshoot and rapid settling of the output voltage. These results confirm the robustness of the control scheme against load and source perturbations, thereby maintaining stable operation under varying operating conditions.

VII. CONCLUSION

In this work, a high step-up single switch based cubic gain DC–DC converter is proposed for PV applications. The topology achieves a cubic voltage gain through the combined operation of three inductors, capacitors and five diodes while employing only a single switch. A comprehensive analysis of the SSCG converter is carried out under CCM, DCM and BCM operating modes. A 200 W hardware prototype designed for a 48 V input and a 400 V output is developed to validate CCM operation. The study further investigates the voltage stress across each component and presents a comparative evaluation with recently reported high-gain converters. In addition, the efficiency of the proposed converter is analyzed by considering non-idealities and closed loop control is implemented to demonstrate its superior performance. The SSCG converter ensures a minimum total component count continuous and low-ripple input current, high voltage gain in a moderate duty ratio (D = 0.508) and a common-ground configuration provides an

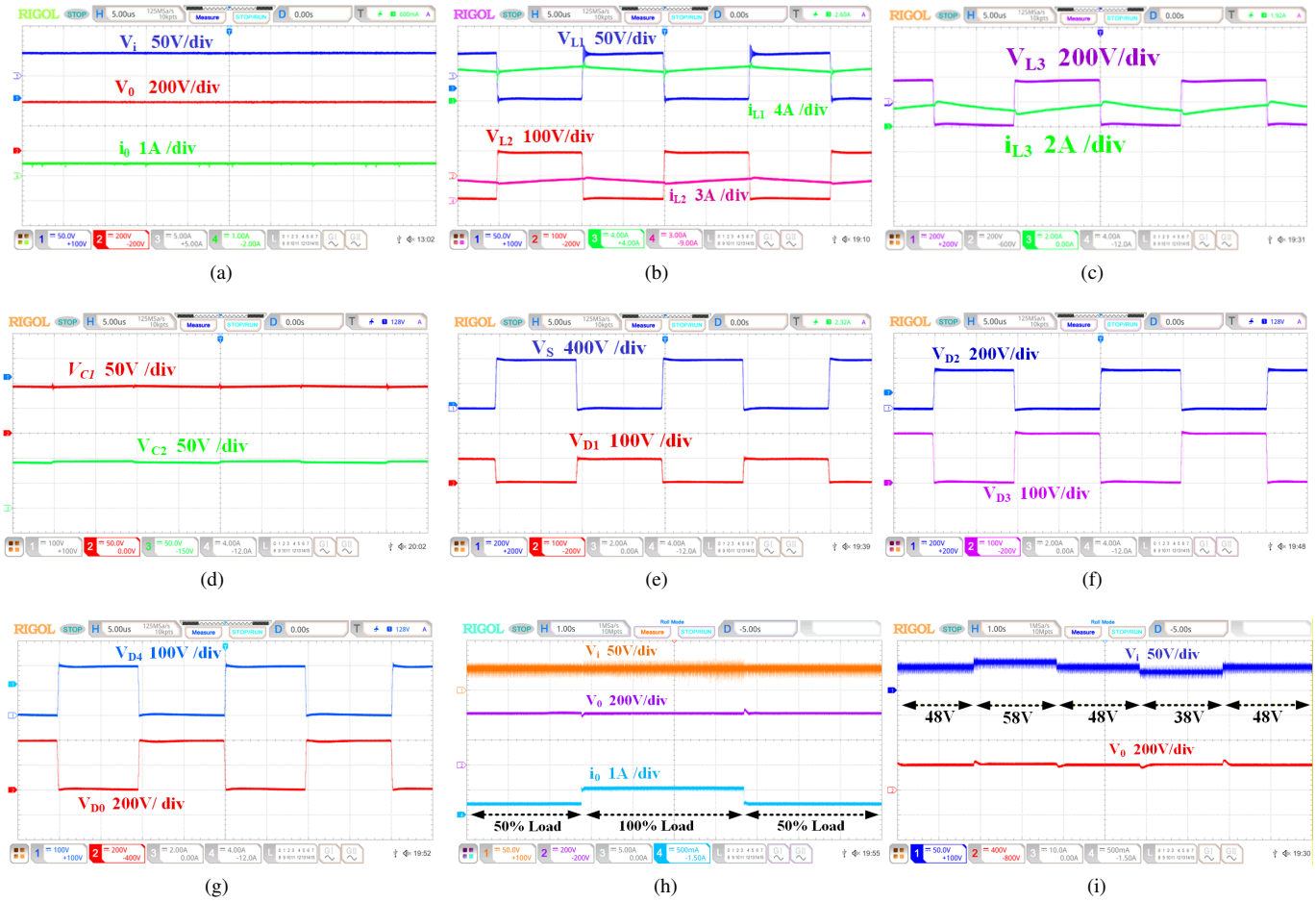

Fig. 11. Hardware evaluation results of the proposed SSCG converter: (a) Input voltage, output voltage and current; (b) Inductor voltages and currents $V_{L1}, I_{L1}, V_{L2}, I_{L2}$ (c) Inductor voltage and current V_{L3}, I_{L3} (d) Capacitor voltages V_{C1}, V_{C2} (e) Switch voltage V_S, Diode voltage V_{d1} (f) Diode voltages V_{d2}, V_{d3} (g) Diode voltages V_{d4}, V_{d0} (h) Closed-loop load variation response (i) Sudden variation in input voltage.

efficient, reliable and structurally optimized solution suitable for high step-up PV energy conversion systems.

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