Analysis and Modeling of a Boost Converter with Power Processing Reduction for PV Applications

Iván A. Reyes-Portillo, Saúl R. Méndez-Elizondo, Jorge A. Morales-Saldaña, Jorge U. Muñoz-Minjares, Claudia A. Rivera-Romero, and Dora L. Castro-López

***Abstract*—The use of photovoltaic (PV) systems has experienced rapid development as part of renewable energy sources. These systems require DC/DC converters with wide transformation ranges to provide regulated output voltages. In PV applications isolated from the electrical grid, output voltage levels of 24 V and 48 V have commonly been reported. Due to the inherent low efficiency of PV modules, it is essential that the converter performs highly efficient power processing in order to properly utilize the energy generated. This paper proposes the analysis of a boost converter based on the concept of Partial Power Processing (PPP) as an alternative for photovoltaic applications. The analysis and evaluation of PPP are presented through modeling in the Volt-Ampere area, as well as through the study of the dynamic effects that this type of processing introduces into the system. Additionally, the switched and linear models of the converter are developed, along with the analysis of PPP through the buffer element. Finally, the obtained results through simulations and experimental measurements are presented, demonstrating a 4.21% increase in the overall efficiency of the system compared to the conventional boost converter.**

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***Index Terms*—DC/DC, VA modeling, Partial power processing, PV applications, Boost converter**

I. Introduction

In recent decades, new DC/DC converter topologies have been developed with the aim of meeting the operational requirements of renewable energy sources [1], [2]. However, one of the main challenges has been to increase the power processing efficiency of these systems [3]. In particular, photovoltaic (PV) panels have relatively low conversion efficiencies, on the order of 25% [4]. If this limitation is considered along with efficiency losses in the DC/DC converter, the overall performance is compromised, resulting in an energetically inefficient solution [5].

Various approaches have been proposed in the literature to increase the efficiency of DC/DC converters. A concept that has become important in recent years for improving the efficiency of DC/DC converters is partial power processing [6]. This approach consists of transferring a fraction of the input power directly to the load, thereby reducing the power that must be actively processed by the converter [6], [7]. The PPP concept has been shown to provide significant improvements in the overall efficiency of DC/DC structures [8]. In [9], a classification of three PPP-based architectures is proposed, which are described below:

a) Partial Power Converters (PPC): the main purpose is to control the power flow, current and voltage level between the source and the load.

b) Differential Power Converters (DPC): these converters are designed to compensate for current imbalances between the different elements connected in series or parallel to the same voltage bus.

c) Mixed strategies: this structure combines the two previous concepts, reducing in structures with partial pseudo-processing, as the presented in [10], [11]. Fig. 1 shows the general structures of converters with PPP according to the above classification.

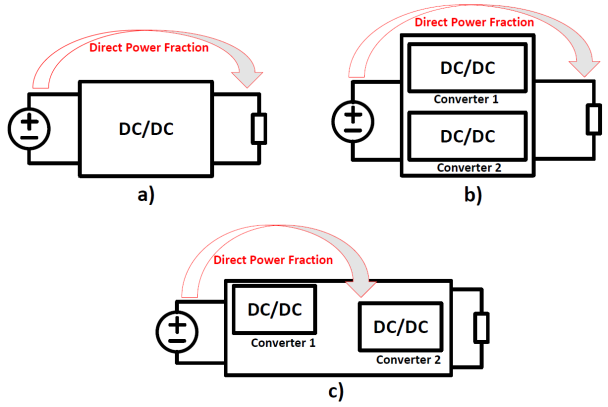

Fig. 1. General structures with partial power processing, a) PPC, b) DPC, and c) Mixed strategies.

The PPP converters have been used in multiple applications, such as electric vehicles, lighting and energy storage [12], [13]. However, there are still several aspects that require further analysis in this type of structure. These include measuring the fraction of power that is processed through the buffer, identifying the variables that influence partial power processing, and studying the dynamic effects associated with the direct path between the DC bus and the load. In [14]–[17], Boost structures with partial power processing (PPP)

The associate editor coordinating the review of this manuscript and approving it for publication was Roberto S. Murphy (*Corresponding author: Iván Alfonso Reyes-Portillo*).

Iván Alfonso Reyes-Portillo, and J. Muñoz-Minjares are with Universidad Autónoma de Zacatecas, Zacatecas, México (e-mails: ivan.reyes@upslp.edu.mx, and ju.munoz@uaz.edu.mx).

S. Méndez-Elizondo, J. Morales-Saldaña, and D. Castro-López are with Universidad Autónoma de San Luis Potosí, San Luis Potosí (e-mails: saul.mendez@uaslp.mx, jmorales@uaslp.mx, and dora.castro@upslp.edu.mx).

C. Rivera-Romero is with Instituto Nacional de Astrofísica, Óptica y Electrónica, Puebla, México (e-mail: c.a.riveraromero@inaoe.mx).

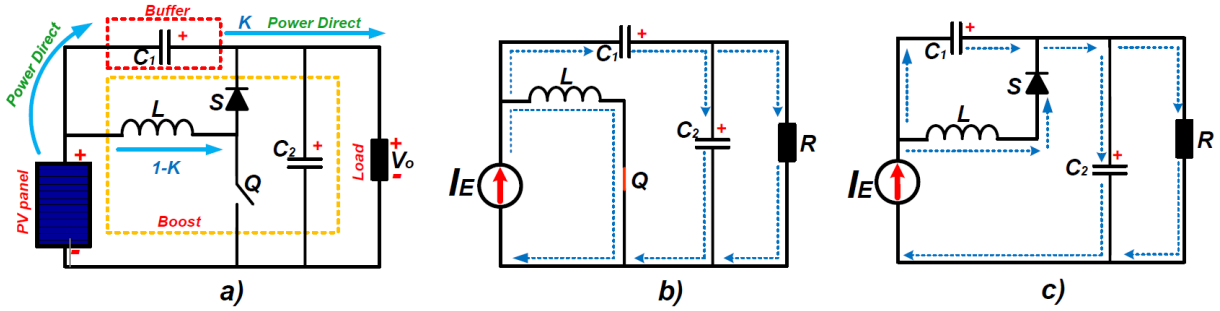

Fig. 2. Electrical networks of the proposed converter, a) Boost converter with partial power processing, b) electrical networks corresponding of the ON state, and c) electrical networks corresponding of the OFF state.

are reported where exhibit high overall efficiency; however, the fraction of power transferred directly between the source and the load is not quantified or analyzed. Such analysis is key to understanding the power flow and the optimization of the design and operation of DC/DC converters. This paper presents a study of a boost converter belonging to the family of partial power processing (PPC) converters, powered by a photovoltaic panel, as shown in Fig. 2(a). The analysis focuses on determining the fraction of power processed by the Boost-PPP converter. Additionally, experimental results are presented that validate the theoretical analysis. This analysis identifies the main parameters that influence partial power processing and, consequently, the overall efficiency of the converter.

The rest of the paper is organized as follows: in Section II is shown the analysis of operation in continuous conduction mode, its converter transformation ratio, the design equations of the reactive elements. The steady state average current/voltage values and the system dynamics based on its transfer function are presented. Section III presents the analysis of the power processing in the converter through Volt-Amper (VA) area modeling. In Section IV, the obtained results theoretically are validated in an experimental prototype. Finally, in Section V, final comments are presented.

II. Boost Converter with Partial Power Processing

The PV panels are modeled as current sources due to their functional nature [18]. Since this converter is proposed for PV applications, a current source has been considered at the input of the converter. The converter behavior is in Continuous Conduction Mode (CCM) where two operating states are presented. In the ON state the switch Q conducts and the diode S is off as shown in Fig. 2(b). In the OFF state, the S diode conducts current and the Q switch is off as shown in Fig. 2(c). The waveforms of the Boost converter with PPP during a switching period (T_s) are shown in Fig. 3, considering the operation of the converter in CCM and without parasitic resistors. The waveforms are the control voltage at the MOSFET gate (V_G), the voltage at the buffer capacitor (V_{C_1}), the voltage at the output capacitor (V_{C_2}), the voltage across the inductor (V_L), the current through the inductor (I_L), and the current through the buffer capacitor (I_{C_1}).

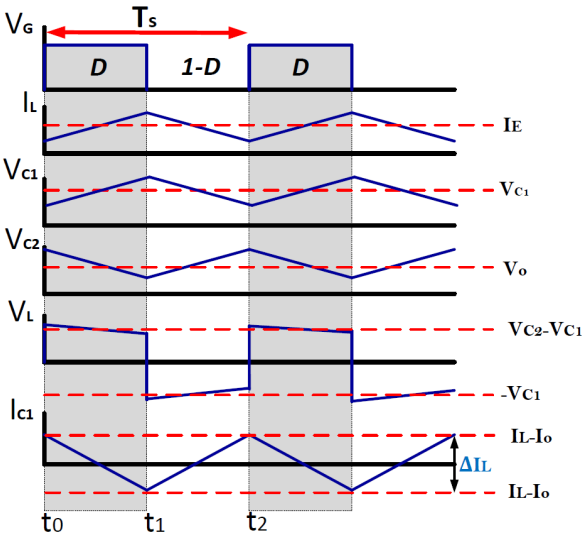

Fig. 3. Current and voltage waveforms during a switching period present in reactive elements.

In Equations (1-3) are obtained the expression for the average current/voltage values in terms of input current (I_E), duty ratio (D) and the load (R).

$$V_{C_1} = I_E D(1-D)R \tag{1}$$

$$V_{C_2} = I_E(1-D)R \tag{2}$$

$$I_L = I_E \tag{3}$$

Considering the Amper-Second balance in the capacitor current C_2, Equation (4) is obtained.

$$(I_E - I_L - I_o)DTs + (I_E - I_o)(1-D)T_s = 0 \tag{4}$$

Substituting the average value of the inductor current (I_L) in the Equation (4) gives the Equation (5) that determines the converter gain in terms of input/output current.

$$M = \frac{I_o}{I_E} = (1-D) \tag{5}$$

Considering the average voltage value in the inductor L during the interval from t_0 to t_1, Equation (6) is obtained, which determines the value of the current ripple in the inductor ΔI_L

in terms of the inductance (L) and the switching frequency (f_s).

$$\Delta I_L = \frac{I_E D(1-D)^2 R}{Lfs} \tag{6}$$

To obtain the value of the voltage ripple in capacitor C_1 there is a direct dependence on the inductor current ripple value. The equation (7) determines the ripple value of the capacitor C_1.

$$\Delta V_{C_1} = \frac{I_E D(1-D)^2 R}{8LC_1 f_s^2} \tag{7}$$

To obtain the value of the voltage ripple (ΔV_{C_2}) in capacitor C_2, the interval from t_1 to t_2 of the switching period is analyzed, which is given by:

$$\Delta V_{C_2} = \frac{I_E(1-D)^2}{C_2 f_s} \tag{8}$$

The current/voltage ripple in the reactive elements will depend on the requirements of the load and the applications. However, these parameters play a fundamental role in the partial power processing in the converter.

A. Modeling of the Converter

The converter modeling was performed from the electrical networks shown in Fig. 2(b), using the state-space technique. The state variables are the capacitor voltages and the inductor current. The ON model for the interval from t_0 to t_1 is determined by the Equation 9.

$$\dot{x}_1 = \begin{bmatrix} \dot{i}_L \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{1}{L_1} \\ \frac{1}{C_1} & 0 & 0 \\ -\frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C_1} \\ \frac{1}{C_2} \end{bmatrix} i_e \tag{9}$$

The model in the OFF state corresponding to the interval t_1 to t_2 is determined by the Equation 10.

$$\dot{x}_2 = \begin{bmatrix} \dot{i}_L \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C_1} & 0 & 0 \\ 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C_1} \\ \frac{1}{C_2} \end{bmatrix} i_e \tag{10}$$

Using Equations (9-10), it is possible to obtain a unified model by integrating the switching function in way as presented in Equation 11.

$$\dot{x} = \dot{x}_1 D + \dot{x}_2(1-D) \tag{11}$$

The average model of the Boost converter with PPP in is given by:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{D}{L} \\ \frac{1}{C_1} & 0 & 0 \\ -\frac{D}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C_1} \\ \frac{1}{C_2} \end{bmatrix} i_e \tag{12}$$

To obtain a valid linear representation at an operating point of the system, the variables are perturbed with small AC signals, such that $D = D + \widetilde{d}$ and $i_E = I_E + \widetilde{i}_e$, resulting in a linear model given by:

$$\begin{bmatrix} \dot{\widetilde{i}}_L \\ \dot{\widetilde{v}}_{C_1} \\ \dot{\widetilde{v}}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{D}{L} \\ \frac{1}{C_1} & 0 & 0 \\ -\frac{D}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} \widetilde{i}_L \\ \widetilde{v}_{C_1} \\ \widetilde{v}_{C_2} \end{bmatrix} + \begin{bmatrix} 0 & \frac{V_{C_2}}{L} \\ -\frac{1}{C_1} & 0 \\ \frac{1}{C_2} & -\frac{I_E}{C_2} \end{bmatrix} \begin{bmatrix} \widetilde{i}_e \\ \widetilde{d} \end{bmatrix} \tag{13}$$

The principal interest in this structure is to achieve regulation of the output voltage v_{C2}. Frequently, the regulation task in Boost converter is achieved using a double control loop, where the inner loop feeds back the current in the inductor and the outer loop feeds back the output voltage. The reason is that the transfer function of the inductor current with respect to the duty ratio of a conventional Boost converter is minimum phase (no zeros on the right side) in order to increase the speed of the control scheme for disturbances. From (13), the transfer function relating the output voltage to the duty ratio of the PPP-based boost converter is obtained and given by:

$$\frac{V_o(s)}{d(s)} = \frac{RI_E\left[C_1 L s^2 + C_1 RD(1-D)s + 1\right]}{C_1 C_2 LRs^3 + C_1 Ls^2 + (C_1 RD^2 + C_2 R)s + 1} \tag{14}$$

Based on the Equation (14), it is possible to locate the position of the poles and zeros of the system, which determine its dynamic behavior. Fig. 4 shows the poles and zeros in the s-plane of the transfer function G_{vd} considering variations in the parameters C_1, C_2, L and D. The poles and zeros maintain their location on the left side of the s-plane presenting a minimum phase dynamics the transfer function (14) under parameter variation. With the variation of the parameters the C_1 and C_2, the real pole approaches the origin. These dynamic behaviors present a great advantage in the controller design due to the minimum phase of the system at the output voltage.

III. Analysis of Partial Power Processing

The power processing analysis is of great relevance to show the benefits of the structure with PPP. For the power processing analysis, the "V·A area modeling" was employed [18], [19]. This method describes graphically the average powers that are processed in each stage of the system in a steady state [20], [21]. The method considers that the input and output power are approximate ($P_{in} \approx P_o$), it does not consider losses due to parasitic effects. Fig. 5 presents the areas related to the input and output power of the proposed converter using the average input and output current/voltage values. In this method, the following concepts are defined: a) *Direct Power* (P_{dir}): It is the power that is transferred from one port to another without the internal passage through a storage element (capacitors and inductors). b) *Indirect Power* (P_{ind}): It is the power that is stored and delivered during the transfer process in the converter. The P_{ind} power is processed by the reactive elements (capacitors and inductors). c) *Differential Power* (P_{dif}): It is the lower limit of the power processing required to deliver a given power to the output. This is generated by the action of the switching devices and is processed by the reactive elements (inductors and capacitors).

A. Analysis of the Convetional Boost Converter

The V·A area analysis is a useful tool for modeling the power processing of DC/DC converters. In the conventional boost converter, it presents the indirect power transfer through

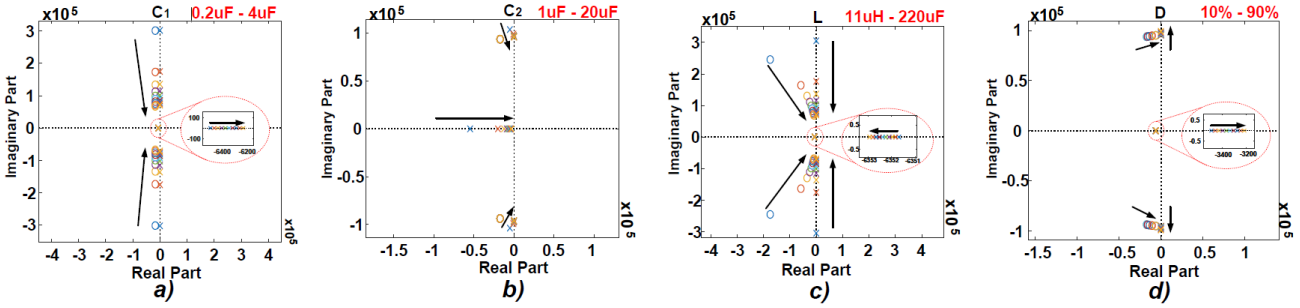

Fig. 4. Poles and zeros of the transfer function in (14) under parametric variations, a) variation of capacitor C_1 (0.2 μF to 4 μF), b) variation of capacitor C_2 (1 μF to 20 μF), c) variation of inductor L (11 μH to 220 μH), and d) variation of duty ratio D (10% to 90%).

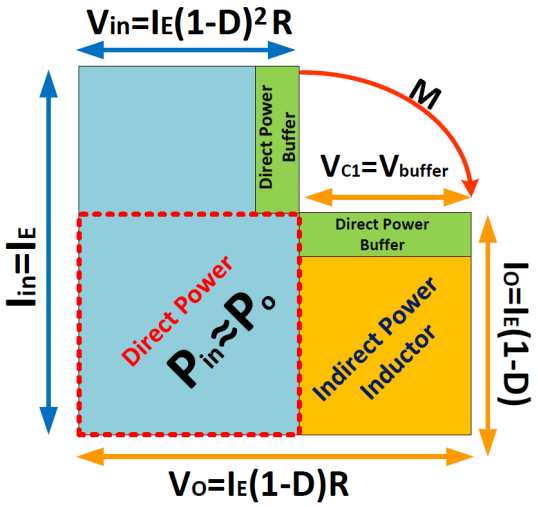

Fig. 5. Modeling of the input/output power area of the Boost with PPP.

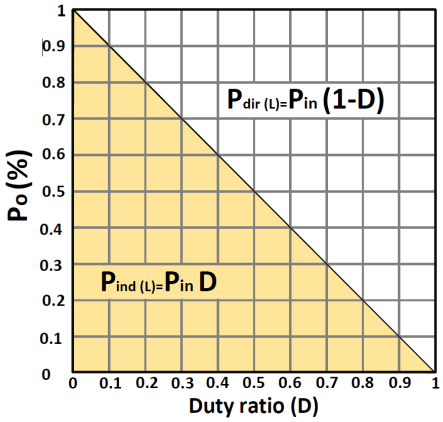

Fig. 6. Power processing analysis of a convetional boost converter.

the inductor. During the ON state, the inductor L is the only element that stores and transfers power without a direct path between the source and the load, as seen in Fig. 2(b). Under this approach, the indirect power in the inductor can be expressed as a function of the product of the applied positive average voltage V_L^+ and the input current I_E, allowing to obtain an expression relating the power to the operating parameters of the converter and its duty ratio. This expression is given by:

$$P_L = V_L^+ \cdot I_E \tag{15}$$

where V_L^+ is the average positive voltage in the interval from t_0 to t_1, which corresponds to the ON state of the converter. Using the operating point voltage values from equations (1-3) the inductor indirect power is defined by:

$$P_{ind_L} = I_E^2 \cdot R \cdot (1-D)^2 \cdot D = P_o \cdot D \tag{16}$$

Fig. 6 shown the relation between the indirect power processed in the inductor with respect to the duty ratio (D).

The direct power in the conventional Boost converter is defined by $P(1-D)$. The power processing in a conventional boost converter, being comprised of only a single energy transfer path, is directly defined by the power processed through its active elements as shown in Equation (17).

$$P_o = P_{ind} + Pdir = P_o D + Po(1-D) \tag{17}$$

B. Analysis of Partial Power Processing in the Boost

The Boost converter with PPP presents a different behavior to the conventional Boost converter, since it incorporates a direct power transfer path between the source and the load. This feature allows reducing the power stress to which the S diode is subjected during its conduction. Since in this case it does not process all the output power as in the conventional topology. In this converter, the output power is distributed in two processing stages: the power transferred directly and the power stored and delivered by the buffer element. This behavior can be described by Equation (18).

$$P_o = P_{Boost} + P_{buffer} \tag{18}$$

The processed direct power by the diode in the converter with PPP is defined by:

$$P_{dir_S} = P_o - P_L - P_{C_1} \tag{19}$$

To obtain the transferred power by the buffer element (C_1), the positive current and its average voltage must be considered as shown in Fig. 8.

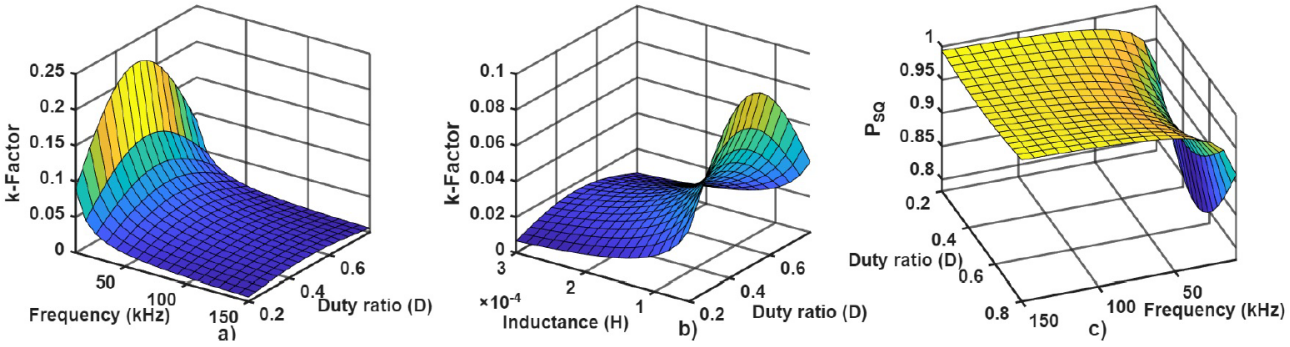

Fig. 7. Area of the k-factor, a) as a function of the duty ratio variation and switching frequency, b) in terms of the inductance variation over a range of 50 to 300 µH and the duty ratio, and c) the power processed over the range of (t_1 to t_2) by the switching stage (P_{SQ}).

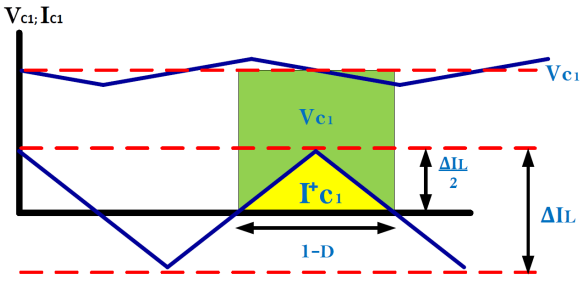

Fig. 8. Current and voltage areas of capacitor C_1.

The positive current in capacitor C_1 is directly related to the inductor current ripple. The capacitor current C_1 is given by :

$$I_{C_1}^{+} = \frac{\Delta_{I_L}}{2} \cdot \frac{(1-D)}{2} \tag{20}$$

substituting the value of the current ripple in the inductor L is obtained:

$$I_{C_1}^{+} = \frac{I_E D(1-D)^2 R}{4Lfs} \cdot (1-D) \tag{21}$$

The indirect power of C_1 is determined by:

$$P_{ind_{C_1}} = P_o \cdot \frac{D^2(1-D)^2 R}{4Lfs} \tag{22}$$

The fraction of partial power processed by the buffer is given by:

$$\kappa = \frac{D^2(1-D)^2 R}{4Lfs} \tag{23}$$

The processed power by the switching stage of the converter is defined by:

$$P_{SQ} = P_o \left(1 - \frac{D^2(1-D)R}{4Lfs}\right) \tag{24}$$

where P_{SQ} is the power processed by the switch and the diode.

C. Model Validation and Analysis

The converter model was verified by considering a photovoltaic panel model ETFE-solar with a voltage of 24 V at the maximum power point and a current of 6.25 A. Table I lists the parameters design used to perform the analysis between the switched model provided by the PowerSim software and an averaged model shown in (12) implemented in Matlab. The k-factor is the fraction of power that is buffered and goes directly to the load. The k-factor in this structure is highly dependent on the current ripple value in the inductor and the switching frequency of the converter. Fig. 7(a) shows the area of the k-factor in terms of variation of duty ratio and switching frequency. Fig. 7(b) shows the area of the k-factor determined by the inductance variation over a range of 50 to 300 µH and the duty ratio and Fig. 7(c) shows the power processed in the interval from (t_1 to t_2) by the switching stage (P_{QS}) considering frequency and duty ratio variations. The power processing through the buffer increases if the current ripple in the inductor is larger. The current ripple depends directly on the inductance value and the operating frequency of the converter.

TABLE I
BOOST CONVERTER PARAMETERS DESIGN WITH PPP

Symbol	*Parameter*	*Value*
I_E	*Input current*	6.25 A
P_o	*Output power*	150 W
I_o	*Output current*	3.125 A
f_s	*Frequency*	50 kHz
L	*Inductor*	110 µHz
ΔI_L	*Current ripple*	2.2 A
C_1, C_2	*Capacitors*	2 µF, 10 µF
ΔV_{C_1}, ΔV_{C_2}	*Voltage ripple*	2.7 V, 3.2 V
D	*Duty ratio*	0.5
Q	*Mosfet*	*C20N60CFD*
S	*Diode*	*TO-220-L*

The Boost converter based on PPP processes more power through the buffer when operating at low frequency. However, it is important to consider that there are applications where the current ripple cannot be too large because it would damage the load, as is the case of battery banks. The areas shown in Fig. 7 allow to select an adequate percentage of the partial processing determined by the k factor considering the

ripple that satisfies the different applications. Fig. 9 shows the capacitor voltage waveforms, inductor current and output current obtained from the switched model and average steady-state model, considering the parameters given in Table I.

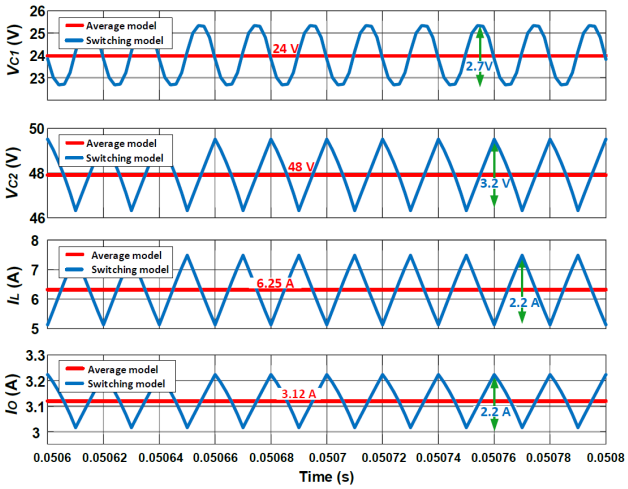

Fig. 9. Voltage/current waveforms obtained from the switched model and average model.

The values of the current/voltage ripples presented in equations (6)-(8) are validated using the parameters of Table I. The current ripple in the inductor plays a fundamental role for the partial power processing, because, it is directly correlated with the current present in the buffer. Using the linear model (13), the frequency response of the transfer function (14) was obtained and compared with the frequency response of the switched model using the PowerSIM simulator. The AC-sweep validation is therefore limited to half the switching frequency ($f_s/2$), which defines a practical upper bound for the averaged small-signal model [22], [23]. Fig. 10 shows the frequency response of the linear model of the Boost converter with PPP.

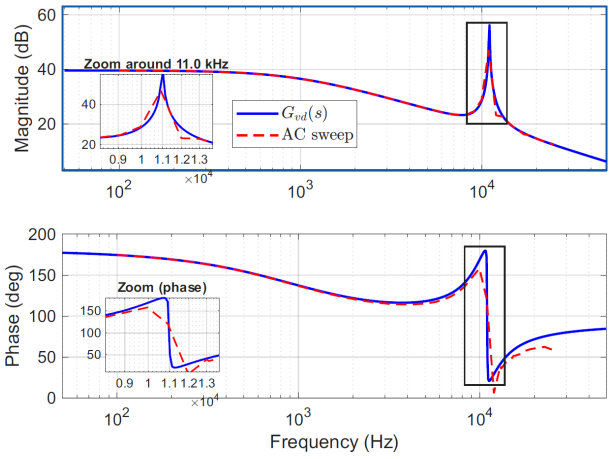

Fig. 10. Frequency response of the linear model of equation (14) and the switched Powersim model.

IV. Experimental Results

The obtained theoretical results are validated by through an experimental prototype considering the parameters in Table I. Fig. 11 shows the prototype of the Boost converter with power processing reduction.

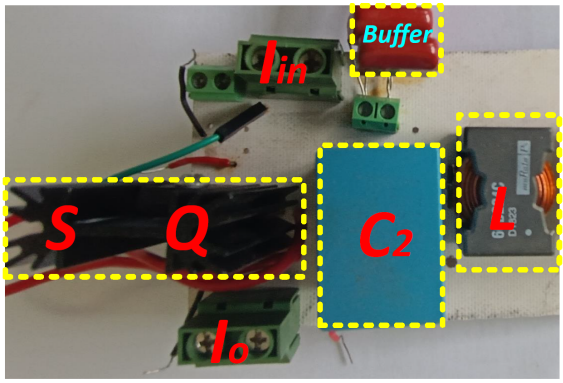

Fig. 11. Prototype of the Boost converter with PPP.

The structure has been modified to compare the basic Boost converter and the Boost converter with PPP under the same operating conditions. Fig. 12 a) shows the current transformation ratio of the Boost converter with PPP in using the Equation (6) obtained by the load balance of the capacitor C_2. The theoretical gain of the converter is 0.5 and the experimental gain obtained is 0.507 Fig. 12 b) shows the waveforms in inductor current L and the capacitor current C_1, where the ripple between the two elements are compared. The current ripple of both elements is Δ_I=2.18 A.

The current in the inductor is 6.12 A. Fig. 12 c) shows the evolution of the current ripple in the capacitor and inductor, showing a direct relationship between both values. In this case, the current ripple in the two elements is 2.18 A, which is a relevant aspect for the analysis of the partial power processing in the converter. Since it confirms the energy balance between the storage and direct power transfer stages. Fig. 13 shows the voltage and current waveforms in the buffer capacitor C_1 for different values of the duty ratio (a) D=0.3, (b) D=0.5 and (c) D=0.7, obtained from the analysis using Volt-Amper area modeling. It is observed that, as the duty ratio increases, the area defined by the product of the positive current and the average voltage in C_1, it increases significantly. However, considering the analysis of Fig. 8, it is identified that the highest power processing in the buffer occurs for $D = 0.5$, since as the duty ratio continues to increase, the direct power processed in the capacitor decrease due to the lower participation of the direct power path. In operation at the rated power of the converter, the current ripple in the buffer capacitor is 2.18 A, with a duty ratio of D=0.5. Under these conditions, the average power processed by the buffer capacitor C_1 is 6.54 W, which represents 4.36% of the converter output power. This percentage corresponds to the portion of power that is transferred indirectly through the buffer, contributing directly to the reduction of the power stress on the active elements and, therefore, this increases the overall efficiency of the converter. One of the advantages is that the small-signal dynamic model represented as a transfer function (14) corresponds to a minimum-phase system, simplifying the controller design process. Based on this advantage, a controller

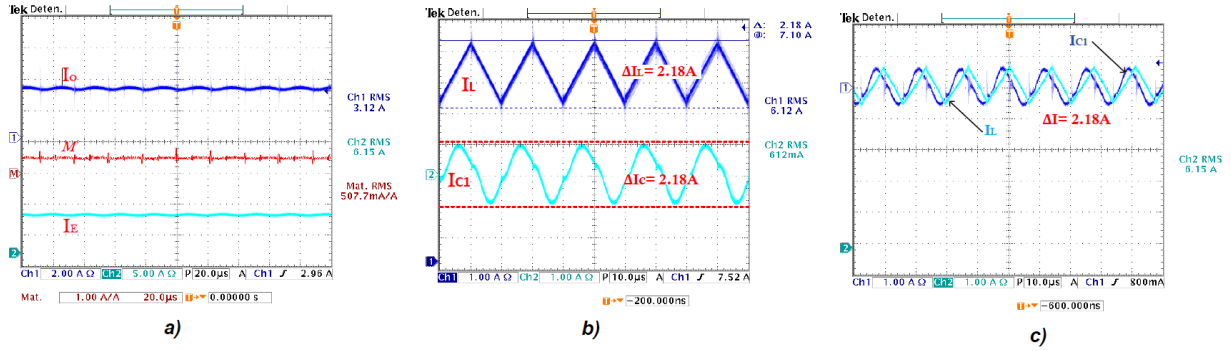

Fig. 12. Experimental waveforms of the PPP Boost converter, a) the transformation ratio in terms of input/output current, b) the waveforms in the inductor current L and the capacitor current C_1, and c) evaluation of the current ripple ratio in the inductor and the buffer.

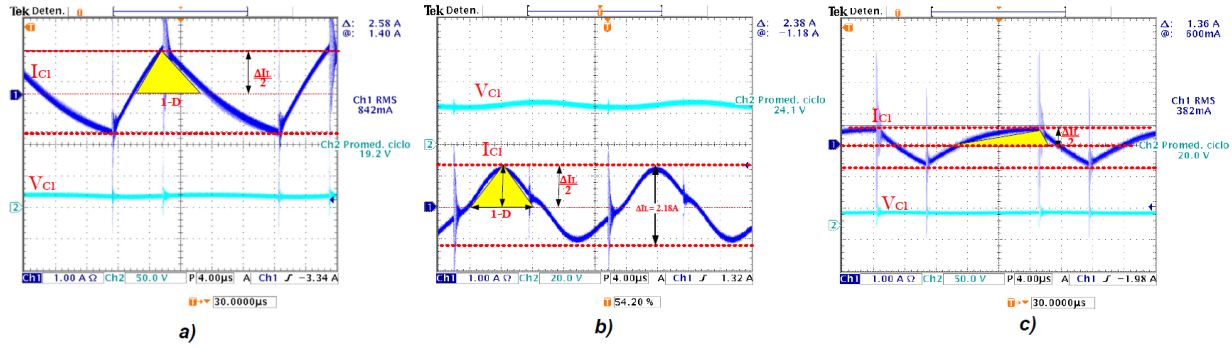

Fig. 13. Analysis by V·A Areas in the buffer during partial power processing with duty ratio variations; a) 0.3, b) 0.5 , and c) 0.7.

was designed to ensure that the output voltage is 48 V. A *PI* controller with feedback on the output voltage is proposed, as shown in Fig. 14.

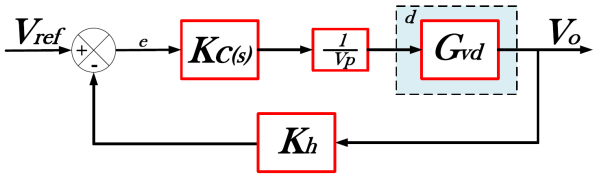

Fig. 14. Block diagram of the proposed control scheme for the Boost converter.

where $K_C(s)$ represents the controller, V_p the peak voltage of the triangular signal, G_{vd} the transfer function, and K_h the voltage sensor gain.

For the controller design, it was used a design method given in [24], [25], the procedure consists in that the controller zero was placed before 10 kHz because that is the frequency where the resonance peak occurs as shown in Fig. 10. The controller gain is tunning so that the zero-crossing frequency is greater than the resonant frequency and minor than half of the switching frequency, the values are presented in equation (25).

$$C(s) = k\frac{s+z}{s} = (12.67)\frac{s+13,700}{s} \qquad (25)$$

Fig. 15 shows the waveforms of the closed-loop converter. Fig. 15 a) shows the output current/voltage waveforms at the nominal power 150 W. Fig 15 b) shows the output voltage of the closed-loop converter under load variations. The load variations were set from 5.30 A to 2.60 A, from 125 W to 255 W, and Fig. 15 shows the time ($t \approx 560\,\mu$s) of stabilization of the output voltage under load changes.

A. Comparison of experimental efficiencies

To validate the experimental results, they are compared with the simulation results obtained theoretically using PowerSim. Table II presents the values obtained in both nominal power scenarios for which the converter was designed, allowing the consistency and accuracy of the proposed design Equations (6-8) to be verified.

TABLE II
COMPARISON OF RESULTS OBTAINED IN SIMULATION (THEORETICAL) AND EXPERIMENTAL

Symbol	*Parameter*	*Theoretical*	*Experimental*
f_s	*Frequency*	50 kHz	50 kHz
D	*Duty ratio*	0.5	0.5
I_E	*Input current*	6.25 A	6.15 A
P_o	*Output power*	150 W	141.84 W
I_o	*Output current*	3.125 A	3.12 A
ΔI_L	*Current ripple*	2.2 A	2.18 A
ΔV_{C_1}	*Voltage ripple*	2.7 V	2.9 V
ΔV_{C_2}	*Voltage ripple*	3.2 V	3.6 V

The efficiency of the converter is related to different conditions, such as component selection, component layout and

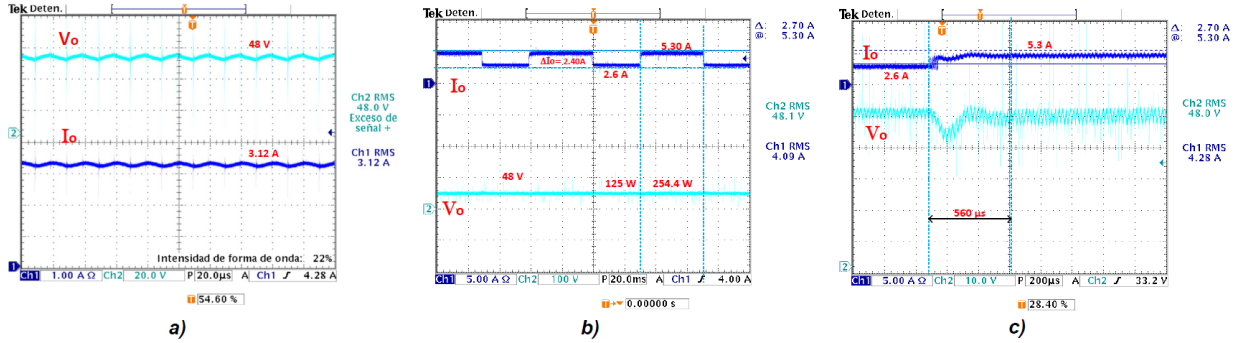

Fig. 15. Experimental waveforms of Boost PPP converter, a) output current/voltage waveforms at nominal power, b) closed-loop voltage and current waveforms of the converter under load change, and c) the stabilization time of the output voltage under load changes.

parasitic resistances of the devices. Fig. 16 shows the efficiency plots of the Boost converter with PPP under conditions open-loop, under conditions closed-loop and the conventional Boost converter considering different power scenarios.

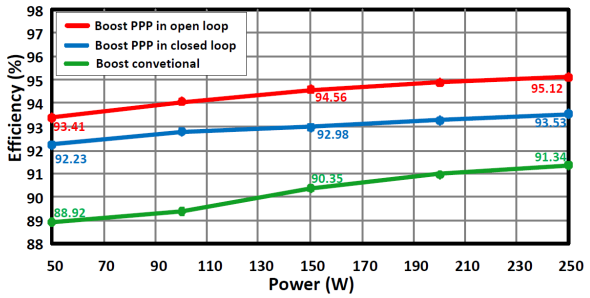

Fig. 16. Experimental plots of the efficiency of the PPP Boost Converter: open-loop (red), closed-loop (blue) and conventional (green).

For the nominal power of 150 W, the converter presents an efficiency of 94.56% in open loop in relation to the input/output power. The maximum power of 250 W that the experimental prototype can be processed reached an efficiency of 95.12%. The converter with PPP has an average efficiency increase of 4% compared to the conventional Boost. This corroborates the theoretical results obtained through VA area modeling. The closed-loop Boost converter with PPP has an average efficiency decrease of 1.5% compared to the open-loop structure. However, it is still more efficient than the open-loop Boost conventional structure. Fig. 17 shows the efficiency of the converter at different switching frequencies, considering the nominal power of 150 W. Experimental frequency variation tests were carried out in open loop in order to obtain a natural response from the system.

The efficiency of the converter shows a decrease with respect to the increase of the switching frequency, because the higher the frequency, the less power is processed in the buffer as shown by the VA area modeling in Fig. 13. However, operating the converter at this frequency will result in inductor current ripple of 5.45 A close to the operation of the converter in Discontinuous Conduction Mode (DCM). In addition to obtaining a large output ripple current which is not suitable for some loads (battery bank, led lighting and water pumps). Fig.

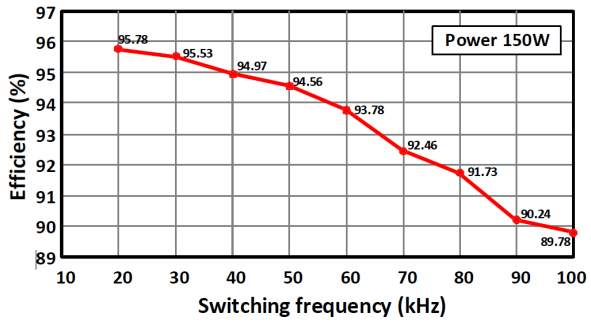

Fig. 17. Experimental efficiency in different switching frequencies.

18 shows the power losses in the different elements present in the converter, these losses are valid for the operation of the converter at a nominal power of 150 W. The highest losses occur in the switching devices, which is due to the importance of the buffer element that transfers a fraction of the input power directly to the output without being processed by the semiconductors.

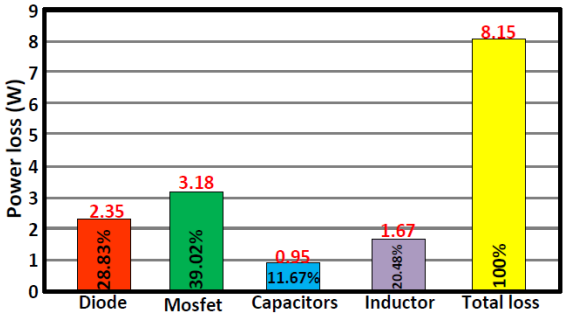

Fig. 18. Power losses in the Boost converter elements with PPP.

V. Conclusions

This paper studies the effects of partial power processing on a boost converter integrated into a PV source. A functional experimental prototype with a nominal power of 150 W was designed and built, where operational and efficiency tests were

carried out. In addition, a comparison was made with the conventional structure, in which the proposed topology exceeded it by 4.21% at a nominal power of 150 W. The experimental results show good agreement with the theoretical analysis, validating both the proposed model and the design methodology used. Fuurter more, the output voltage transfer function with respect to the duty ratio were analyzed, allowing the dynamic behavior of the system to be characterized. The efficiency analysis under different power scenarios demonstrates that the use of partial power processing reduces conversion losses, improving the overall performance of the system, compared to the conventional Boost structure. In particular, the analyzed structure presents a minimum phase characteristic in the output voltage, which simplifies the control design for voltage regulation. The results obtained confirm that the Boost converter with partial power processing is an attractive alternative for renewable energy applications, such as photovoltaic systems, DC microgrids, and energy storage systems, due to its high efficiency, lower voltage stress on semiconductor devices, high power density, and continuous input current. Future work should expand the analysis to higher power levels, evaluate the converter's behavior under dynamic irradiance and load conditions, and explore advanced control strategies, including their integration with maximum power point tracking (MPPT) algorithms, to broaden the scope and applicability of this topology in real PV systems.

ACKNOWLEDGMENTS

The authors thank Secretaría de Ciencia, Humanidades, Tecnología e Innovación (SECIHTI).

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Iván Alfonso Reyes Portillo received the degree of Electromechanical Engineer from the Instituto Tecnológico Superior de San Andrés Tuxtla, San Andrés Tuxtla, Veracruz, México in 2016 and the degree of Master of Science in Electronic Engineering from the Centro Nacional de Investigacion Y Desarrollo Tecnológico, Cuernavaca, Morelos, México in 2019. Obtained a Ph.D. in Electrical Engineering from the Universidad Autónoma de San Luis Potosí, San Luis Potosí, México, in 2024. He is currently a professor at the Universidad Politécnica de San Luis Potosí, in the Academy of Industrial Systems and Technologies Engineering, and an associate researcher at the Universidad Autónoma de Zacatecas. His main areas of interest are DC/DC converters, redundant power processing converters, energy storage, and renewable energies.

Saúl Rolando Mendez-Elizondo received the B.S. degree in Biomedical Engineering in 2017 and the M.S. degree in Electrical Engineering in 2020 from the Universidad Autónoma de San Luis Potosí, San Luis Potosí, Mexico. He is currently pursuing the Ph.D. degree in Electrical Engineering at the Universidad Autónoma de San Luis Potosí. His research interests include DC/DC converters, stability analysis of DC microgrids, energy storage systems, and control design for power electronic systems.

Jorge Alberto Morales-Saldaña received the degree of Electrical Engineer and the degrees of Master´s and Ph.D. degrees in Electrical Engineering from the Universidad Autónoma de San Luis Potosi, San Luis Potosí, Mexico, in 1995, 1997 and 1999, respectively. He currently works at the Faculty of Engineering of the same University as a Research Professor. His main areas of interest are the development of high-efficiency switching converters, DC/DC conversion systems and control engineering applied to power electronic systems.

Jorge Ulises Muñoz-Minjares received his B.S. degree in Communications and Electronics Engineering from the Universidad Autónoma de Zacatecas in 2010. Subsequently, he obtained his M.S. and Ph.D. degrees in Electrical Engineering from DICIS, Universidad de Guanajuato, in 2012 and 2018, respectively. He is currently a research professor at the Universidad Autónoma de Zacatecas in Zacatecas, Mexico. His research interests include digital signal and image processing, optimal filtering, and probability, statistics and design of power electronics systems.

Claudia Angélica Rivera Romero received her Master's degree in Electrical Engineering from the Universidad de Guanajuato in 2012. She obtained her PhD degree in Electrical Engineering from Universidad Autónoma de San Luis Potosí in 2021. She is currently an associate researcher at the Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), México. Her areas of interest are digital image processing, machine learning and power electronics.

Dora Luz Castro-López received the B.S. degree in Mechanical Engineering from the Universidad Autónoma de Zacatecas (UAZ), Zacatecas, in 2011, and the Master's and Ph.D. degrees in Mechanical Engineering from the Universidad Autónoma de San Luis Potosí (UASLP), San Luis Potosí, México, in 2014 and 2021, respectively. She is currently a professor at Universidad Politécnica de San Luis Potosí in the Academy of Engineering in Systems and Industrial Technologies. His research interests focus on heat transfer in biomedical systems and fluid mechanics applications. In addition, she is interested in the study of heat transfer and thermal design of power electronics systems.