Comparison of Two Harmonic Load-Pull Systems Using Frequency-Domain and Time-Domain Measurements for Evaluating GaN Transistor Output Power and Efficiency

Edgar Hernández-Limón, *Member, IEEE*, Daniel Alonso-Tejera, *Member, IEEE*, J. Apolinar Reynoso-Hernández, *Member, IEEE*, María del Carmen Maya-Sánchez, *Member, IEEE*, José Raúl Loo-Yau, *Member, IEEE*, Manuel Alejandro Pulido-Gaytan, *Member, IEEE*, and Jaime Sánchez-García, *Member, IEEE*

***Abstract*— Two active real-time harmonic load-pull systems were developed: one operating in the time domain (TD-AHLP) and the other one in the frequency domain (FD-AHLP). The main distinction between them lies in their receivers: the first utilizes a four-channel oscilloscope, while the second uses a vector network analyzer. Measurements of output power and drain efficiency were performed using both load-pull systems on a MACOM CGH40010F GaN-HEMT transistor, biased as a Class-B power amplifier (V_{GS} = -2.92 V, V_{DS} = 28 V, I_{DS} = 200 mA), at a fundamental frequency of 1 GHz. The performance of both systems was compared to evaluate the harmonic loads up to their third harmonic, output power, drain efficiency, and power gain of a Harmonic Tuned Power Amplifier (HTPA). Results demonstrate high consistency between the two systems, with mean relative deviations below 3% for both output power and drain efficiency. Both systems identify specific second-harmonic impedance regions along the periphery of the Smith chart where performance metrics remain nearly constant and largely independent of the second-harmonic reactance.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/10302

***Index Terms*— Drain efficiency, GaN, Harmonic load-pull, Output power, Power amplifier.**

I. Introduction

LOAD-PULL techniques are widely used in the design of power amplifiers to determine the impedance at which a transistor delivers maximum output power to the load [1] and to validate nonlinear transistor models [2]. From a measurement perspective, a load-pull system can be implemented in three main ways: using a passive load [3], an active load [4], or a combination of these [5]. Load-pull can also be performed through simulation using CAD tools with the aid of nonlinear transistor models.

Active load-pull was first introduced by Takayama [6]-[7], where a feedback signal is injected into the device under test (DUT) through an active load consisting of a linear power amplifier and a vector signal generator to compensate for losses between the DUT and the load-pull system. Active load-pull systems enable the synthesis of arbitrary impedances, both inside and outside the Smith chart. Although more expensive, active load-pull systems mitigate the impedance synthesis limitations typically encountered in passive load-pull systems, in which impedances near the periphery of the Smith chart cannot be synthesized due to tuner losses.

Both passive and active load-pull systems have been implemented using vector network analyzers (VNAs) [8]-[10] or sampling oscilloscopes [11]-[12]. For example, Mokhti *et al.* [13] compared the performance of a passive load-pull system with a VNA receiver and an active harmonic load-pull system using a sampling oscilloscope. Similarly, Clymore *et al.* [14] compared active and passive load-pull systems to investigate the performance of GaN HEMTs. However, in both studies, each comparison was performed between different architectures of the load-pull systems. Recently, implementations of load-pull systems based on integrated RF platforms, including RFSoC/FPGA-based measurement setups, have also been proposed [15].

To the authors' knowledge, no previous work has reported a direct comparison of active real-time harmonic load-pull systems in which the test-bench configuration is preserved while only the receivers are swapped, using a VNA in one case and a sampling oscilloscope in the other. For this reason, this paper evaluates the performance of two active real-time harmonic load-pull systems—one operating in the frequency domain (with VNA receivers) and the other in the time domain (with sampling oscilloscope receivers)—by comparing their ability to determine the optimal load, output power, and

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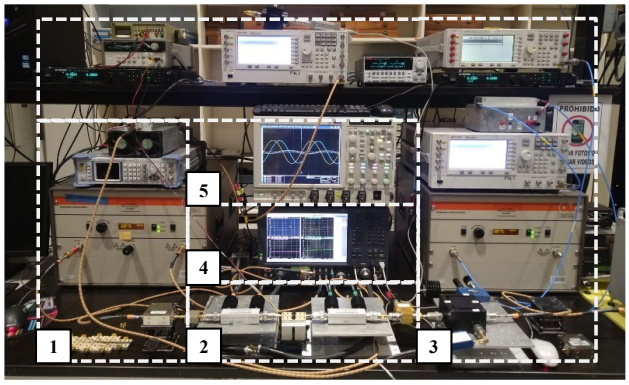
Edgar Hernández-Limón, D. Alonso-Tejera, J. Apolinar Reynoso-Hernández, M. D. C. Maya-Sánchez, M. A. Pulido-Gaytan, and J. Sánchez-García are with the Department of Electronics and Telecommunications, Center for Scientific Research and Higher Education at Ensenada, Ensenada, Mexico (e-mails: edgarhl@cicese.edu.mx, dalonsotd@cicese.edu.mx, apolinar@cicese.mx, mcmaya@cicese.mx, manuel.pulidogaytan@skyworksinc.com, and jasan@cicese.mx).

J. R. Loo-Yau is with the Center for Research and Advanced Studies of the National Polytechnic Institute, Guadalajara Campus, Guadalajara, Mexico (e-mail: raul.loo@cinvestav.mx).

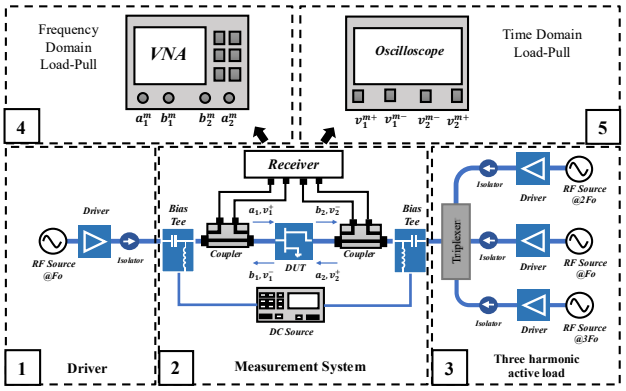
drain efficiency, as well as to study the influence of the second-harmonic reactance on the output power and efficiency of Harmonic-Tuned Power Amplifiers (HTPAs). The control of harmonic load impedances has been shown to improve amplifier efficiency through waveform engineering [16]-[18].

II. Description of the Load-Pull System

Fig. 1 provides an overview of the proposed active harmonic load-pull systems. The setup comprises three main blocks: the driver, the three-harmonic active load, and the measurement system.



(a)



(b)

Fig. 1. Active harmonic load-pull test benches with VNA-based and oscilloscope-based receivers: (a) photograph of the experimental setup and (b) block diagram of the measurement system. The numbered labels indicate the main subsystems of the test bench: (1) driver amplifier, (2) measurement system, (3) three-harmonic active load network, (4) VNA receivers, and (5) oscilloscope receivers.

A. Driver

The driver block consists of a vector signal generator (SMB100A), a high-power linear amplifier (AR20/20S1G18) used as the driver amplifier to excite the DUT, and an isolator.

B. Three-Harmonic Active Load

The three-harmonic active load block includes a triplexer operating at the fundamental frequency band (0.8–1 GHz). Its input is fed by three vector signal generators (E8267D) and three wideband high-power linear amplifiers, each connected to an isolator at its output. These vector signal generators synthesize the fundamental frequency as well as the second and third harmonics required for harmonic load-pull operation.

C. Measurement System

The measurement system, from left to right, consists of a low-power bias tee for biasing the transistor's gate while allowing to inject the continuous-wave (CW) input signal, a bidirectional coupler (30 dB coupling factor) at the DUT input to sense the incident (a_1 or v_1^+) and reflected (b_1 or v_1^-) waves, a test fixture and a second bidirectional coupler at the DUT output is used to sense the incident (b_2 or v_2^-) and reflected (a_2 or v_2^+) waves, and a wideband high-power bias tee for biasing the drain with the DC supply voltage (2602A) and to inject the harmonic signals generated by the active load block.

The measurement system integrates either four-port PNA-X VNA receivers (N5245B) to implement the Frequency Domain Active Load Pull (FD-AHLP) system, which captures incident and reflected wave data in the frequency domain, or four-channel sampling oscilloscope receivers (DPO 70404C) for the Time Domain Active Load Pull (TD-AHLP) system, which captures voltage waveforms and allows the reconstruction of current waveforms in the time domain. A summary of the key characteristics of both receiver types is presented in Table I.

TABLE I
KEY FEATURES OF VNA AND OSCILLOSCOPE RECEIVERS

Parameter / Feature	Keysight PNA-X N5245B (VNA)	Tektronix MSO70404C (Oscilloscope)
Primary measurement domain	Frequency domain (vector measurement: magnitude and phase)	Time domain (waveform)
Receiver architecture	Coherent heterodyne: RF signal down-converted to baseband (I/Q) using mixers and a synchronized LO	Real-time sampling: direct digitization of the RF signal using high-speed ADCs
Signal digitized by the ADC	Baseband I/Q components (DC–kHz range)	Full RF waveform (up to ~4 GHz)
Frequency range / bandwidth	10 MHz – 50 GHz (frequency-swept measurement)	Determined by the 4 GHz analog bandwidth (–3 dB) and sampling rate (25 GS/s)
Impact on dynamic range	Very high; typical dynamic range >120 dB for vector measurements with narrow IF bandwidth	Limited; effective dynamic range ≈ 38–44 dB (8-bit ADC, ENOB ≈ 6–7 bits at maximum bandwidth)
Sensitivity / noise floor	Very low noise floor (typically < –110 dBm, dependent on IFBW and averaging)	Noise determined by ENOB, V/div scale, and bandwidth; typically

III. System Calibration

The load-pull system enables the characterization of a power transistor under large-signal conditions at the device reference planes for different load impedances. The key transistor parameters determined by the load-pull method include input power (P_{in}), output power (P_{out}), drain efficiency (η_d), power gain (G_p) and optimal output load (Z_{opt}). Since all these parameters must be measured at the device reference planes under large-signal condition, proper calibration is essential. Calibration mitigates the non-idealities of the bidirectional couplers, test fixtures, VNA receivers (or sampling oscilloscope receivers), and the coaxial cables connecting the different elements of the measurement system. The calibration process consists of two main steps: relative calibration and power calibration. For systems that also perform time-domain waveform measurements,

an additional phase calibration is required.

A. Relative Calibration

Relative calibration uses an error model to represent the measurement system and a calibration technique to extract the error terms. In this work, the 8-term error model is adopted to describe the system's non-ideal behavior. The error terms are determined using the Thru-Reflect-Line (TRL) calibration technique reported in [19]-[21]. When the measurement system uses a sampling oscilloscope, the TRL is implemented using the ABCD-parameter matrix formalism, since the oscilloscope measures voltages at its four channels [19]-[20]. When the system utilizes a VNA, the TRL is implemented using the T-parameter matrix formalism, as the VNA measures incident and reflected power waves at its receivers [19],[21]. The test fixture and the calibration structures used for this step are illustrated in Fig. 2.

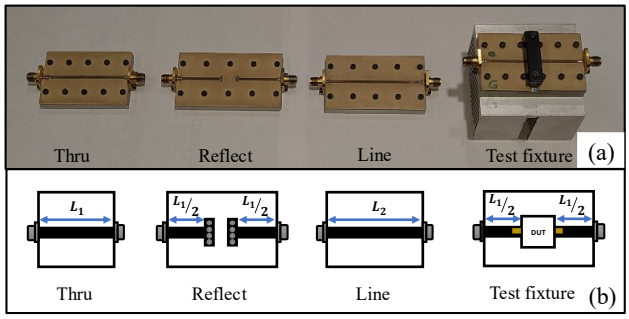


Fig. 2. TRL calibration standards: (a) photograph of the calibration standards and (b) schematic diagram of the TRL standards used in the measurement setup.

B. Power Calibration

Power calibration is performed by replacing the DUT in the test fixture with a thru connection and assuming that the bidirectional coupler at the output of the measurement system is reciprocal [22]. This assumption was experimentally validated by characterizing the bidirectional coupler's S-parameters with a calibrated VNA from 10 MHz to 4 GHz. As shown in Table II, the magnitude difference between S_{21} and S_{12} is minimal across the entire frequency range, with an average difference of 0.0296 dB and a maximum deviation of 0.1054 dB. These quantitative results confirm the reciprocal assumption used in the power calibration process.

TABLE II
RECIPROCITY CHARACTERIZATION OF THE BIDIRECTIONAL COUPLER

Frequency Range (GHz)	Avg. $\|S_{21}\|$ (dB)	Avg. $\|S_{12}\|$ (dB)	Avg. $\Delta\|S\|$ (dB)	Max. $\Delta\|S\|$ (dB)
0.01 – 4	–0.2743	–0.2457	0.0296	0.1054

This coupler is modeled as a one-port network with four error terms as reported in [22]-[23]. By using the Short-Open-Load (SOL) one-port calibration technique along with a power meter, the four error terms can be determined. Under the reciprocity assumption, this procedure provides the magnitudes of the transmission error term at port one and the corresponding error term at port two. These values enable the accurate computation of the input and output power at the DUT reference planes for any predetermined load. Therefore, after power calibration, the measurement system allows determining the key performance parameters and the optimal output load for different bias points at the DUT reference plane.

C. Phase Calibration

Phase calibration is necessary when time-domain waveform measurements are required in addition to harmonic load-pull extraction. This step follows a procedure similar to power calibration, using the same SOL standards but requiring an additional phase calibration standard. The phase standard may be a comb generator or an oscilloscope, as proposed in [24]. In this work, the sampling oscilloscope itself is used as the phase calibration standard.

The absolute phase reference is established by designating one acquisition channel as the phase standard, to which all other channels are referenced during calibration. This process, integrated within the 8-term error model, effectively corrects systematic phase errors and inter-channel skew. The consistency of this reference is experimentally validated by applying a common signal to all channels, ensuring phase normalization across all measured wave quantities.

D. Device Under Test and Measurement Settings

The DUT in this study is a 10 W CGH40010F GaN HEMT, biased in Class-B with a drain-source voltage of V_{DS} = 28 V and a gate-source voltage of V_{GS} = –2.92 V, resulting in a quiescent drain current of I_{DS} = 200 mA. After calibration, the measurement reference plane was set at the DUT terminals, as illustrated in Fig. 3, over a frequency band from 0.9 GHz to 4 GHz. In both load-pull systems, the DUT was driven with a single-tone CW signal at a fundamental frequency, f_0 = 1 GHz.

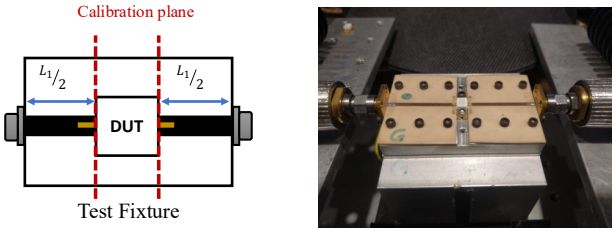


Fig. 3. Test fixture used for transistor characterization in the load-pull measurement system: (a) schematic diagram and (b) photograph of the fabricated fixture. The transmission line sections labeled $L_1/2$ represent half of the Thru standard used in the TRL calibration, placing the calibration reference planes at the transistor terminals.

IV. EXPERIMENTAL RESULTS

A. Load-Pull Contours

With the systems calibrated and the DUT biased under identical conditions in both setups, the device was first characterized using load-pull measurements to determine the optimal impedances for maximum power and maximum

efficiency, enabling a direct comparison of the receivers' performance.

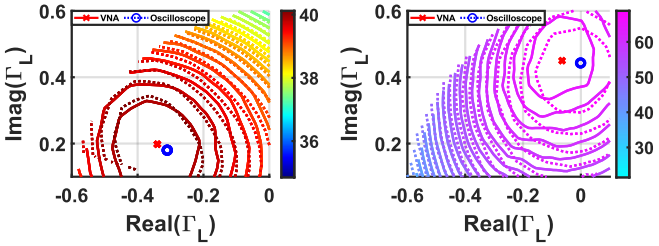


Fig. 4. Comparison of load-pull contours and optimal load impedances for: (a) maximum output power and (b) maximum drain efficiency. The contours illustrate the variation of the measured performance over the load impedance plane, while the markers indicate the corresponding optimal load points. Bias conditions: f_0 = 1 GHz, V_{GS} = -2.92 V, V_{DS} = 28 V, I_{DS} = 200 mA.

Fig. 4 shows the load-pull contours for maximum power and maximum efficiency obtained with both systems, while Table III summarizes the key performance metrics. As observed, the drain efficiencies measured with TD-AHLP are slightly higher than those with FD-AHLP. This difference can be attributed to slight variations in the optimal impedances extracted by each system. Notice that the remaining parameters, such as input power and output power, exhibit only minor discrepancies. Overall, the results indicate that both approaches provide consistent characterization of the DUT.

TABLE III
EXPERIMENTAL RESULTS COMPARISON UNDER OPTIMAL LOAD IMPEDANCE

Parameter	TD-AHLP	FD-AHLP	TD-AHLP	FD-AHLP
	Max Power		Max Efficiency	
Z_{opt} (Ω)	24.98+10.22i	22.85+10.74i	33.60+37.02i	29.4+33.89i
Γ_{opt}	-0.31 + 0.18i	-0.34 + 0.2i	-0.001+0.443i	-0.065+0.45i
P_{in} (dBm)	14.13	14.01	14.41	14.77
P_{out} (dBm)	39.98	40.03	38.47	38.92
η_d (%)	56.71	54.51	70.47	67.73

B. Output power, Drain efficiency, and Power Gain versus Input Power

Fig. 5 shows the output power, drain efficiency, and power gain as a function of input power for maximal power and maximal efficiency conditions. For input power levels below 6 dBm, it was not possible to reliably compare the performance metrics from both systems. This limitation is primarily due to the oscilloscope's lower dynamic range and higher noise floor compared to the VNA receivers, as summarized in Table I. Specifically, the oscilloscope's 8-bit vertical resolution and its reduced effective number of bits (ENOB) result in a higher noise floor, which obscures the low-level signals at these input power ranges. This degrades the accuracy of the wave acquisition required to calculate the performance metrics, whereas the VNA maintains high precision due to its superior dynamic range.

For input power greater than 6 dBm, both systems are comparable, with no significant differences observed in output power when the transistor is loaded for maximal power, as reported by the relative errors (ΔP_{out}) shown in Fig. 5(a). However, small differences in output power are observed when the transistor is loaded for maximum efficiency and the input power is below 14 dBm, as shown in Fig. 5(b).

For drain efficiency and input power greater than 14 dBm, it is observed that in this region, the drain efficiency measured with TD-AHLP is higher than that measured with FD-AHLP, regardless of whether the DUT is loaded for maximal power or maximal efficiency, as shown by the relative drain efficiency error ($\Delta\eta_d$) in Figs. 5(a) and 5(b). In this operating region, the maximum relative drain efficiency error is approximately 5%. Regarding the power gain, once the input power exceeds 14 dBm, both load-pull systems yield comparable results, and no significant differences are observed.

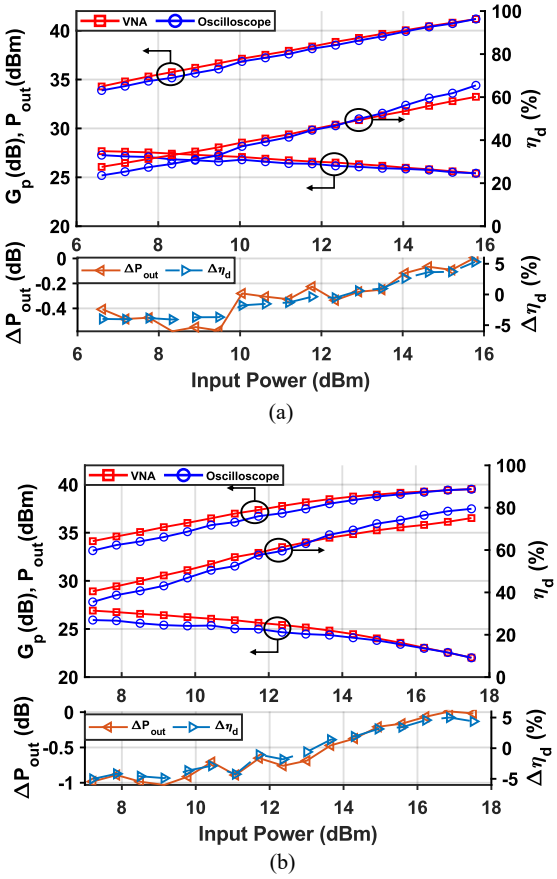


Fig. 5. Comparison of output power, drain efficiency, and power gain for load-pull measurements under the bias conditions (f_0 = 1 GHz, V_{GS} = -2.92 V, V_{DS} = 28 V, I_{DS} = 200 mA): (a) at the optimal load for maximum output power, and (b) at the optimal load for maximum efficiency.

C. Three Harmonic Power Amplifier

In this section, the performance of a power amplifier under load conditions up to the third harmonic, with the fundamental frequency optimized for both maximum output power and maximum efficiency, was evaluated using both TD-AHLP and FD-AHLP systems. Fig. 6(a) shows the impedances at the fundamental, second, and third harmonics, with the fundamental set to the optimum for maximum output power ($Z_{opt,P}$), Table III, the third harmonic open-circuited (Z_{3F0}), and the second harmonic (Z_{2F0}) varied along the edge of the Smith chart. Figs. 6(b) and 6(c) depict the output power and drain efficiency, respectively, as functions of the second-harmonic reactance, X_2.

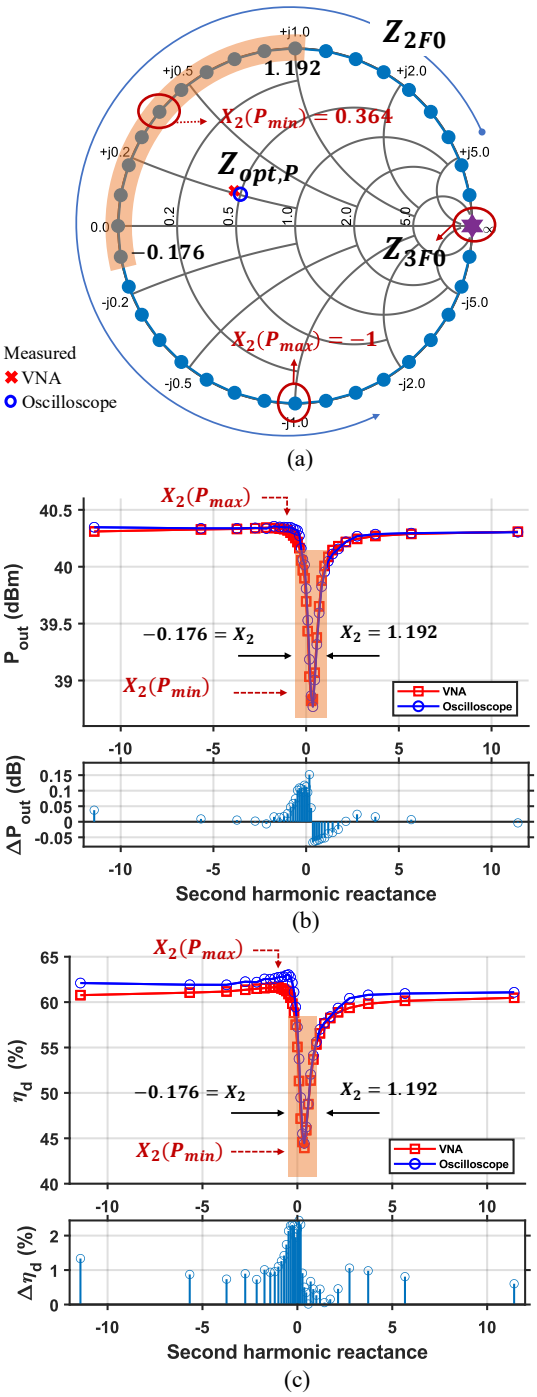


Fig. 6. Comparison of measured TD-AHLP and FD-AHLP results with the load optimized for maximum output power at the fundamental frequency. (a) Smith chart showing the optimal load impedance at the fundamental frequency, the sweep of the second-harmonic reactance, and the third-harmonic open-circuit condition. (b) Output power versus second-harmonic reactance. (c) Drain efficiency versus second-harmonic reactance. Bias conditions: f_0 = 1 GHz, V_{GS} = -2.92 V, V_{DS} = 28 V, I_{DS} = 200 mA.

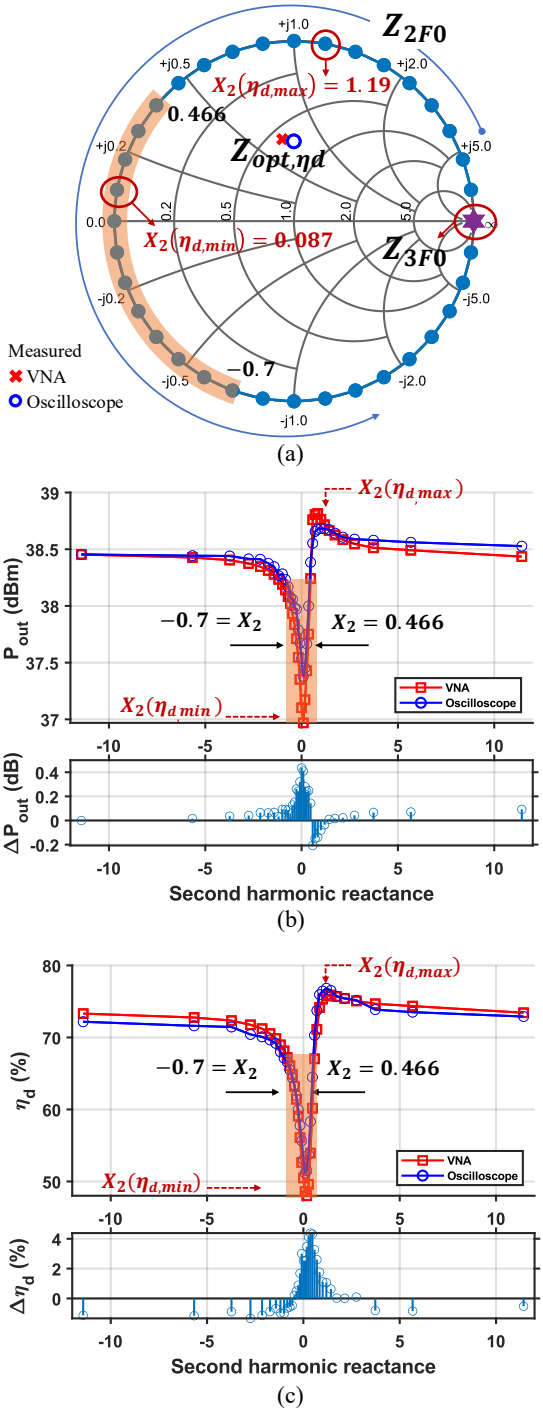


Fig. 7. Comparison of measured TD-AHLP and FD-AHLP results with the load optimized for maximum drain efficiency at the fundamental frequency. (a) Smith chart showing the optimal load impedance at the fundamental frequency, the sweep of the second-harmonic reactance, and the third-harmonic open-circuit condition. (b) Output power versus second-harmonic reactance. (c) Drain efficiency versus second-harmonic reactance. Bias conditions: f_0 = 1 GHz, V_{GS} = −2.92 V, V_{DS} = 28 V, I_{DS} = 200 mA.

As indicated by the shaded region in the plots, both power and efficiency decrease significantly near the short-circuit condition (zero reactance). But out of these points, the power and efficiency are nearly independent of the reactance value of the second harmonic. This behavior was published in [25], where CAD simulation was used to perform a harmonic load pull, investigating the power and efficiency dependence of the second and third harmonics in the HTPA.

To the best of the author's knowledge, a comprehensive investigation based on measurements of the power and efficiency of harmonic power amplifiers has not been previously reported. It is worth noting that maximal power is achieved when the reactance of the second harmonic is negative. As for the drain efficiency, measured under fundamental load conditions corresponding to maximum power, it is observed that the maximum value of the drain efficiency also occurs at negative reactance values.

On the other hand, the transistor output was loaded for maximal drain efficiency ($Z_{opt,\eta d}$), as specified in Table III, at the fundamental frequency. The third harmonic was kept open-circuited, while the second-harmonic reactance was varied along the edge of the Smith chart, maintaining the same bias conditions as in the maximal power case, as shown in Fig. 7(a). Figs. 7(b) and 7(c) show the output power and drain efficiency as functions of the second-harmonic reactance, X_2. From these plots, it is observed that both maximal power and maximal drain efficiency occur at positive reactance values. In contrast, both performance metrics exhibit a minimum near zero reactance.

A comparison between the TD-AHLP and FD-AHLP measurement results reveals a high level of consistency across the entire reactance sweep. This is quantitatively validated by the relative error analysis summarized in Table IV, which reports mean relative deviations below approximately 3% for both output power and drain efficiency. As illustrated in Figs. 6 and 7, larger relative deviations occur for second-harmonic reactance values approaching the short-circuit condition. In this region, where the DUT performance significantly decays and the synthesized impedances are inherently small, the output metrics exhibit a pronounced sensitivity to minor variations in the harmonic load. This high sensitivity suggests that more stringent stability in the load synthesis and measurement control is required to minimize discrepancies in such extreme impedance regions.

TABLE IV
QUANTITATIVE SUMMARY OF RELATIVE ERRORS BETWEEN MEASUREMENT SYSTEMS

Operating Condition	Metric	Mean Relative Error (%)	Maximum Relative Error (%)	Minimum Relative Error (%)
Maximum Output Power Optimum	Output Power	1.16	3.55	0.03
	Drain Efficiency	1.93	4.92	0.03
Maximum Efficiency Optimum	Output Power	2.98	10.54	0.01
	Drain Efficiency	2.45	8.28	0.02

V. CONCLUSION

The time- and frequency-domain load-pull systems were compared to evaluate the output power, drain efficiency, and power gain of a three-harmonic tuned power amplifier. The two architectures demonstrate high consistency, with mean relative deviations below 3% for both output power and drain efficiency.

Beyond the system comparison, the experimental results reveal a performance collapse as the second-harmonic reactance, varied along the periphery of the Smith chart, approaches the short-circuit point. In contrast, other specific regions on this periphery exhibit nearly constant performance.

Furthermore, a shift in the optimal second-harmonic region was identified, with negative reactance values for maximum output power and positive values for maximum drain efficiency. These observed behaviors align with physical phenomena reported in the literature—often characterized through simulations—which reinforces the reliability of the developed measurement setups.

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Edgar Hernández-Limón (Member, IEEE) received the B.Sc. degree in electronics sciences from the Benemérita Universidad Autónoma de Puebla, Puebla, Mexico, in 2016, and the M.Sc. degree in electronics and telecommunications from the Center for Scientific Research and Higher Education of Ensenada (CICESE), Baja California, Mexico, in 2020. He is currently pursuing the Ph.D. degree in electronics and telecommunications with a specialization in high frequencies at CICESE. His research interests include RF power amplifiers, load-pull characterization, and microwave circuits.

Daniel Alonso-Tejera (Member, IEEE) received the B.Sc. degree in Telecommunications and Electronics Engineering from the Central University "Marta Abreu" of Las Villas in 2020. He was an Assistant Professor at the same university, where he taught antennas and radio electronics. He earned the M.Sc. degree in Electronics and Telecommunications with a focus on high frequencies from CICESE, Ensenada, Mexico, in 2024, where he is currently pursuing a Ph.D. His research interests include RF and microwave circuit design, Load-Pull techniques, waveform engineering, and power amplifiers.

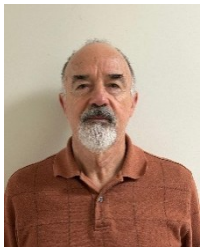
J. Apolinar Reynoso-Hernández (Member, IEEE) received the Electronics and Telecommunications Engineering degree from ESIME-IPN, Mexico, in 1984, the M.Sc. degree in Solid State Physics from CINVESTAV-IPN in 1985, and the D.E.A. and Ph.D. degrees in Electronics from LAAS-CNRS, Université Paul Sabatier, Toulouse, France, in 1987 and 1989, respectively. Since 1990, he has been a Professor at the Electronics and Telecommunications Department at CICESE,

Ensenada, Mexico. His research interests include high-frequency on-wafer measurements, device modeling, and nonlinear characterization. He is main author of the book titled *Principles and Applications of Vector Network Analyzer Calibration Techniques* (River Publishers, 2024). He has led CICESE's Microwave Group to receive five Best Interactive Forum Paper Awards. He has served as TPC and Workshop Organizer for ARFTG and is a regular reviewer for several IEEE journals. He is Associate Editor of IEEE transactions On Microwave Theory and Techniques (2022-2025).

María del Carmen Maya-Sánchez (Member, IEEE) received the B.S. degree in Communications and Electronic Engineering from ESIME-IPN, Mexico City, in 1995, the M.S. degree in Electronics and Telecommunications from CICESE, Ensenada, Mexico, in 1997, and the Ph.D. degree from the Universitat Politècnica de Catalunya, Barcelona, Spain, in 2003. She was a faculty member at the Department of Signal Theory and Communications, Universitat Politècnica de Catalunya, from 2003 to 2004. Since 2004, she has been a Researcher in the Department of Electronics and Telecommunications at CICESE, working with the High Frequency Group. Her research interests include MESFET, HEMT, and HBT device modeling, on-wafer noise measurement techniques, and the analysis, design, and characterization of microstrip and coplanar transmission lines.

José Raúl Loo-Yau (Senior Member, IEEE) was born in Panamá City, Panamá. He received the degree in Electronic and Communication Engineering from the Universidad Autónoma de Guadalajara in 1998, and the M.Sc. and D.Sc. degrees in Electronics and Telecommunications with a focus on high-frequency electronics from CICESE, Ensenada, Mexico, in 2000 and 2006, respectively. Since 2007, he has been a Research Professor with the Electronic Design Group at Cinvestav-GDL. His research interests include linear and nonlinear modeling of microwave transistors, high-efficiency power amplifiers, digital predistortion, and RF active circuit design.

Manuel Alejandro Pulido-Gaytan (Member, IEEE) was born in Zacatecas, México, on December 4, 1986. He received the B.S. degree in electronic engineering from the State University of Zacatecas (UAZ), Zacatecas, México, in 2010, and the M.S. and Ph.D. degrees in high-frequency electronics from the Center for Scientific Research and Higher Education at Ensenada (CICESE), Ensenada, México, in 2012 and 2016, respectively. From 2016 to 2020, he was with the Department of Applied Physics at CICESE. He is Co-author of the book titled *Principles and Applications of Vector Network Analyzer Calibration Techniques* (River Publishers, 2024). He is currently a Principal RF Device Modeling Engineer with Skyworks Solutions, Inc. His main research interests include the measurement, characterization, and modeling of microwave and RF devices.



Jaime Sánchez-García (Member, IEEE) received the Ph.D. degree in Electrical Engineering with a specialization in communications from The George Washington University, USA, in 2001. He holds an M.Sc. in Electronics and Telecommunications from CICESE (1979), and a degree in Communications and Electronics Engineering from ESIME-IPN (1976). He is a Senior Researcher ("C" level) at the Department of Electronics and Telecommunications, CICESE, where he conducts research and teaching in wireless communications. His research interests include wireless networks, MIMO-OFDM, space-time-frequency coding, and physical-layer techniques for 4G systems. He received 1st place in the 3rd Annual Ericsson Telecommunications Award (1988) and has completed research stays at Telefónica de España, the University of Arizona, and the University of Texas at Austin.