A Switched-Inductor-Capacitor Network-Based Quadratic High-Gain DC-DC Converter

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***Abstract*—This article introduces a quadratic high step-up DC–DC converter that incorporates a switched inductor–capacitor network. The proposed converter is intended to align the voltage at the output terminals of the converter with the DC link voltage suitable for renewable energy sources such as solar photovoltaic systems and fuel cells. The converter provides a superior voltage conversion ratio over an extensive range of duty cycles. To validate its functionality, the converter is assessed under both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The influence of parasitic components is taken into account to precisely evaluate the DC voltage gain. The circuit's performance is evaluated against existing topologies concerning the voltage conversion ratio, voltage stresses encountered by the switches, and maximum voltage gain. A 300 W hardware prototype was constructed and evaluated. The proposed converter, operating with a 24 V input source, delivers an output voltage of 380 V as confirmed by experimental results.**

Link to graphical and video abstracts, and to code:
https://latamt.ieeer9.org/index.php/transactions/article/view/10295

***Index Terms*—Switched Inductor, DC-DC Converter, Solar Photovoltaic Systems, CCM, DCM, Voltage Stress.**

I. Introduction

GLOBALLY, the employment of renewable energy sources is steadily growing as a means of reducing the environmental impact caused by the generation of electricity from fossil fuels. Along with sustainable energy sources (like solar photovoltaic systems, fuel cells, and wind energy systems), electrochemical storage systems (batteries), and electrostatic storage systems (ultracapacitors) are now widely used. However, a key challenge associated with these sources is their low-voltage output. The traditional DC-DC boost converter has the capability to attain high-voltage gain at extreme duty ratios. However, pertaining to applications in the real world, their performance is constrained by the parasitic effects of inductors and capacitors, particularly under high duty ratios. Furthermore, the switch experiences significant voltage stress, which limits its suitability for high-output voltage applications. The selection of excessively high duty cycles in order to boost voltage not only results in increased conduction losses and voltage spikes but also causes significant diode reverse recovery problems [1], [2]. Therefore, as Fig. 1 depicts, the adoption of a high step-up DC-DC converter is indispensable

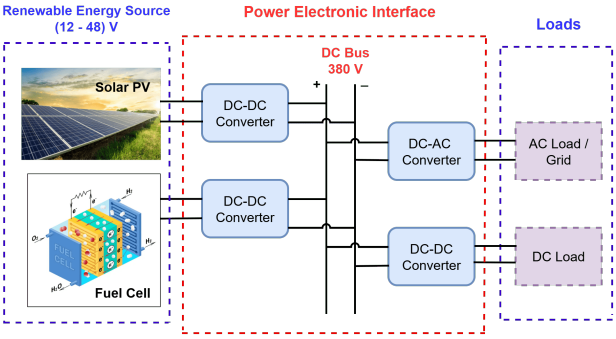

Fig. 1. Schematic representation of renewable energy source integration into the DC microgrid through the high-gain DC–DC converter.

to align the output voltage of sources like solar photovoltaic systems and fuel cells with the required DC bus voltage range of 310–400 V [3].

DC-DC converters generally fall into two types: isolated and non-isolated converters. Although isolated converters provide advantages like higher voltage conversion ratios and ensure electrical separation between input and output, they also have several limitations. These include problems related to leakage inductance, higher cost, larger size, and the necessity for high-frequency transformers or multitap inductors. In contrast, non-isolated converters eliminate the need for transformers, which can lead to higher power density. Their simple design, affordability, and ease of use make them a popular choice for low and medium-power applications [4].

The converters in [5] and [6] utilize a coupled-inductor-based topology incorporated with diode-capacitor voltage multiplier cells to attain extremely high voltage conversion ratio and ZVS operation with minimal active components. However, they introduce increased control complexity and require precise design of the coupled inductors, along with additional auxiliary components, which pose significant challenges in practical implementation. The modified SEPIC converter in [7] has several positive aspects, such as a high step-up voltage gain, minimal voltage stress on the switch, high efficiency, and fewer components. Thus, it is rendered appropriate for use in renewable energy sources. However, it has some drawbacks, like a more complex design in the version with magnetic coupling and energy loss due to hard switching in the version without it.

In [8], an interleaved high-step converter employing a diode–capacitor configuration offers advantages like a higher voltage gain, lower input current ripple, and diminished voltage stress on power switches, which facilitates the adoption

The associate editor coordinating the review of this manuscript and approving it for publication was Julio C. Rosas-Caro (*Corresponding author: Manikanta Kuraganti*).

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of lower-rated components and enhances system efficiency. However, increasing the component count and circuit complexity results in increased design effort, larger physical size, and higher cost. In [9], a modified cuk converter with SI and SC cells is presented to attain a high step-up voltage conversion ratio and non-pulsating output current. However, the converter still suffers from increased current stress and reduced efficiency resulting from high voltage stress across the semiconductor devices. In [10], a wide-range high-gain DC-DC converter employing an active switched inductor and ladder-configured voltage multiplier is introduced. The converter achieves an exceptional voltage conversion ratio by employing fewer components, even at lower duty cycles, thereby enhancing efficiency and reducing cost. Nevertheless, the voltage stress encountered by the switch and diodes remains considerably high, posing challenges in component selection and reliability.

A converter utilizing switched capacitor and switched inductor networks [11], a switched capacitor cell based converter [12], and a voltage-lift technique based converter [13] are reported to use eight, eight, and nine components respectively, and achieve a voltage conversion ratio of $\frac{(1+d)}{(1-d)}$. The topology proposed in [14] utilizes eleven components and provides a gain of $\frac{(3+d)}{2(1-d)}$. Although the aforementioned converters use fewer components, their gain is limited. The converter introduced in [16] achieves a voltage conversion ratio of $\frac{3-d}{1-d}$. Notably, despite eliminating two inductors compared to the design in [15], it still achieves a slightly higher gain. The converters presented in [17] and [18] each employ twelve components, offering voltage gains of $\frac{2(1+d)}{1-d}$ and $\frac{3+d}{1-d}$, respectively. While the design in [17] incorporates three inductors, the converter in [18] achieves a higher voltage gain over the entire practical duty cycle range using only two inductors. The high-gain DC-DC converters in [19] and [20] with extendable stages incorporate two or more switches. However, the improvement in the voltage conversion ratio remains relatively modest, despite the use of additional components in the extended stages. To resolve the shortcomings identified in the converters discussed in the aforementioned literature, a quadratic DC–DC converter incorporating a switched inductor–capacitor network, designed to achieve a high voltage conversion ratio, has been presented. The proposed converter exhibits the following key features:

- Utilizes only two inductors, resulting in reduced space requirements.
- Requires just two switches, simplifying the overall circuit design and control.
- Achieves a higher voltage gain even at relatively low duty ratios.
- Ensures very low voltage stress across the switches, enhancing reliability and efficiency.

II. Operation and Analysis of Proposed Converter

A quadratic high-gain DC-DC converter employing a switched inductor-capacitor network is illustrated in Fig. 2. The converter enables effective interfacing of renewable energy systems into the power grid. It consists of a pair of switches, a pair of inductors, five diodes, and five capacitors.

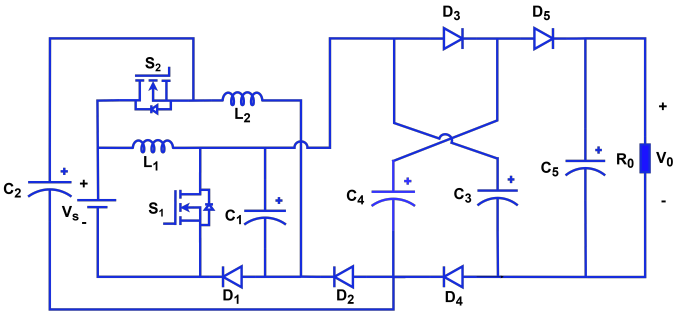

Fig. 2. Proposed switched-inductor-capacitor (SI-SC) network-based high-gain DC–DC Converter.

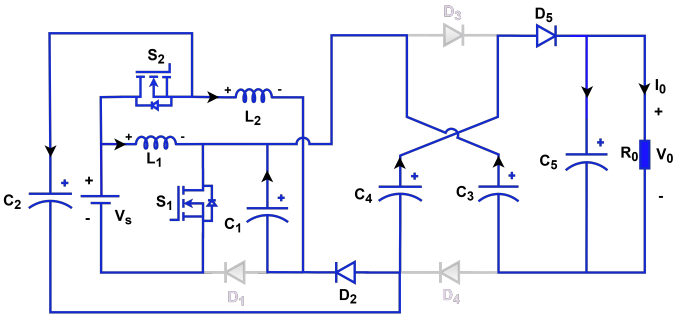

Fig. 3. Mode I operation of the proposed high-gain DC–DC converter.

The proposed configuration is evaluated in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM operation, two distinct operating states are identified based on the switching sequence of the two switches, whereas in DCM operation, three distinct operating modes are observed.

A. Continuous Conduction Mode

Mode I: Shoot-Through Condition $(0 \leq t \leq dT_s)$: In the shoot-through condition, both switches S_1 and S_2 are activated at a time. The diodes D_1, D_3 and D_4 operate in reverse bias condition, whereas the diodes D_2 and D_5 are in forward bias condition. The inductor L_1 is charged by the input voltage V_{in} through switch S_1, while the inductor L_2 is charged by the combined voltage $V_{\text{in}} + V_{C1}$ through switch S_2. The input source V_{in}, together with the energy released from capacitor C_1, simultaneously charges both inductor L_2 and capacitor C_2. Since C_2 and L_2 are connected across the same nodes, the voltage across C_2 equals that across L_2. Furthermore, capacitor C_4 not only transfers energy to charge capacitor C_5 but also supplies power to the load. Employing KVL to the circuit illustrated in Fig. 3, the voltage relations have been written as:

$$V_{L1} = V_{in} \tag{1}$$

$$V_{L1} = V_{C2} - V_{C1} \tag{2}$$

$$-V_{C1} + V_{C3} - V_0 + V_{C4} = 0 \tag{3}$$

$$V_{L1} = V_{C2} - V_{C3} + V_0 - V_{C4} \tag{4}$$

$$V_{L2} = V_{C2} \tag{5}$$

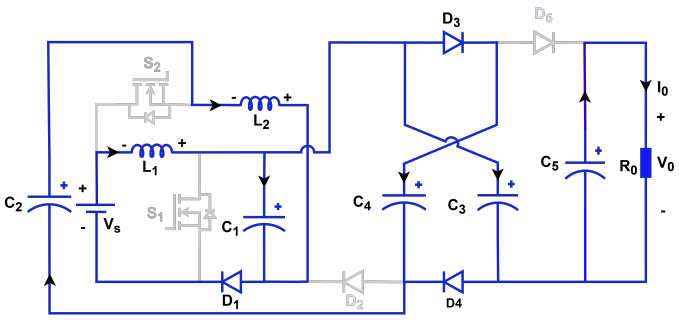

Fig. 4. Mode II operation of the proposed high-gain DC–DC converter.

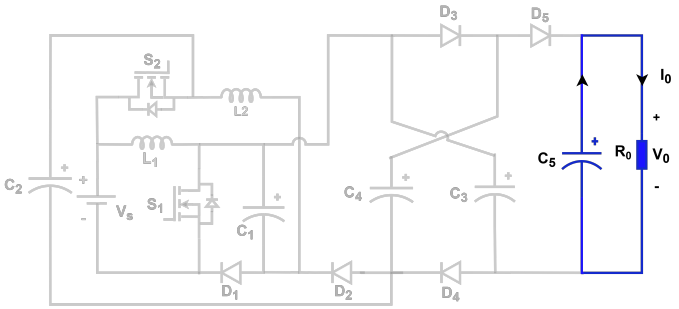

Fig. 5. Mode III operation of the proposed high-gain DC–DC converter.

$$V_{L2} = V_{C1} + V_{L1} \tag{6}$$

$$V_{L2} = V_{C1} + V_{in} \tag{7}$$

$$V_{L2} = V_{C3} - V_0 + V_{C4} + V_{in} \tag{8}$$

Employing KCL to the circuit illustrated in Fig. 3, the current relations are written as:

$$I_{in} = I_{L1} + I_{L2} + I_{C2on} \tag{9}$$

$$I_{L1} = I_{in} + I_{C1on} + I_{C3on} \tag{10}$$

$$I_{C4on} + I_{C1on} + I_{L2} + I_{C2on} = 0 \tag{11}$$

$$I_{C4on} + I_{C5on} + I_0 = 0 \tag{12}$$

$$I_{C3on} + I_0 + I_{C5on} = 0 \tag{13}$$

Mode II: Non-shoot-through condition $(dT_s \leq t \leq (1-d)T_s)$: In the non-shoot-through condition, the switches S_1 and S_2 are deactivated. The diodes D_1, D_3 and D_4 are in forward bias condition, whereas the diodes D_2 and D_5 are in reverse bias condition. The supply voltage V_{in}, along with the energy released from the inductor L_1 charges the capacitor C_1. The supply voltage V_{in}, along with the stored energy retrieved from the inductors L_1, L_2 and the capacitor C_2, charges the capacitors C_1, C_3 and C_4. The capacitor C_5 feeds energy to the load. Employing KVL to the circuit illustrated in Fig. 4, the voltage relations have been written as:

$$V_{L1} = V_{in} - V_{C1} \tag{14}$$

$$-V_{C1} + V_{C3} - V_{C2} + V_{L2} = 0 \tag{15}$$

$$V_{L2} = V_{C1} + V_{C2} - V_{C3} \tag{16}$$

$$V_{C3} = V_{C4} \tag{17}$$

$$V_{L2} = V_{C1} + V_{C2} - V_{C4} \tag{18}$$

Employing KCL to the circuit illustrated in Fig. 4, the current relations are written as:

$$I_{in} = I_{L1} \tag{19}$$

$$I_{L1} = I_{C1off} + I_{C3off} + I_{C4off} \tag{20}$$

$$I_{C1off} + I_{L2} = I_{in} \tag{21}$$

$$I_{L2} = -I_{C2off} \tag{22}$$

$$I_{C2off} + I_{C4off} + I_{C3off} = 0 \tag{23}$$

$$I_{C5off} + I_0 = 0 \tag{24}$$

Adopting a volt-sec balance for inductors L_1 and L_2 yields the following capacitor voltages:

$$V_{C1} = \frac{V_{in}}{(1-d)} \tag{25}$$

$$V_{C2} = V_{in}\frac{(2-d)}{(1-d)} \tag{26}$$

$$V_{C3} = V_{C4} = V_{in}\frac{(3-2d)}{(1-d)^2} \tag{27}$$

Solving (3) using (25), and (27) yields the voltage gain G_{CCM} of the proposed topology, expressed below:

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{I_{in}}{I_0} = \frac{(5-3d)}{(1-d)^2} \tag{28}$$

B. Discontinuous Conduction Mode

Mode I: Shoot-through condition $(0 \leq t \leq dT_s)$: The switches S_1 and S_2 are activated simultaneously at $t = t_0$. The currents associated with the inductors, denoted by I_{L1} for L_1 and I_{L2} for L_2, increase in a linear manner from zero to their respective peak values, reaching I_{LP1} and I_{LP2} at time $t = t_1$. Therefore, the converter exhibits identical behavior during Mode I in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The maximum inductor current I_{L2onp} through the inductor L_2 is expressed as:

$$I_{L2onp} = \frac{V_{in}}{L_2}\left(\frac{7-6d+d^2}{(1-d)^2} - V_0\right)dT_s \tag{29}$$

Mode II: Non-shoot-through condition $(dT_s \leq t \leq d_xT_s)$: The switches S_1 and S_2 are deactivated synchronously at $t = t_1$. By time t_2, the currents through inductors, denoted by I_{L1} for L_1 and I_{L2} for L_2, decrease to zero. The maximum current through the inductor, denoted by I_{L2offp} for L_2 is expressed as:

$$I_{L2offp} = \frac{V_{in}}{L_2}\left(\frac{d(d-2)}{(1-d)^2}\right)d_xT_s \tag{30}$$

Mode III: Non-shoot-through Condition $(d_xT_s \leq t \leq (1-d)T_s)$: At t_1, the switches S_1 and S_2 are deactivated simultaneously. By time $t_2 = d_xT_s$, the currents through inductors, denoted by I_{L1} for L_1 and I_{L2} for L_2, decrease to zero. Fig. 5 illustrates the equivalent circuit corresponding

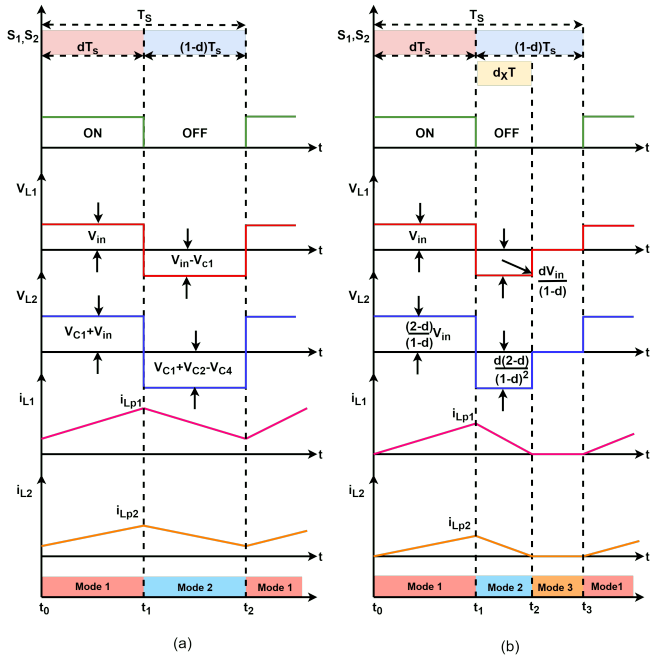

Fig. 6. Analytical waveforms of the proposed high-gain DC-DC converter: (a) CCM: (i) Gate pulses for S_1 and S_2 (ii) Voltage across L_1 (iii) Voltage across L_2 (iv) Current through L_1 (iv) Current through L_2. (b) DCM: (i) Gate pulses for S_1 and S_2 (ii) Voltage across L_1 (iii) Voltage across L_2 (iv) Current through L_1 (iv) Current through L_2.

to Mode III. Using (29) and (30), the mathematical expression for the duty ratio d_x is derived and presented in equation (31):

$$d_x = \left(\frac{7-6d+d^2}{(d-2)} - \frac{V_0}{V_{in}}\frac{(1-d)^2}{(d-2)}\right) \tag{31}$$

The mathematical expression for the voltage gain in DCM for the proposed topology, G_{DCM}, is extracted based on the averaged input current from the source, as shown in equation (32). Here, τ represents the time constant of an inductor.

$$G_{DCM} = -\frac{(1-d)^2}{4\tau} \pm \sqrt{\left(\frac{(1-d)^4}{16\tau^2}\right) + \left(\frac{7-6d+d^2}{2\tau}\right)} \tag{32}$$

Fig. 6 illustrates the analytical waveforms of the proposed topology under CCM and DCM operations.

C. Boundary Condition Mode

By equating the voltage gains obtained in CCM and DCM, ensuring that $G_{\text{DCM}} = G_{\text{CCM}}$, the converter's boundary condition is established and is expressed below.

$$\tau_{LB} = \frac{d(7-6d+d^2)}{2(d-2)\left(\frac{(5-3d)^2}{(1-d)^4} + \frac{(5-3d)d}{(d-2)}\right)} \tag{33}$$

The inductor time constant, $\tau = \frac{Lf_s}{R}$. where L is the inductance, R is the load resistance, and f_s is the switching frequency. Fig. 7 presents the dependence of the inductor time constant on the duty cycle. The graph illustrates the boundary condition that defines the operating regions of the

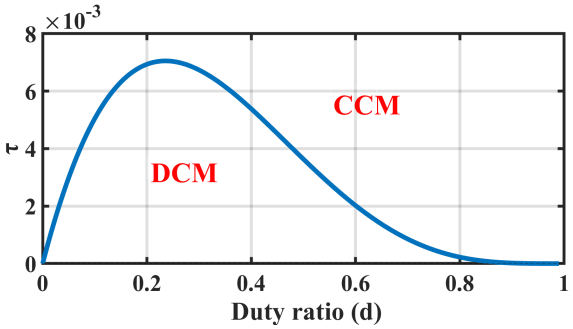

Fig. 7. Variation of the time constant with duty ratio for the proposed converter.

proposed topology, distinguishing between the CCM and DCM operating modes. Specifically, Fig. 7 shows that if $\tau > \tau_{LB}$ then the converter operates in CCM otherwise, it operates in DCM. The value of inductance is selected such that $\tau > \tau_{LB}$ inorder to ensure continuous conduction mode of operation.

D. Design and Component Selection

(i) Inductors selection: The design of the inductors ensures that the ripple current stays within 20% to 40% of the average currents. The voltage expressions for inductors L_1 and L_2 during the ON state are as follows.

$$V_{L1} = \frac{L_1\,\Delta I_{L1}}{dT_S} = V_{in} \tag{34}$$

$$V_{L2} = \frac{L_2\,\Delta I_{L2}}{dT_S} = V_{in}\frac{(2-d)}{(1-d)} \tag{35}$$

Utilizing the aforementioned equations, the subsequent equations are employed to ascertain the values of L_1 and L_2.

$$L_1 \geq \frac{dV_{in}}{\Delta I_{L1} f_s} \tag{36}$$

$$L_2 \geq \frac{dV_{in}(2-d)}{(1-d)\Delta I_{L1} f_s} \tag{37}$$

(ii) Capacitors Selection: The capacitors are sized to ensure that the voltage ripple remains below 5% of their steady-state voltages. During the ON state, the current expressions for capacitors C_1 through C_5 are expressed as follows.

$$I_{C1on} = \frac{C_1\,\Delta V_{C1}}{dT_S} = \frac{I_o(1+d)}{d(1-d)}) \tag{38}$$

$$I_{C2on} = \frac{C_2\,\Delta V_{C2}}{dT_S} = \frac{2I_o}{d} \tag{39}$$

$$I_{C3on} = \frac{C_3\,\Delta V_{C3}}{dT_S} = \frac{I_o}{d} \tag{40}$$

$$I_{C4on} = \frac{C_4\,\Delta V_{C4}}{dT_S} = \frac{I_o}{d} \tag{41}$$

$$I_{C5on} = \frac{C_5\,\Delta V_{C5}}{dT_S} = \frac{I_o(1-d)}{d} \tag{42}$$

Using the above expressions, the determination of capacitor values C_1 through C_5 is carried out as follows.

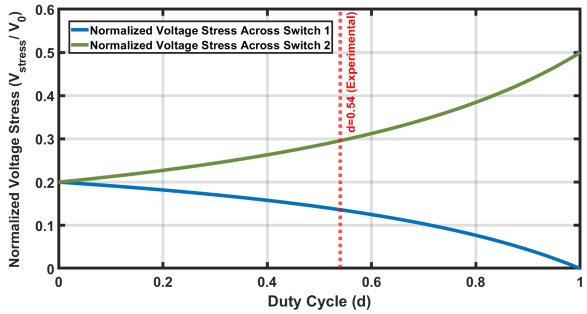

Fig. 8. Normalized voltage stress across the switches S_1 and S_2 of the proposed converter versus duty cycle.

$$C_1 \geq \frac{I_0(1+d)}{(1-d)\Delta V_{C1} f_s} \tag{43}$$

$$C_2 \geq \frac{2I_0}{\Delta V_{C2} f_s} \tag{44}$$

$$C_3 \geq \frac{I_0}{\Delta V_{C3} f_s} \tag{45}$$

$$C_4 \geq \frac{I_0}{\Delta V_{C4} f_s} \tag{46}$$

$$C_5 \geq \frac{I_0(1-d)}{\Delta V_{C5} f_s} \tag{47}$$

(iii) Selection of semiconductor devices: The selection of controlled and uncontrolled switches is determined by the voltage and current stresses they experience, and the corresponding stress expressions for the switches S_1 and S_2 are provided below.

$$V_{S1} = \frac{V_{in}}{1-d} \tag{48}$$

$$I_{S1,\text{rms}} = I_o \frac{2+d-d^2}{(1-d)^2}\sqrt{\frac{1}{d}} \tag{49}$$

$$V_{S2} = \frac{V_{in}}{(1-d)^2} \tag{50}$$

$$I_{S2,\text{rms}} = \frac{2I_o}{1-d}\sqrt{\frac{1}{d}} \tag{51}$$

The following equations describe the voltage and current stresses experienced by the diodes.

$$V_{D1} = \frac{V_{in}}{1-d} \tag{52}$$

$$V_{D2} = V_{D3} = V_{D4} = V_{D5} = \frac{(d-2)V_{in}}{(1-d)^2} \tag{53}$$

$$I_{D1,\text{rms}} = I_o \frac{3-d}{\sqrt{(1-d)^3}} \tag{54}$$

$$I_{D2,\text{rms}} = I_{D5,\text{rms}} = \frac{I_o}{\sqrt{d}} \tag{55}$$

$$I_{D3,\text{rms}} = I_{D4,\text{rms}} = \frac{I_o}{\sqrt{1-d}} \tag{56}$$

Fig. 8 illustrates the comparative plots of the voltage stress across the switches of the proposed topology.

E. Influence of Parasitic Components on the Converter's DC Voltage Conversion Ratio

The equivalent circuit of the proposed configuration, considering the effects of parasitic components, is illustrated in Fig. 9. Inductors L_1 and L_2 are associated with the internal resistances represented as R_{L1} and R_{L2}, respectively. Switches S_1 and S_2 are associated with on-state resistances represented as R_{S1} and R_{S2}, respectively is illustrated in Fig. 9. The internal resistances of the diodes D_1 through D_5 are represented by R_{D1} to R_{D5}, and their corresponding forward voltage drops are denoted by V_{F1} to V_{F5}, respectively. R_{C1} through R_{C5} denote the internal resistances of the capacitors C_1 through C_5, respectively. For the sake of simplicity, The voltage gain equation of the proposed topology, considering the parasitic components of the inductors, diodes, and switches, is derived under the assumptions that both inductors have equal parasitic resistances and both switches have equal parasitic resistances, and equal forward voltage drops for the diodes. Specifically, $R_{L1} = R_{L2} = R_L$, $R_{S1} = R_{S2} = R_S$, $R_{D1} = R_{D2} = R_{D3} = R_{D4} = R_{D5} = R_d$, and $V_{F1} = V_{F2} = V_{F3} = V_{F4} = V_{F5} = V_d$. The voltage gain equation of the proposed topology, taking parasitic components into account, is obtained as follows:

$$\left.\frac{V_0}{V_{\text{in}}}\right|_{\text{Non-ideal}} = \frac{(5-3d)-(5d^2-12d+7)\frac{V_d}{V_{\text{in}}}}{(1-d)^2 + x\frac{R_L}{R_0} + y\frac{R_d}{R_0} + z\frac{R_s}{R_0}} \tag{30}$$

where

$x = \frac{9-2d-3d^2}{(1-d)^2}$; $y = \frac{(2-d+d^2)}{d(1-d)}$; $z = \frac{(d^2-2-d)^2-(4-8d+4d^2)}{d(1-d)^2}$;

Fig. 10 illustrates the graph of voltage gain versus duty ratio for both conditions, including and excluding parasitic components.

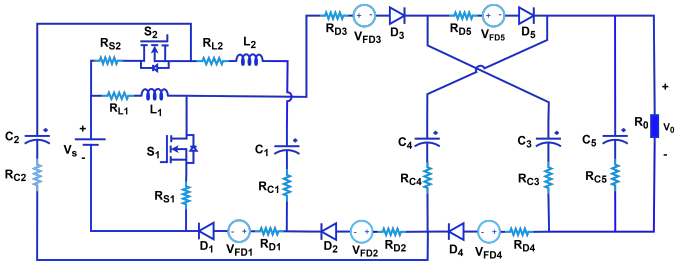

Fig. 9. Equivalent circuit of the proposed topology with non idealities.

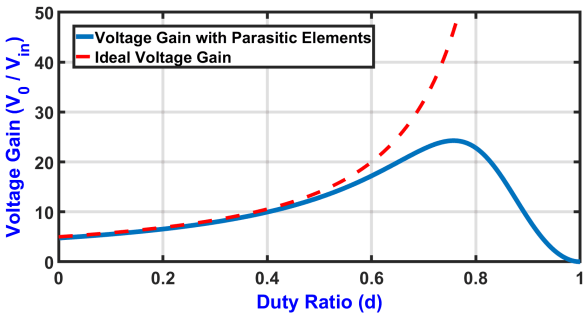

Fig. 10. Voltage gain versus duty ratio of the proposed converter under ideal and non-ideal conditions.

F. Efficiency Analysis

The total power loss associated with the proposed topology includes the power loss due to the winding resistance of the inductors, the power loss due to ESR of capacitors, the conduction and switching losses of the switches, and the conduction loss as well as the forward voltage drop loss of the diodes. The power loss resulting from the winding resistance of the inductors L_1 and L_2 is expressed as follows, considering r_L = 10 m Ω.

$$\begin{aligned} P_L &= (I_{L1,rms}^2 + I_{L2,rms}^2) r_L \\ &= \frac{(5d^2 - 14d + 13) I_0^2}{(1-d)^4} r_L = 0.93 \text{ W} \end{aligned} \tag{57}$$

The power loss associated with the ESR of the capacitors C_1 through C_5 is given as follows, considering r_c = 7 m Ω.

$$\begin{aligned} P_C &= (I_{C1,rms}^2 + I_{C2,rms}^2 + I_{C3,rms}^2 + I_{C4,rms}^2 + I_{C5,rms}^2) r_c \\ &= \frac{(5d^2 + 6) I_0^2}{d(1-d)} r_c = 0.1 \text{ W} \end{aligned} \tag{58}$$

The power loss caused by the on-state resistance of switches S_1 and S_2 is given as follows, considering r_s = 0.055 Ω.

$$\begin{aligned} P_S &= (I_{S1,rms}^2 + I_{S2,rms}^2) r_s \\ &= \frac{(d^4 - 2d^3 - 4d + 8) I_0^2}{d(1-d)^4} r_s = 1.23 \text{ W} \end{aligned} \tag{59}$$

The switching loss corresponding to the switches S_1 and S_2 is given as follows, considering (t_{on}+t_{off}) = 214 ns.

$$P_{SW} = \frac{1}{2} V_S I_S f_s (t_{on} + t_{off}) = 0.87 \text{ W} \tag{60}$$

where V_S is the maximum voltage across the switch, I_S is the maximum current through the switch, f_s is the switching frequency and t_{on} and t_{off} are the on time and off time, respectively. The power loss associated with the diodes D_1 through D_5 during conduction is given as follows, considering r_D = 0.12 Ω.

$$\begin{aligned} P_D &= (I_{D1,rms}^2 + I_{D2,rms}^2 + I_{D3,rms}^2 + I_{D4,rms}^2 + I_{D5,rms}^2) r_D \\ &= \frac{(d^3 - 4d^2 + 5d + 2) I_0^2}{d(1-d)^2} r_D = 2.35 \text{ W} \end{aligned} \tag{61}$$

the power loss due to the forward voltage drops of the diodes D_1 through D_5 is as follows, considering V_{FD} = 0.975 V.

$$\begin{aligned} P_{VF} &= (I_{D1,avg} + I_{D2,avg} + I_{D3,avg} + I_{D4,avg} + I_{D5,avg}) V_{FD} \\ &= \frac{(d - d^2 + 2) I_0^2}{d(1-d)} V_{FD} = 6.88 \text{ W} \end{aligned} \tag{62}$$

The total power loss of the proposed converter is given as

$$P_{loss} = P_L + P_C + P_S + P_{SW} + P_D + P_{VF} = 14.17 \text{ W} \tag{63}$$

The efficiency of the proposed converter is given as

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = 95.32\% \tag{64}$$

G. Small Signal Analysis

The state-space averaging method is used to develop the small-signal model of the proposed converter. The currents through the inductors and the voltages across the capacitors are taken as state variables. The source voltage is considered the input variable, whereas the voltage across the load is taken as the output variable. A resistance r is considered as the loop resistance to establish the state equations. During the ON period, the two switches are turned ON, and the corresponding state equations are derived as follows.

$$\left.\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{v_{in}(t)}{L_1} \\ \frac{di_{L2}(t)}{dt} &= \frac{v_{in}(t) + v_{c1}(t)}{L_2} \\ \frac{dv_{c1}(t)}{dt} &= \frac{-v_{c1}(t) + v_{c2}(t) - v_{in}(t)}{rC_1} \\ \frac{dv_{c2}(t)}{dt} &= \frac{v_{c1}(t) - v_{c2}(t) + v_{in}(t)}{rC_2} \\ \frac{dv_{c3}(t)}{dt} &= \frac{v_{c1}(t) - v_{c3}(t) - v_{c4}(t) + v_{c5}(t)}{rC_3} \\ \frac{dv_{c4}(t)}{dt} &= \frac{v_{c2}(t) - v_{c3}(t) - v_{c4}(t) + v_{c5}(t) - v_{in}(t)}{rC_4} \\ \frac{dv_{c5}(t)}{dt} &= \frac{v_{in}(t) - v_{c2}(t) + v_{c3}(t) + v_{c4}(t) - v_{c5}(t)}{rC_5} \end{aligned}\right\} d(t)T_s$$

During the OFF period, the two switches are turned OFF, and the corresponding state equations are derived as follows.

$$\left.\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{v_{in}(t) - v_{c1}(t)}{L_1} \\ \frac{di_{L2}(t)}{dt} &= \frac{v_{c1}(t) + v_{c2}(t) - v_{c3}(t)}{L_2} \\ \frac{dv_{c1}(t)}{dt} &= \frac{i_{L1}(t) - i_{L2}(t)}{C_1} \\ \frac{dv_{c2}(t)}{dt} &= \frac{-i_{L2}(t)}{C_2} \\ \frac{dv_{c3}(t)}{dt} &= \frac{v_{c4}(t) - v_{c3}(t)}{rC_3} \\ \frac{dv_{c4}(t)}{dt} &= \frac{v_{c3}(t) - v_{c4}(t)}{rC_4} \\ \frac{dv_{c5}(t)}{dt} &= \frac{-v_{c5}(t)}{RC_5} \end{aligned}\right\} (1 - d(t))T_s$$

The state-space matrices during the ON period are represented by eqs. (65) and (66), whereas the state-space matrices during the OFF period are represented by eqs. (67) and (68). The state-space averaged matrices are presented in Eqs. (69) and (70). The control to output voltage transfer function is presented in Eq. (71). All the poles of the transfer function are located in the left half of the s-plane, which confirms the stability of the proposed converter.

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c4}(t)}{dt} \\ \frac{dv_{c5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{rC_1} & \frac{1}{rC_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{rC_2} & -\frac{1}{rC_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{rC_3} & 0 & -\frac{1}{rC_3} & -\frac{1}{rC_3} & \frac{1}{rC_3} \\ 0 & 0 & 0 & \frac{1}{rC_4} & -\frac{1}{rC_4} & -\frac{1}{rC_4} & \frac{1}{rC_4} \\ 0 & 0 & 0 & -\frac{1}{rC_5} & \frac{1}{rC_5} & \frac{1}{rC_5} & -\frac{1}{rC_5} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c4}(t) \\ v_{c5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ -\frac{1}{rC_1} \\ \frac{1}{rC_2} \\ 0 \\ -\frac{1}{rC_4} \\ \frac{1}{rC_5} \end{bmatrix} v_{in}(t) \tag{65}$$

$$v_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & v_{c1}(t) & v_{c2}(t) & v_{c3}(t) & v_{c4}(t) & v_{c5}(t) \end{bmatrix}^T \tag{66}$$

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c4}(t)}{dt} \\ \frac{dv_{c5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} & 0 & 0 \\ \frac{1}{rC_1} & -\frac{1}{rC_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{rC_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{rC_3} & \frac{1}{rC_3} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{rC_4} & -\frac{1}{rC_4} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{RC_5} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c4}(t) \\ v_{c5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \tag{67}$$

$$v_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & v_{c1}(t) & v_{c2}(t) & v_{c3}(t) & v_{c4}(t) & v_{c5}(t) \end{bmatrix}^T \tag{68}$$

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c4}(t)}{dt} \\ \frac{dv_{c5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{1-d}{L_2} & \frac{d-1}{L_2} & 0 & 0 \\ \frac{1-d}{rC_1} & \frac{d-1}{rC_1} & -\frac{d}{rC_1} & \frac{d}{rC_1} & 0 & 0 & 0 \\ 0 & \frac{d-1}{rC_2} & \frac{d}{rC_2} & -\frac{d}{rC_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{d}{rC_3} & 0 & -\frac{1}{rC_3} & -\frac{1-2d}{rC_3} & \frac{d}{rC_3} \\ 0 & 0 & 0 & \frac{d}{rC_4} & \frac{1-2d}{rC_4} & -\frac{1}{rC_4} & \frac{d}{rC_4} \\ 0 & 0 & 0 & -\frac{d}{rC_5} & \frac{d}{rC_5} & \frac{d}{rC_5} & (-\frac{d}{rC_5} - \frac{1-d}{RC_5}) \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c4}(t) \\ v_{c5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{d}{L_2} \\ -\frac{d}{rC_1} \\ \frac{d}{rC_2} \\ 0 \\ -\frac{d}{rC_4} \\ \frac{d}{rC_5} \end{bmatrix} v_{in}(t) \tag{69}$$

$$v_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & v_{c1}(t) & v_{c2}(t) & v_{c3}(t) & v_{c4}(t) & v_{c5}(t) \end{bmatrix}^T \tag{70}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{6.72 \times 10^4 s^6 + 6.11 \times 10^{13} s^5 + 1.38 \times 10^{22} s^4 + 2.2 \times 10^{27} s^3 + 4.98 \times 10^{35} s^2 + 7.46 \times 10^{34} s + 1.26 \times 10^{43}}{s^7 + 1.64 \times 10^9 s^6 + 8.74 \times 10^{17} s^5 + 1.5 \times 10^{26} s^4 + 4.47 \times 10^{27} s^3 + 1.4 \times 10^{34} s^2 + 3.8 \times 10^{35} s + 9.5 \times 10^{39}} \tag{71}$$

III. Comparative Performance

The proposed topology is assessed against other existing topologies with respect to voltage conversion ratio, voltage stress, component count, maximum achievable gain, input voltage, output voltage, output power, highest voltage stress on diode, switching frequency, and efficiency, as summarized in Table I. Fig. 10 and Fig. 11 illustrate the voltage conversion ratio versus duty cycle, highlighting the superior voltage gain of the proposed topology compared to existing designs.

Although the converters reported in [21]– [23] employ twelve components, they still rely on additional inductors. The converter in [21] offers only a modest improvement in voltage gain over the conventional boost converter, whereas the topology in [22] achieves a significant enhancement in voltage gain by exhibiting a quadratic voltage gain characteristic. Nevertheless, these converters provide lower voltage gain than the proposed topology. Furthermore, the converter reported in [23] incorporates a larger number of inductors and subjects both switches to higher voltage stress compared to the proposed converter. The topology reported in [24] matches the proposed converter in component count but incorporates more inductors and offers a lower voltage gain, although the voltage stresses imposed on switches S_1 and S_2 in [24] are equal to those in the proposed converter. However, the topology reported in [23] features a lower component count, utilizing only twelve components, in contrast to fourteen used in the converter described in [24]. On the other hand, the converter reported in [24] provides the advantage of a reduced voltage stress experienced by the switches in comparison with that of the converter in [23]. Moreover, both converters incorporate a

TABLE I
COMPARATIVE ANALYSIS OF PROPOSED AND EXISTING CONVERTERS

Topology	**[21]**	**[22]**	**[23]**	**[24]**	**[10]**	**[25]**	**[26]**	**[27]**	**[28]**	**[Proposed]**
Switches	2	1	2	2	3	1	1	2	2	2
Diodes	2	5	3	3	3	5	2	2	6	5
Inductors	4	3	4	4	3	4	1	2	4	2
Capacitors	4	3	3	5	3	6	2	2	6	5
Device count	12	12	12	14	12	16	6	8	18	14
Voltage gain	$\frac{(1+d)}{(1-d)}$	$\frac{d^2}{(1-d)^2}$	$\frac{-d^2+2d+1}{(1-d)^2}$	$\frac{2d(2-d)}{(1-d)^2}$	$\frac{3-d^2}{(1-d)^2}$	$\frac{-2d^2+2d+1}{(1-d)^2}$	$\frac{2-d}{1-d}$	$\frac{1}{(1-d)^2}$	$\frac{3+d}{1-d}$	$\frac{5-3d}{(1-d)^2}$
Voltage gain at $d = 0.8$	9	16	49	48	59	33	6	25	19	65
Switch Stress	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)}$	$V_S = \frac{V_i}{(1-d)^2}$	$V_{S1} = \frac{V_i(1+d)}{(1-d)^2}$ $V_{S2} = \frac{V_i(1+d)}{(1-d)^2}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)^2}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)}$ $V_{S3} = \frac{2V_i}{(1-d)^2}$	$V_S = \frac{V_i}{(1-d)^2}$	$V_S = \frac{V_i}{1-d}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)^2}$	$V_S = \frac{V_i}{1-d}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)^2}$
Max. Voltage Stress on Diode	$\frac{V_i}{(1-d)}$	$\frac{V_i}{(1-d)^2}$	$\frac{V_i(2-d)}{(1-d)^2}$	$\frac{V_i(2-d)}{(1-d)^2}$	$\frac{2V_i}{(1-d)^2}$	$\frac{V_i}{(1-d)^2}$	$\frac{V_i}{(1-d)}$	$\frac{V_i}{(1-d)^2}$	$\frac{V_i}{(1-d)}$	$\frac{V_i(d-2)}{(1-d)^2}$
Input Voltage	24 V	20 V	20 V	30 V	24 V	24 V	50 V	20 V	24 V	24 V
Output Voltage	120 V	45 V	80 V	200 V	310 V	217.7 V	200 V	164 V	200 V	380 V
Output Power	240 W	45 W	150 W	160 W	300 W	200 W	100 W	135 W	200 W	300 W
Switching Frequency	25 KHz	40 KHz	20 KHz	40 KHz	40 KHz	50 KHz	100 KHz	20 KHz	50 KHz	50 KHz
Efficiency	91	80	90	93.82	95.72	90	95.4	-	-	95.32

TABLE II
COMPARATIVE ANALYSIS OF PROPOSED CONVERTER WITH SWITCHED-INDUCTOR AND SWITCHED-CAPACITOR NETWORK BASED CONVERTERS

Topology	**[29]**	**[30]**	**[31]**	**[32]**	**[33]**	**[34]**	**[Proposed]**
Switches	2	2	2	1	2	2	2
Diodes	6	6	3	6	6	4	5
Inductors	1	4	4	3	2	2	2
Capacitors	5	4	4	4	6	4	5
Device Count	14	16	13	14	16	12	14
Voltage Gain	$\frac{4}{(1-d)}$	$\frac{2d}{(1-d)^2}$	$\frac{(2-d)^2}{(1-d)^2}$	$\frac{(3-d)}{(1-d)^2}$	$\frac{(5+d)}{(1-d)}$	$\frac{4-d}{(1-d)}$	$\frac{(5-3d)}{(1-d)^2}$
Voltage gain at $d = 0.8$	20	40	36	55	29	16	65
Switch Stress	$V_{S1} = \frac{2V_i}{(1-d)}$ $V_{S2} = \frac{2V_i}{(1-d)}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i(3d-1)}{(1-d)^2}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)^2}$	$V_S = \frac{2V_i}{(1-d)^2}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)}$	$V_{S1} = \frac{V_i}{(1-d)}$ $V_{S2} = \frac{V_i}{(1-d)^2}$
Highest Voltage Stress on Diode	$\frac{2V_i}{(1-d)}$	$\frac{V_i(1-3d)}{(1-d)^2}$	$\frac{(2-d)V_i}{(1-d)^2}$	$\frac{V_i(3+d)}{2(1-d)^2}$	$\frac{2V_i}{(1-d)}$	$\frac{2V_i}{(1-d)}$	$\frac{V_i(d-2)}{(1-d)^2}$
Input Voltage	20 V	24 V	48 V	48 V	20 V	40 V	24 V
Output Voltage	200 V	180 V	210 V	300 V	400 V	330 V	380 V
Output Power	100 W	250 W	400 W	300 W	200 W	600 W	300 W
Switching Frequency	200 KHz	50 KHz	50 KHz	20 KHz	50 KHz	30 KHz	50 KHz
Efficiency	90.48	92.4	95.2	94.4	94	93.2	95.32
Required Duty Ratio for V_{in} = 24 V and V_0 = 380 V	0.747	0.704	0.664	0.635	0.643	0.797	0.54

higher inductor count than the proposed converter. Although similar voltage gain profiles are observed in the converters presented in [23] and [24], their voltage gains are lower across all duty cycles in comparison with that of the proposed topology. Although the topology presented in [10] exhibits a voltage conversion ratio profile similar to that of the proposed converter, it requires three switches and three inductors. The voltage gain profile of the topology reported in [25] is similar to that of the topology in [23] at lower duty cycles, but it exhibits superior gain performance at higher duty cycles.

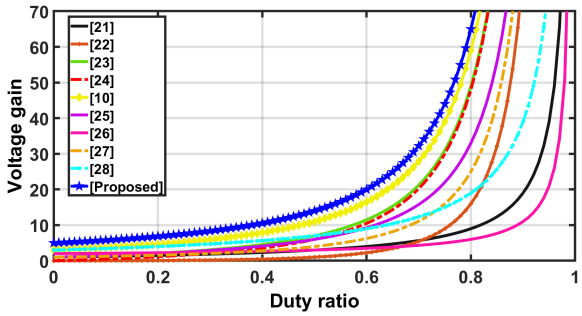

Fig. 11. Comparative Analysis of Voltage Gain: Proposed Converter vs. Existing Converters.

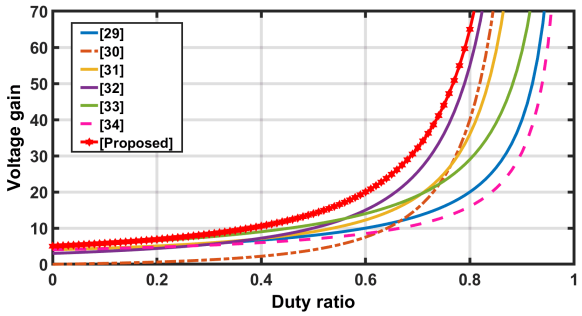

Fig. 12. Comparative Analysis of Voltage Gain: Proposed Converter vs. SLSC Network Based Converters .

However, the converter in [25] requires a total of sixteen components, including four inductors, yet the overall voltage gain improvement remains relatively limited. The converters presented in [26] and [27] require fewer components but exhibit a low voltage gain profile. The converter reported in [28] requires a higher number of components and inductors and exhibits a lower voltage gain profile compared to the proposed converter. Table II summarizes the comparative analysis of the proposed converter with switched-inductor- and switched-capacitor-network-based converters, while Fig. 11 illustrates the voltage gain versus duty ratio for the corresponding topologies. The topology reported in [29] provides a voltage gain merely fourfold compared to that of the classical boost converter, despite employing a higher component count of fourteen. Additionally, its voltage gain performance is inadequate across all duty ratios below 0.6. Converters reported in [30]- [32] require a higher number of components, whereas the converter in [33] requires more components and exhibits a lower voltage gain profile compared to the proposed topology. The converter in [34] employs fewer components but provides a very low voltage gain profile. The converters reported in [29]– [34] require a higher duty ratio to achieve the same output voltage for a given input voltage compared to the proposed converter. The effect of parasitic components associated with the inductors, capacitors, switches, and diodes becomes significant under practical operating conditions. Therefore, a duty ratio of D=0.8, which is generally regarded as the maximum practical duty cycle, is considered for comparison. At this duty ratio, the proposed converter achieves a higher voltage gain compared to the existing topologies listed in the table I and table II. In conclusion, the proposed topology demonstrates superior performance compared to many existing converter configurations by achieving a higher voltage gain even at low duty ratios, while requiring a reduced component count compared to some existing topologies. Furthermore, the reduced voltage stress across the switches enhances reliability and efficiency, making the topology well-suited for industrial DC and other applications.

IV. Experimental Analysis

To figure out the viability of the proposed topology, a 300W laboratory prototype shown in Fig. 21 was constructed with a 24 V input voltage to deliver an output voltage of 380 V. TABLE III provides its design specifications.

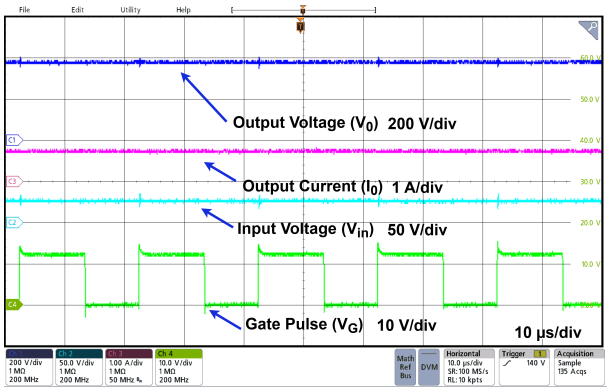

Fig. 13. Under steady-state operating conditions: (a) V_0, Output Voltage (V); (b) I_0, Output Current (A); (c) V_{in}, Input Voltage (V); (d) V_G, Gate Pulse (V).

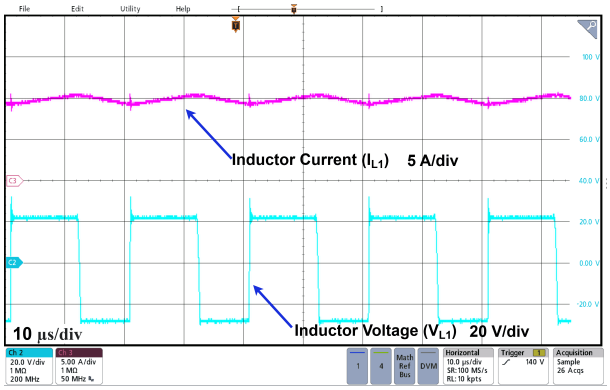

Fig. 14. Under steady-state operating conditions: (a) I_{L1}, Current through L_1 (A); (b) V_{L1}, Voltage across L_2 (V).

TABLE III
Component Selection of the Proposed Converter

Specification	Value
Input Voltage	24 V
Output Voltage	380 V
Switching Frequency	50 kHz
Inductors	$L_1 = L_2 = 0.35$ mH
Capacitors	22 μF
Switches	S_1, S_2 : IRFP260
Diodes	D_1 : MUR820G D_2 through D_5 : MUR840G

The steady-state waveforms were captured at a source voltage of 24 V, yielding 380 V at the load, where both

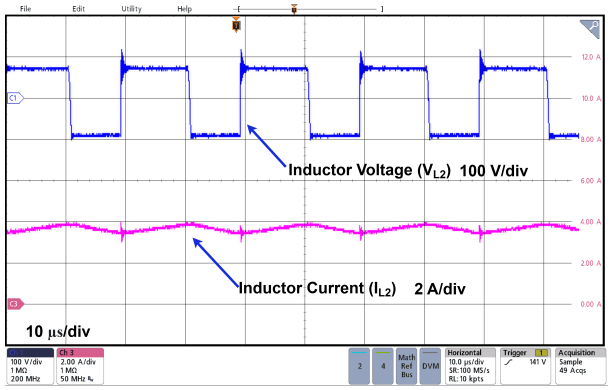

Fig. 15. Under steady-state operating conditions: (a) V_{L2}, Voltage across L_2 (V); (b) I_{L2}, Current through L_2 (A).

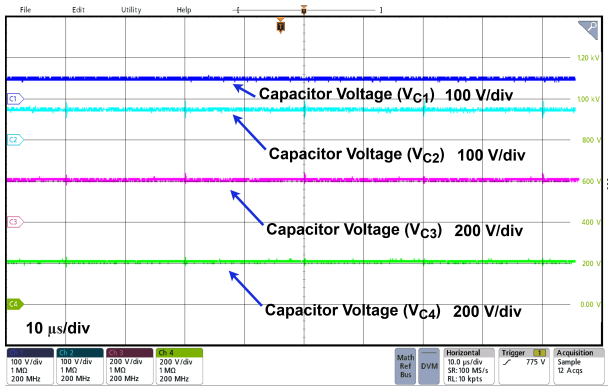

Fig. 16. Under steady-state operating conditions: (a) V_{C1}, (b) V_{C2}, (c) V_{C3}, (d) V_{C4} — Capacitor Voltages (V).

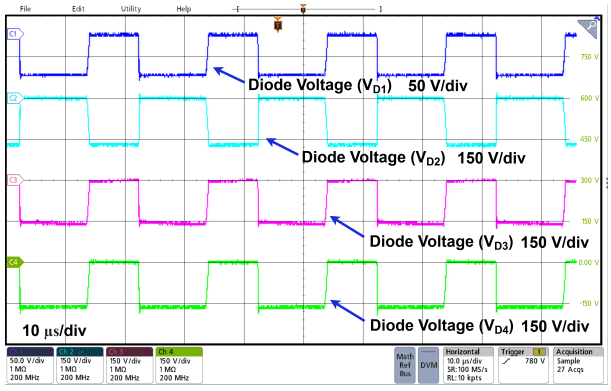

Fig. 17. Under steady-state operating conditions: (a) V_{D1}, (b) V_{D2}, (c) V_{D3}, (d) V_{D4} — Diode Voltages (V).

switches were driven by gate pulses under a duty ratio of 0.54 with a switching frequency of 50 kHz. The converter's performance was assessed under continuous conduction mode operation. Fig. 13 displays the experimental waveforms for V_{GS} (gate pulse), V_{in} (supply voltage), V_0 (output voltage), and I_0 (output current), where V_{in} = 24 V, V_0 = 380 V, and I_0 = 0.78 A. Fig. 14 displays the experimental waveforms for V_{L1} (voltage across L_1) and I_{L1} (current through L_1). Fig. 15 displays the experimental waveforms for V_{L2} (voltage across L_2) and I_{L2} (current through L_2). The inductor currents I_{L1rms} and I_{L2rms} were recorded as 9.5 A and 3.6 A,

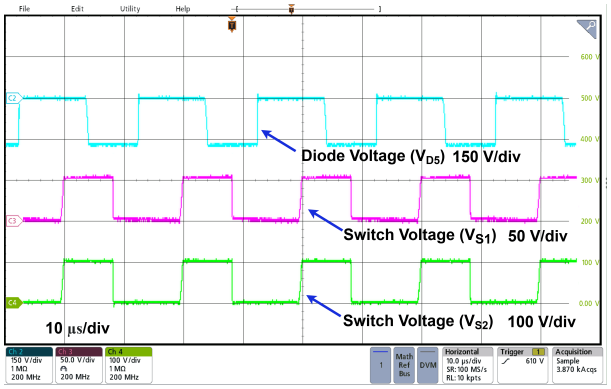

Fig. 18. Under steady-state operating conditions: (a) V_{D5}, (b) V_{S1}, (c) V_{S2} — Device Voltages (V).

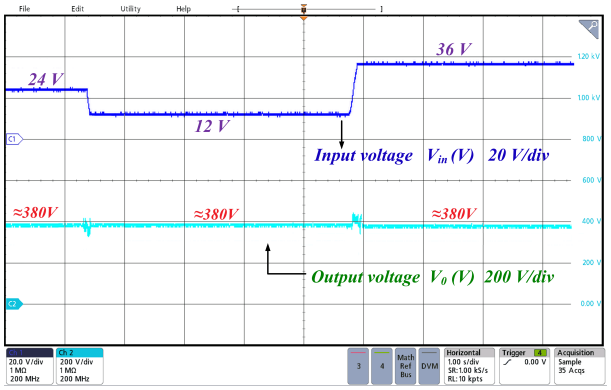

Fig. 19. Dynamic Response of Input Voltage.

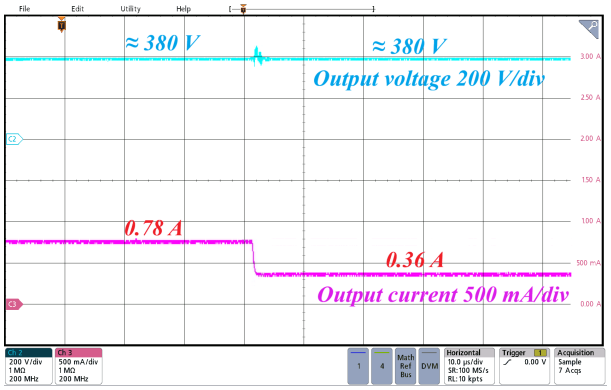

Fig. 20. Dynamic Response of Load Current.

respectively. The experimental waveforms for the capacitor voltages V_{C1} through V_{C4} are shown in Fig. 16, where V_{C1} = 53 V, V_{C2} = 75 V, and V_{C3}= V_{C4} = 216 V. The experimental waveforms of diode voltages V_{D1} through V_{D4} are portrayed in Fig. 17 and Fig. 18 displays the experimental waveforms of the diode voltage V_{D5} and the voltage stresses on the switches (V_{S1}, and V_{S2}). The measured voltage stresses across the switches, denoted by V_{S1} for S_1 and V_{S2} for S_2, are 52 V and 112 V, respectively. For diodes D_1 through D_5, the corresponding voltage stresses V_{D1}, V_{D2}, V_{D3}, V_{D4}, and V_{D5} were recorded as 52 V, 164 V, 164 V, 164 V, and 164 V, respectively. Fig. 19 and Fig. 20 illustrate the dynamic response of the proposed converter under variations in input

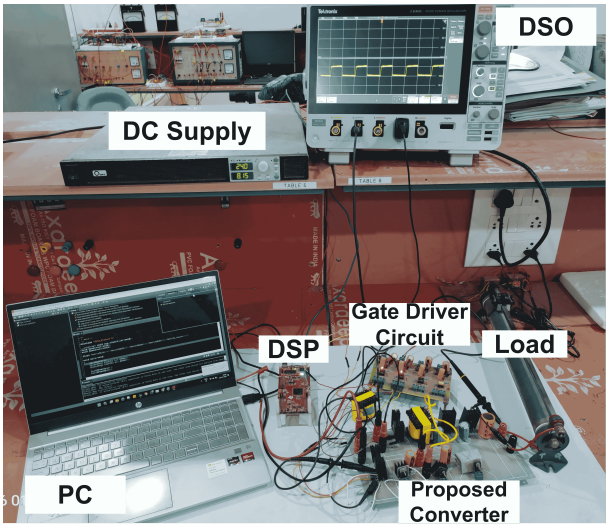

Fig. 21. Experimental Setup of The Proposed Converter.

voltage and load current. The proposed converter delivers an output voltage of 380 V, while the maximum voltage stresses across the switch and the diodes are limited to 112 V and 164 V, respectively. This corresponds to approximately 30% and 43% of the output voltage, indicating that both the switch and diode stresses remain well below the output level. Such reduced voltage stress not only enhances device reliability but also allows the use of low-voltage-rated components, thereby improving overall efficiency and reducing cost.

V. Conclusion

A novel high-gain quadratic DC–DC converter, incorporating a switched inductor–capacitor network and designed for applications involving single phase systems with a solar photovoltaic input, was presented in this article. The operation of the proposed topology was examined under both CCM and DCM modes. Despite certain disadvantages such as low power density, construction complexity, and the absence of a common ground, the proposed topology achieves a substantial voltage conversion ratio over a wide range of duty cycles while ensuring significantly reduced voltage stress on the switches. Owing to its ability to achieve a higher voltage gain even at lower duty cycles compared with conventional boost and other high-gain DC–DC converters, this configuration is well-suited for microgrid applications. The operational performance of the proposed topology was assessed by means of experimental validation. The proposed topology was designed to deliver 300 W of output power while operating with a switching frequency of 50 kHz and to achieve an output voltage of 380 V from a 24 V input, which served as the reference voltage for the solar photovoltaic source.

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