A Compact Nine-Level Boost Multilevel Inverter Using Novel Switching Control

Karunakaran Eddu, *Student Member, IEEE,* Suresh Yellasiri, *Senior Member, IEEE,* Kancharapu Aditya, *Member, IEEE,* and Nageswar Rao Bhukya, *Member, IEEE*

***Abstract*—Switched-capacitor multilevel inverters (SCMLIs) have gained considerable attention in various power conversion applications due to their inherent voltage boosting capability and reduced component count, eliminating the need for auxiliary sources, transformers, or inductors. This paper proposes a novel nine-level compact boost multilevel inverter (NCBMLI) that employs only ten switches, two capacitors, and a single DC input source to achieve a voltage gain of twice the input voltage. The proposed topology is designed for compactness and cost-effectiveness by minimizing the number of active components per voltage level. Further, to operate the proposed NCBMLI a novel fuzzy logic switching method is implemented, offering a flexible alternative to conventional control methods based on static logic circuits and pre-defined lookup tables. This method utilizes rule-based membership functions (MFs) to generate adaptive switching signals, which enhances the overall performance. A detailed comparative analysis is presented to highlight the advantages of the proposed NCBMLI. Furthermore, the effective performance of the proposed NCBMLI is validated through hardware implementation under varying dynamic load conditions and modulation indices.**

Link to graphical and video abstracts, and to code:
https://latamt.ieeer9.org/index.php/transactions/article/view/10065

***Index Terms*—Multilevel inverters (MLIs), switched capacitors(SCs), voltage boosting, membership functions(MFs), fuzzy logic switching(FLS).**

NOMENCLATURE

V_{dc}	Input DC voltage.
V_o	Output voltage.
C_1	Fixed capacitor.
C_f	Flying capacitor.
ESR	Equivalent series resistance.
R_{eq}	Equivalent resistance during charging/discharging.
Q	Electric charge.
C	Capacitance.
V	Voltage.
ΔQ	Change in electric charge.
i_o	Peak load current.
t_n	Time interval.
R	Resistance.
ω	Angular frequency.
$x\%$	Ripple percentage.
FLS	Fuzzy logic switching.
FLC	Fuzzy logic controller.
UMF	Upper membership function.
LMF	Lower membership function.
FOU	Footprint of Uncertainty.
PWM	Pulse width modulation.
SQ	Sine quantizer.
HH	Half height.
MFs	Membership functions.
V_{ref}	Reference Signal.
V_d	Amplitude of reference signal.
K	Quantization interval.
e	Scaling factor.
N	No of levels.
Φ_m	Extraction of firing angle (SQ).
F_j	Conversion of angle to switching magnitude (SQ).
β_k	Extraction of firing angles (HH).
Y_l	Conversion of angles to switching magnitudes (HH).
θ_q	Optimized firing angles.
TSV	Total standing voltage.
V_{sw}	Voltage across individual switch.
CF_{pu}	Cost factor per unit.
N_{sw}	Number of switches.
N_D	Number of diodes.
N_C	Number of capacitors.
α	Weightage factor.
MBV	Maximum boost voltage.
N_L	Number of levels.
P_{sw}	Switch loss.
P_{cond}	Conduction loss.
f_{sw}	Switching frequency.
f_{ref}	Reference frequency.
I_{sw}	Switch current.
t_{on}	Turn on time of the switch.
t_{off}	Turn off time of the switch.
I_{rms}	Output RMS current.
R_{on}	On-state resistance of the switch.
I_{dc}	Average current.
P_{Crip}	Capacitor ripple loss.
P_{Tl}	Total loss.

The associate editor coordinating the review of this manuscript and approving it for publication was Julio C. Rosas-Caro (*Corresponding author: Karunakaran Eddu).*

Karunakaran Eddu, S. Yellasiri, and K. Aditya are with the National Institute of Technology Karnataka, Surathkal, Mangalore, India (e-mails: eddukarunakaran.227ee002@nitk.edu.in, ysuresh.ee@nitk.edu.in, and aditya.187ee002@nitk.edu.in).

N. R. Bhukya is with the Dr B R Ambedkar National Institute of Technology, Jalandhar, Punjab, India (e-mail: raobn@nitj.ac.in).

I. INTRODUCTION

MULTILEVEL INVERTERS (MLIs) offer a promising solution to many of the inverter related challenges dealing with unreliable power grids, limited technical resources, and cost constraints. By generating high-quality output with reduced harmonic distortion, minimizing dv/dt

stress on switches, these inverters improve power reliability and compatibility with sensitive consumer and industrial equipment. Their modular and compact design reduces the number of components needed, thereby reducing both cost and maintenance requirements, which is a key advantage in remote or marginalized areas [1], [2]. However, conventional multilevel inverter topologies, such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) configurations, require a significant number of components including switches, diodes, and capacitors as the output voltage level escalates. This leads to higher circuit complexity, increased implementation cost, and challenges associated with voltage imbalance. Moreover, NPC and FC inverters demand additional capacitor voltage control mechanisms. In addition, symmetrical CHBs requires more number of switches & DC sources to achieve higher voltage levels. In contrast, asymmetrical CHBs can achieve higher voltage levels with fewer switches and DC sources. However, they require a higher input DC voltage, typically in binary or trinary ratios. Furthermore, MLIs that use cascaded transformers for voltage boosting lead to increased circuit complexity, higher losses, larger size, and higher costs [3]–[6].

Considering the above limitations of conventional MLI topologies, recent research has emphasized the advantages of switched capacitor multilevel inverters, establishing them as strong alternatives to traditional designs. By employing capacitors as supplementary DC sources, SCMLIs can generate output voltage waveforms that closely approximate a pure sine wave without the need for separate DC sources. These capacitors not only enhance the overall output voltage but also inherently maintain voltage balance without requiring additional circuitry or complex control methods. Furthermore, the series-parallel capacitor configuration with self-voltage balancing eliminates the need for transformers and inductors, leading to a simpler and more efficient inverter topology [7], [8]. Firstly, the author in [9] introduced a scalable and adaptive topology that incorporates a greater number of switches, however it attains a reduced voltage gain than the proposed inverter. Different structures of switched capacitor inverter designs have been introduced in [10]–[13] for generating 9-level output waveforms with voltage gain of two & four. For instance, the inverter presented in [10] incorporates a common ground configuration, however it requires higher number of switches, capacitors and diodes, which leads to higher power losses and voltage balancing issues. Similarly the inverter in [11], achieves a reduction in the number of capacitors and diodes. However, it comprises of higher number of switches, leading to greater complexity to control. Further, the topologies presented in [12]–[14] introduce clamping-type switched capacitor multilevel inverters that utilize additional bidirectional switches and diodes to control capacitor voltage. Although the inverter proposed in [12] eliminates the need for diodes, it employs significantly a higher number of switches, which in turn increases losses, cost, and control complexity.

Furthermore, a boost inverter topology with a reduced number of switches was introduced in the reference [15]; however, it relies on an H-bridge inverter for polarity reversal, which results in higher voltage stress on the polarity changing switches. Later, the inverter employing with minimized component count was introduced in [16], utilizing three capacitors and two diodes for voltage boosting. Nevertheless, the use of uncontrolled diodes introduces multiple conduction paths, which may effect circuit performance. The topologies suggested in [17], [18] present nine-level quadruple-boost inverters with enhanced voltage gain but require a larger number of switches, resulting in increased total standing voltage and a higher cost factor. Furthermore, the multilevel modular inverter structures proposed in [19], [20] incorporate a common ground configuration; however, they involve a greater number of capacitors and may cause intermittent disconnection of the DC source under certain switching states. Similarly, the T-type switched capacitor inverter is presented in [21] achieves voltage boosting by connecting across the input source, yet it faces challenges in maintaining voltage balance, particularly under dynamic load conditions. In overall, above mentioned configurations inherently suffer from drawbacks such as increased component count, higher conduction and switching losses, complex gate-driving requirements for bidirectional switches, and reduced overall efficiency. To address the aforementioned limitations, this paper proposes a novel nine-level compact boost multilevel inverter that integrates a combination of fixed capacitor and flying capacitor(FC) to achieve a voltage gain of two. The proposed inverter completely eliminates diodes and significantly reduces the number of switches, thereby lowering the total number of components, minimizing losses, eliminating the need for additional sensors, and resulting in a compact structure with improved overall efficiency. The proposed NCBMLI is highly suitable for medium-voltage applications, including residential PV systems, uninterruptable power supplies(UPS), low-medium voltage motor drives, and electric vehicle systems.

Moreover, in recent years, several control techniques have been implemented for switched capacitor inverters. In contrast, many of them rely on logic gate-based designs [22], which inevitably increase circuit complexity and hardware design. To address this limitation, this paper introduces an optimized fuzzy logic switching strategy that employs rule-based membership functions, by simplifying the overall control method. The optimized fuzzy logic provides adaptive control under dynamic load variations, can effectively balance the capacitor voltages, achieves lower THD, and enhances efficiency. Furthermore, it intelligently optimizes switching decisions to minimize losses and improve the overall performance of the inverter. Here are some salient features of the proposed inverter:

1) It requires only ten switches and two capacitors with one DC-source to achieve voltage boosting of two.
2) The peak voltage across the switches remains below $2V_{dc}$, thereby minimizing the blocking voltage stress on each semiconductor device.
3) It requires only a few conducting switches in each voltage level which implies low conduction losses and improved efficiency.
4) It eliminates the need for an additional H-bridge to generate negative polarity.

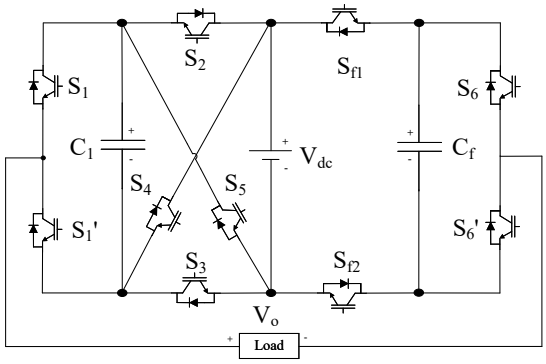

Fig. 1. Proposed NCBMLI.

5) All the switches are operated at line frequency(50Hz) with reduced switch losses due to fuzzy control switching.

The rest of this paper is organized as follows. Section II describes the configuration of the proposed NCBMLI, including its circuit topology, operating modes, and determination of capacitors. Section III outlines the modulation strategy for the proposed inverter. A comparative analysis between the proposed NCBMLI and existing MLI topologies is presented in Section IV, followed by an assessment of power loss distribution and the efficiency in Section V. Section VI provides performance validation through detailed experimental results. Finally, Section VII presents the conclusion of the paper.

II. Proposed NCBMLI topology

A. Overview of the Circuit

The proposed NCBMLI circuit is shown in the Fig.1, with ten switches (S_1 to S_6 & S_{f1},S_{f2}), two capacitors(C_1 & C_f) and one DC-source for obtaining the 9-level voltage. Capacitor C_1 is charged to V_{dc} and C_f is the FC with $0.5V_{dc}$, for boosting the voltage gain of two. The operating modes of the proposed NCBMLI for each level is illustrated in the Fig.2 and the switching states are shown in the Table I. In Fig.2, it can be observed that each level voltage & current flow path with only active switches presents the mode of operation. The fixed capacitor C_1 & the flying capacitor C_f undergoes charging and discharging through a series-parallel configuration, for voltage boosting operations and it is presented in the Fig.3.

TABLE I
Switching Table

V_L	S_1	S_2	S_3	S_4	S_5	S_6	S_{f1}	S_{f2}	S'_1	S'_6	V_{C1}	V_{Cf}
$2V_{DC}$	1	0	0	1	0	0	0	1	0	1	↓	-
$1.5V_{DC}$	1	0	0	1	0	0	0	1	0	0	↓	↑
$1V_{DC}$	1	1	1	0	0	0	0	1	0	1	↑	-
$0.5V_{DC}$	1	1	0	0	0	0	0	0	0	1	-	↓
$+0$	1	1	1	0	0	0	0	0	0	0	↑	-
-0	0	1	1	0	0	0	0	0	1	0	↑	-
$-0.5V_{DC}$	0	0	1	0	0	1	0	0	1	0	-	↓
$-1V_{DC}$	0	1	1	0	0	1	1	0	1	0	↑	-
$-1.5V_{DC}$	0	0	0	0	1	0	1	0	1	0	↓	↑
$-2V_{DC}$	0	0	0	0	1	1	1	0	1	0	↓	-

0: OFF; 1: ON; ; ↑: Charging; ↓:Discharge;.

B. Operating modes of the Proposed NCBMLI

In the proposed NCBMLI, the switches are considered to be ideal, and the capacitors are assumed to have sufficiently immense values to sustain stable charge and discharge cycles when operating under a purely resistive load. The switching state transition 0 denotes turnoff and 1 denotes as turnon of the switch. $0^+$and 0^-conform to zero level during positive and negative cycle respectively. Switches S_4 & S_5 are the least switching transition, switches S_1, S_6 & their complimentary switches are turned on only once in every half-cycle, which results in reduced switch losses.

1) To generate positive zero voltage, switches S_1, S_2 and S_3 are turned on, while the remaining switches remain off. Similarly, for negative zero voltage generation, switches S'_1, S_2 and S_3 are activated. These switching states are depicted in Fig.2(a) & Fig.2(f).
2) To generate $0.5V_{dc}$, switches S_1, S_2 and S'_6 are switched on, while all other switches remain off. In this state, the capacitor C_f discharges along this path, as illustrated in Fig.2(b).
3) To generate $1V_{dc}$, switches S_1, S_2, S_3, S_{f2}, and S'_6 are turned on, while the remaining switches in off condition. During this process, the capacitor C_1 charges to V_{dc}, as shown in Fig.2(c).
4) To generate $1.5V_{dc}$, switches S_1, S_4 and S_{f2} are switched on, while the remaining switches are in off condition. During this operation, the capacitor C_f charges to $0.5V_{dc}$ & capacitor C_1 discharges V_{dc}, as depicted in Fig.2(d).
5) To generate $2V_{dc}$, switches S_1, S_4, S'_6, and S_{f2} are turned on, while all other switches remain off. In this state, the capacitor C_1 discharges and assists the DC voltage source, as illustrated in Fig.2(e).

Likewise, the voltage levels for the negative cycle are depicted in Fig.2(g) to (j) with combination of source and capacitors. The waveforms corresponding to each operating mode of the proposed inverter is shown in Fig.3.

C. Determination of Fixed & Flying Capacitance

A clear understanding of each switching state and its impact on capacitor voltages is essential, as illustrated in Fig.3. Since fluctuations in capacitor voltage directly affect the quality of the output waveform, a self-regulating mechanism is employed, where capacitors are arranged in parallel during charging and in series during discharging. Capacitor C_1 charges to $\pm V_{dc}$ when connected in parallel with the DC source & discharges during $\pm 1.5V_{dc}$ and $\pm 2V_{dc}$. Similarly, the flying capacitor (C_f) charges at $\pm 1.5V_{dc}$ and discharges at $\pm 0.5V_{dc}$, as shown in Fig.4. Due to the continuous discharge of C_1 during $\pm 1.5V_{dc}$ and $\pm 2V_{dc}$, a slight voltage ripple occurs, whereas C_f undergoes periodic charge-discharge cycles, ensuring voltage stability. It is important to highlight that the charging and discharging processes take place within a single fundamental period of the output voltage. The capacitance of the switched capacitors(SCs) is determined based on the longest discharge duration, peak current, and the maximum allowable voltage ripple ($x\%$). The effective resistive conduc-

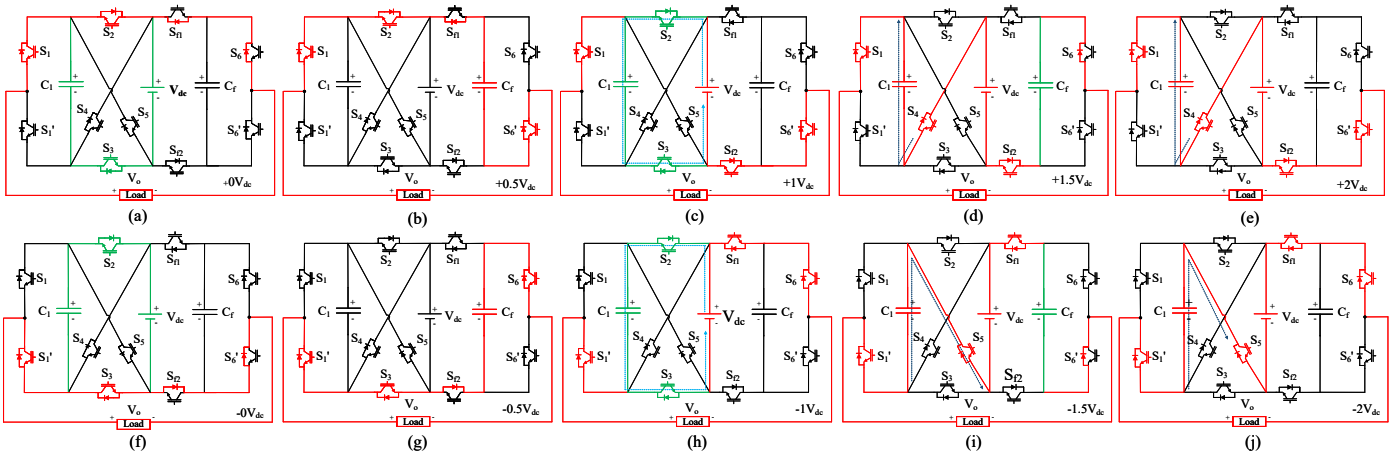

Fig. 2. Operating modes of the proposed NCBMLI(a)0^{+}(b)$0.5V_{dc}$(c)V_{dc}(d)$1.5V_{dc}$(e)$2V_{dc}$(f)0^{-}(g)$-0.5V_{dc}$(h)$-1V_{dc}$(i)$-1.5V_{dc}$(j)$-2V_{dc}$.

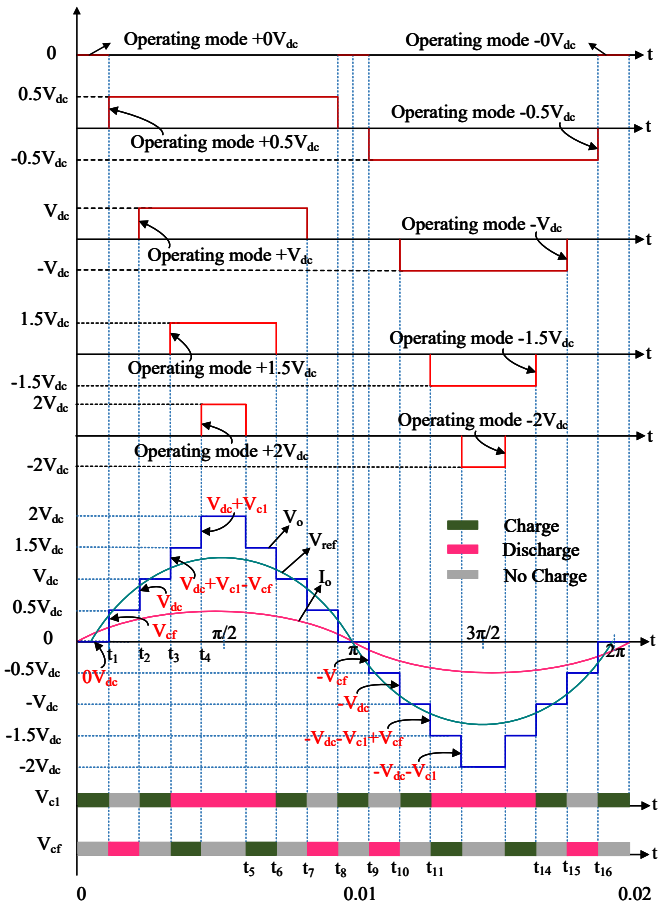

Fig. 3. Waveforms of the corresponding operating modes and 9-level Staircase waveform with capacitor charge and discharge paths.

tion path involved in the capacitor's charging and discharging process is illustrated in Fig.4.

The basic charge-voltage relationship is given as:

$$Q = CV \tag{1}$$

Taking (1) into account, with maximum permissable voltage ripple is set to $x\%$ of the steady-state capacitor voltage, the

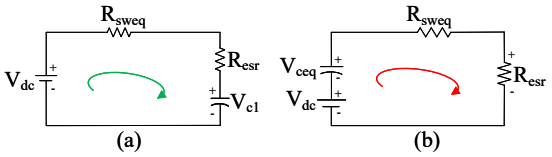

Fig. 4. Equivalent circuit path for (a) Charging & (b) Discharging.

optimal capacitance value for SCs can be represented as follows.

$$C_1 = C_f \geq \frac{\Delta Q}{xV} \tag{2}$$

The discharge period is governed by the load current and the duration of discharge. Considering a full cycle period π the maximum discharge time for capacitor C_1 occurs from t_3 to $\pi - t_3$, while for capacitor C_f, it discharges from t_1 to t_2. The charge variation in C_1 and C_f is derived as follows:

$$Q_{C_1} = 2 \times \int_{t3}^{\pi - t_3} i_o(t)dt = 2 \times \int_{t_{12}}^{2\pi - t_{14}} i_o(t)dt \tag{3}$$

$$Q_{C_f} = 2 \times \int_{t_1}^{t_2} i_o(t)dt = 2 \times \int_{t_9}^{t_{10}} i_o(t)dt \tag{4}$$

where i_o is the peak value of the load current & the time interval is calculated as follows as in (5):

$$\begin{aligned} t_1 &= \frac{\sin^{-1}(1/8)}{2\pi f}\ \text{s} \\ t_2 &= \frac{\sin^{-1}(3/8)}{2\pi f}\ \text{s} \\ t_3 &= \frac{\sin^{-1}(5/8)}{2\pi f}\ \text{s} \\ t_4 &= \frac{\sin^{-1}(7/8)}{2\pi f}\ \text{s} \end{aligned} \tag{5}$$

By using the (2),(3),(4) & (5), the optimal minimum capacitance of the capacitors is calculated with the voltage ripple allowed ($x\%$) for the R load shown in (6):

$$C_1 = \frac{3V_{dc}}{R \times \omega \times xV}(\pi - 2t_3)$$
$$C_f = \frac{V_{dc}}{R \times \omega \times xV}(t_2 - t_1). \quad (6)$$

After determining the capacitance value, it is important to recognize that in switched capacitor inverters, peak currents typically result from the rapid charging and discharging of capacitors through specific switches, causing transient stress on the components. Selecting a suitably large capacitance helps suppress voltage and current ripples, improving waveform smoothness and reducing total harmonic distortion, while low equivalent series resistance further enhances capacitor performance by enabling efficient charge transfer and reducing thermal stress. To complement this, the proposed inverter employs an optimized type-II fuzzy logic switching at fundamental frequency, which reduces redundant switching and associated losses. By intelligently controlling the capacitor charging and discharging sequences, it minimizes current spikes, ensures smoother transitions, and alleviates capacitor stress. The combination of large, low-ESR capacitors with fuzzy logic switching effectively limits ripple, enhances efficiency, and ensures stable performance of the proposed inverter.

III. Modulation Strategy

A. Description of Optimized Type-II Fuzzy Logic Switching

As the number of output levels in the inverter increases, conventional logic gate design become increasingly complex and rigid, preventing modifications. In contrast, Type-II fuzzy logic switching offers a distinctive rule-based membership functions and a set of predefined rules, eliminating the need for fixed logic gate circuitry and enabling reprogrammability for future design adjustments. Among various FLC, the Takagi-Sugeno and Mamdani types are primarily employed for fuzzy switching [23], [24]. This paper primarily leverages the commonly used and computationally efficient Mamdani FLC. As highlighted in the introduction, MFs are defined for both the input and output variables to facilitate effective fuzzy logic control. The input MFs are formulated based on pre-calculated firing angles, determined using techniques such as SQ and HH, which are employed to effectively suppress lower order harmonics in the output waveform. In [25], a type-I fuzzy switching technique was proposed, employing a single MF associated with a specific linguistic variable and operating with a limited rule base of 25 rules. In contrast, this paper introduces an improved type-II fuzzy switching approach that supports up to 49 rules, thereby enhancing control flexibility and system adaptability. Type-II fuzzy switching extends the foundation of type-I fuzzy swicthing by incorporating two MFs: the Upper Membership Function (UMF) and the Lower Membership Function (LMF). While the UMF is analogous to the traditional type-I MF, the LMF is either equal to or less than the UMF. The region enclosed between these two functions, known as the Footprint of Uncertainty (FOU), reflects the level of uncertainty influenced by varying circuit conditions. To effectively capture this behavior, a customized input MF is developed, and its step-by-step design methodology is illustrated in Fig.5(a).

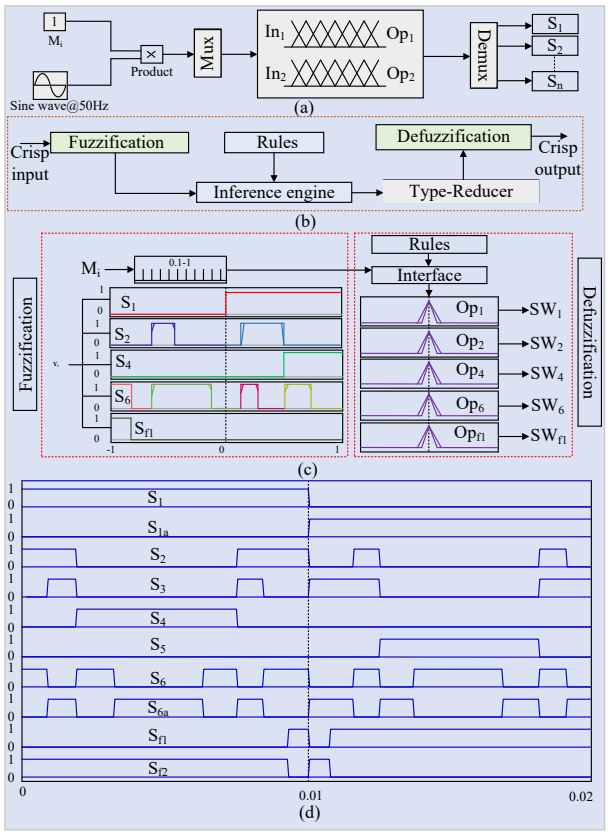

Fig. 5. (a) & (b)Generalized fuzzy logic presentation (c)Rule based fuzzy logic switching for proposed SCMLI (d)Switching pulses from fuzzy logic controller.

FLS comprises of three fundamental stages: fuzzification, inference, and defuzzification, as depicted in Fig.5(b). During the fuzzification stage, MF are assigned to switching variables with magnitudes ranging from –1 to 1, including 0. In the defuzzification stage, output MFs are treated as singletons with an amplitude of 1, facilitating the generation of switching pulses based on the number of inverter switches. The inference engine, as shown in Fig.5(c), processes the fuzzified inputs using a predefined rule base to determine the appropriate switching actions. This fuzzy switching enhances the system robustness while providing precise and adaptive control, particularly under complex and dynamic operating conditions. In contrast to conventional PWM techniques that rely on fixed modulation strategies and static rule sets, FLS offers a model-independent and adaptive solution, effectively addressing the nonlinear behavior inherent in SCMLIs, as outlined in Table II. The proposed FLS method significantly reduces total harmonic distortion and improves voltage balancing across the capacitors. Moreover, by employing an optimized rule set specifically tailored to mitigate the effects of parasitic capacitance, the approach also minimizes switching and leakage losses.

B. Determination of MFs from Optimized Firing Angles

The switching angle marks the transition of output voltage levels. For an m-level output, a total of 2(m-1) switching

TABLE II
COMPARISON OF PROPOSED FLS WITH CONVENTIONAL SWITCHING METHODS

Switching Methods	Control Type	THD Performance	Computation
Conventional PWM	Deterministic & model-based	Generally low THD by tuning precisely	Moderate to high
Proposed FLS	Adaptive & rule-based	Good, depends on rule accuracy	Low to moderate, no heavy computation

angles are required. Due to the symmetry of the NCBMLI waveform in Fig.3, the negative half is a mirror image of the positive half, and the second quarter replicates the first. As a result, the key switching angles for fuzzy logic control lies within 0°-90° and are computed using the SQ and HH methods. This optimized angles are then converted into switching magnitudes, represented as MFs, to enhance inverter performance.

From the SQ method, the desired angles are generated using the quantizer and the sine reference signal i.e, V_{ref}=V_d $*$ $\sin*(2 * \pi * 50 * t)$. The quantizer output waveform is typically a stepped waveform, with each level changing by equal magnitudes consecutively, and it follows as:

$$K = \frac{V_d}{0.5 * (N-1)} \tag{7}$$

$$V_d = \frac{6.5 * e}{\sin(\Phi_m)} \tag{8}$$

$$\sin(\phi_m) = \frac{6.5 \times e}{0.5 \times (N-1) \times K}. \tag{9}$$

The K & e value is calculated based on the number of levels in output voltage & the peak amplitude of the reference signal in (7) are referred from [25]. Angle ϕ_m is calculated using (8) & (9). conversion of switching angles to constant magnitudes is shown in (10) which are utilized as MFs.

$$F_j = M_i * \sin\left(\Phi_m * \frac{\pi}{180}\right) \tag{10}$$

Half-height method uses a simplified sine function to derive the switching angles. Therefore, the generalized formula for evaluating the kth switching angle from HH method is given in (11) & conversion of angles to switching magnitudes is obtained from (12).

$$\beta_k = \sin^{-1}\left(\frac{2i-1}{m-1}\right) \ , where\ i = 1, 2....(m-1)/2 \tag{11}$$

$$Y_l = \frac{\sin(\beta_k)}{\sin(\beta_{\max})}, \tag{12}$$

$$\theta_q = \frac{\phi_m + \beta_k}{2} \tag{13}$$

The angles derived from the SQ and HH methods are averaged as shown in (13) and presented in Table III for $M_i = 1$. In this context, the MFs for fuzzy logic switching are obtained using the SQ and HH methods, with the corresponding switching pulses illustrated in Fig.5(d).

TABLE III
NEW FIRING ANGLES FOR THE PROPOSED NCBMLI

SQ Angles (Φ)	HH Angles (β)	Averaged Angles (θ)	Switching Magnitudes
$\Phi_1 = 6.390$	$\boldsymbol{\beta}_1 = 7.18$	$\theta_1 = 6.785$	0.113
$\Phi_2 = 19.476$	$\boldsymbol{\beta}_2 = 22.024$	$\theta_2 = 20.750$	0.343
$\Phi_3 = 33.740$	$\beta_3 = 38.682$	$\theta_3 = 36.211$	0.561
$\Phi_4 = 51.066$	$\boldsymbol{\beta}_4 = 61.04$	$\theta_4 = 56.053$	0.790

IV. COMPARATIVE STUDY

A comparative study between the proposed NCBMLI and former MLI topologies with single DC-source has been presented in this section.

Table IV presents a comparative study, highlighting key parameters such as the number of switches (N_{sw}), diodes (N_D), capacitors (N_C), gate drivers (N_{GD}), maximum boost voltage (MBV), total standing voltage (TSV), cost factor (CF) and efficiency. The table clearly demonstrates that the proposed inverter operates with only 10 switches. While topologies in [13], [14] and [19] also use the same number of switches, but they rely on additional diodes and capacitors to achieve a nine-level output in which it results high CF. Significantly, all the SCMLIs presented in comparison table utilizes a single DC source and generates 9-level output voltage. The SCMLIs presented in [10], [11], [15], [17]–[20] are four-fold voltage gain inverters with increased component count, resulting in higher TSV and CF. Even though the MLIs in [10], [11], [15] are operated at low switching frequency but due to higher component count they offer lower efficiency when compared with the proposed NCBMLI.

In SCMLI designs, capacitors are the second most critical components in terms of reliability and their count should be minimized. Among the various two and four boost MLI topologies presented in the comparison, the proposed NCBMLI achieves the lowest number of capacitors (N_C). Although SCMLIs in [11]–[13], [15], [18], [21] also utilize an equal number of capacitors, but their increased switch count and reliance on high switching frequencies lead to higher TSV, elevated switch losses and reduced overall efficiency. The proposed NCBMLI achieves MBV of 2, while the presented two boost MLIs in [12]–[14], [16], [21] requires more component count, leading to an increase in the TSV and overall CF whereas the proposed one achieves low TSV,CF. Among all the MLI topologies, [20] shows the highest TSV, along with the more number of switches, capacitors and high switching frequency. The TSV is determined in(14).

$$TSV = \sum_{i=1}^{N_{sw}} V_{sw,i} \tag{14}$$

TABLE IV
COMPARISON OF THE PROPOSED NCBMLI WITH EXISTING SCMLI TOPOLOGIES

Topology	N_L	N_{SW}	N_D	N_C	N_{GD}	MBV	TSV	Cost Factor (pu) $\alpha = 0.5$	Cost Factor (pu) $\alpha = 1$	η (%)	Frequency (Hz/kHz)
[10]	9	11	2	3	11	4	28	2.16	3.22	95.64	50Hz
[11]	9	11	1	2	11	4	28	1.94	2.33	96.37	50Hz
[12]	9	13	–	2	13	2	15	2.08	2.50	96.05	2kHz
[13]	9	10	2	2	10	2	15	1.97	2.38	97.12	50Hz
[14]	9	10	2	3	10	2	13	2.02	2.38	–	5kHz
[15]	9	11	1	2	11	4	27	1.93	2.30	90.90	50Hz
[16]	9	8	2	3	8	2	13	1.81	2.16	96.40	2kHz
[17]	9	12	–	3	12	4	28	2.05	2.44	97.30	20kHz
[18]	9	12	–	2	12	4	28	1.94	2.34	–	5kHz
[19]	9	13	–	3	13	4	29	2.18	2.58	97.60	5kHz
[20]	9	16	4	4	16	4	24	2.50	3.30	–	5kHz
[21]	9	10	1	2	10	2	15	1.80	2.16	–	50Hz
Proposed	9	10	–	2	10	2	10	1.61	1.88	97.82	50Hz

N_L = Number of output levels; N_{SW} = Number of switches; N_D = Number of diodes; N_C = Number of capacitors; N_{GD} = Number of gate drivers; MBV = Maximum boost voltage; TSV = Total standing voltage; η = Efficiency.

In contrast, the proposed inverter achieves the lowest CF, making it the most economically efficient option among the compared circuits. The per unit cost factor for all the MLI topologies discussed in this paper is determined using (15), where α is the weightage factor and it accurately represents the genuine contribution of each component to the overall cost or complexity, rather than merely summing all components uniformly.

$$CF_{pu} = \frac{N_{sw} + N_D + N_C + (\alpha * TSV/MBV)}{N_L} \tag{15}$$

Moreover, the multilevel inverters outlined in the comparison table predominantly utilize low & high-frequency PWM control techniques, while also depending on logic gate-based architectures for their switching operations. In contrast, the proposed NCBMLI utilizes fuzzy logic switching. The comparison table clearly demonstrates that the proposed inverter reduces the number of switches and capacitors, minimizes TSV and CF, while maintaining low switching frequency operation and enhancing overall efficiency. Fig.6(a) & 6(b) shows the bar graph comparing the component count v/s topologies and TSV, CF v/s topologies presented in the comparison table.

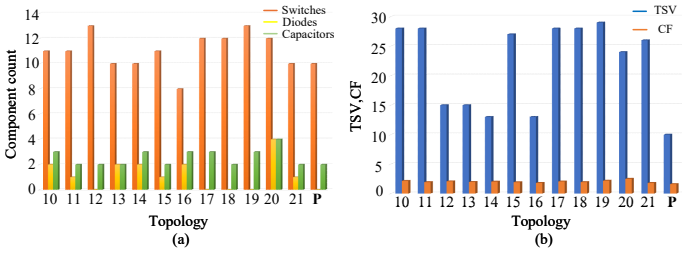

Fig. 6. Comparison of the proposed inverter with existing MLI topologies in (a) Number of component count v/s MLI topologies & (b) TSV, CF v/s MLI topologies.

V. POWER LOSS DISTRIBUTION & EFFICIENCY

The loss analysis and efficiency calculations has been conducted in this section to evaluate the performance of the proposed NCBMLI. The primary loss components in the proposed NCBMLI includes switching losses(P_{sw}), conduction losses(P_{cd}) & Capacitor ripple loss($P_{C_{rip}}$).

A. Switch Loss and Conduction Loss

Switch losses arise during the rapid changes of power switches between their ON and OFF states. The losses are predominantly affected by factors such as the switching frequency, the magnitude of the load current, and the voltage impeded by the device during switching, as presented in (16). Conduction losses occur due to the continuous current flow through semiconductor switches and passive components during their ON-state operation as determined in (17).

$$P_{\text{sw}} = \sum_{i=1}^{N_s} f_{sw,i} \cdot V_{sw,i} \cdot I_{sw,i} \cdot (t_{on,i} + t_{off,i}) \tag{16}$$

$$P_{\text{cond}} = \sum_{i=1}^{N_s} I_{rms,i}^2 \cdot R_{on,i} + \sum_{j=1}^{N_d} V_{o,j} \cdot I_{dc,j} \tag{17}$$

B. Capacitor Ripple Loss

Furthermore, the ripple current and the internal resistance of the capacitors generate power losses in the inverter. The charging phase exhibits a voltage ripple resulting from a disparity between the capacitor voltage and the input supply, causing energy dissipation, as depicted in (18):

$$P_{C_{rip}} = \frac{f_{ref}}{2} \left(C_1 \times xV_{C_1}^2 + C_f \times xV_{C_f}^2 \right) \tag{18}$$

Therefore, the total losses are expressed as P_{Tl} in (19):

$$P_{Tl} = P_{\text{sw}} + P_{\text{cond}} + P_{C_{rip}} \tag{19}$$

Further, Fig.7(a) illustrates the power loss distribution, while Fig.7(b) displays the power versus efficiency curve.

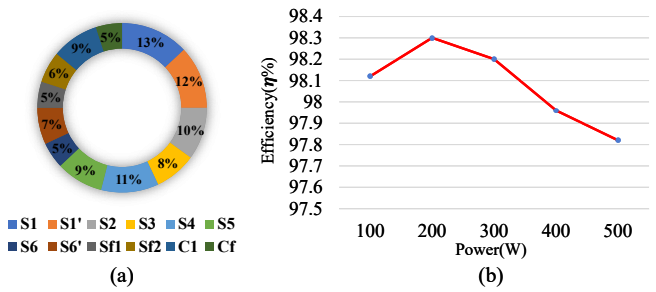

Fig. 7. (a) Power loss distribution of the Switches & Capacitors & (b) Power v/s Efficiency Curve.

VI. Experimental Results

A scaled-down prototype of the proposed inverter is shown in Fig.8. The proposed NCBMLI operates with a DC supply of $V_{dc} = 50V$, and all circuit attributes used for experiment are listed in Table V. The proposed NCBMLI is built using IGBTs(SKM75GB07E3) as switching devices. The on-state resistance values for the IGBT, antiparallel diode and regular diode are determined by analyzing their performance characteristics extracted from the respective datasheet. The junction-to-case thermal resistance, typically around 0.26K/W, enables effective heat dissipation and allows the device to withstand short-circuit events for up to $6\,\mu$s at a maximum junction temperature of $150°$C, thereby ensuring reliable operation under both steady-state and transient load conditions. Additionally, the integrated antiparallel freewheeling diode supports high-speed switching with reduced reverse recovery losses. The gate pulses for the switches are generated using the OpalRT(OP4200) controller. A TLP350 gate driver board is utilized to drive the pulses for the proposed inverter.

TABLE V
Experimental Parameters

Components/parameters	Value
DC voltage (V_{dc})	50 V
Switches	SKM75GB07E3, 600V, 75A, 1.09 mΩ
Capacitor (C_1)	2200μF, 100V
Capacitor (C_F)	1100μF, 50V
Switching frequency	50HZ
Controller	OpalRT(OP4200)
Gate-driver	TLP350
Output frequency	50Hz
Load resistance & inductance	R=50 Ω & L=120mH

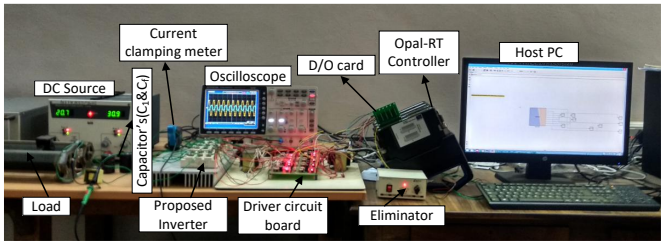

Fig. 8. Hardware setup of the proposed NCBMLI.

Fig.9, presents the hardware validation of the proposed NCBMLI under various dynamic load conditions and modulation indices (M_i). The output voltage exhibits a uniform 9-level stepped waveform, which confirms the capacitor's voltage-boosting capability. Fig.9(a) presents the output voltage and current waveforms for an R-load, along with the respective capacitor voltage profiles, confirming stable and consistent operation. The rms voltage is observed to be 70.72 v and the current is 1.49A. Fig.9(b) depicts the corresponding voltage, current and capacitor waveforms under an inductive load, demonstrating the inverter's reliable performance under RL-load conditions with rms voltage as same in R-load and the current is 1.69A. From this result it is observed that the current lags the voltage with increased magnitude, confirming its effective operation with inductive loads. Later, Fig.9(c) & (d) illustrate the load transitions from R-load to RL-load and vice versa, showing that the capacitor voltages remain unaffected. This indicates that the proposed NCBMLI maintains improved voltage and current waveforms under RL-load conditions compared to pure R-load. Moreover, the current remains well regulated without significant overshoot or distortion, confirming the stable operation of the inverter during load transitions.

Furthermore, the impact of modulation index (M_i) transitions from 0.3 to 1 is shown in Fig.9(e) to (g). Specifically, Fig.9(e) captures the transition from $M_i = 0.3$ to 0.5, where the output voltage shifts from a 3 to 5-level waveform, along with corresponding changes in current magnitude. Fig.9(f) illustrates the transition from $M_i = 0.5$ to 0.7, resulting in a 5 to 7-level voltage shift and corresponding current variations. Fig.9(g) presents the waveforms for M_i increasing from 0.7 to 1, where the output transitions from a 7 to 9-level voltage waveform. This indicates that the proposed inverter can consistently produce output voltage without disruption, ensuring an uninterrupted current supply to the load. Significantly, capacitor voltages remain stable despite these changes in M_i. Moreover, at lower modulation index, the inverter continues to operate with an output voltage equal to the input voltage, confirming its superior performance. Finally, Fig.9(h) to (j) presents the voltage stress across the switches of the proposed inverter and it is observed that all the switches operate well within their rated limits, confirming optimized voltage distribution, reduced switching losses, and improved overall efficiency of the inverter. Furthermore, Fig.10(a) & (b), presents the capacitor voltage and current waveforms of the proposed NCBMLI under resistive and inductive load conditions. The ripple RMS current of capacitor C_1 is observed to be 3.53A, while the RMS current through the flying capacitor C_f is measured as 5.62A. These results confirm that the current ripple of the capacitor is observed to be within acceptable limits, ensuring stable circuit performance without adverse effects and enhanced durability of the proposed NCBMLI under resistive and inductive load conditions.

Moreover, the proposed NCBMLI achieves a maximum efficiency of 97.82% at rated power of 500W, demonstrating its suitability for energy-efficient applications with low power loss. The measured output voltage and current THD values are 5.83% and 1.85%, respectively, at a modulation index of

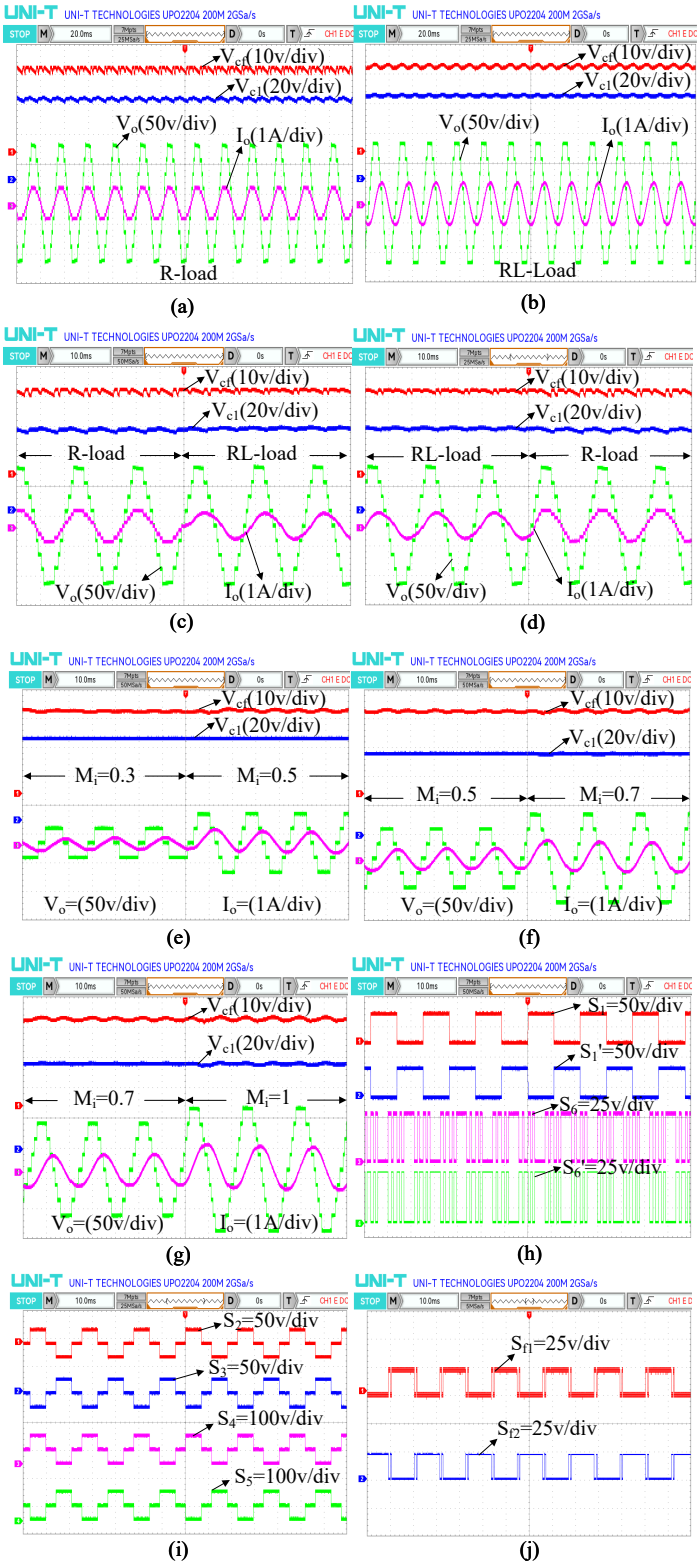

Fig. 9. Experimental results of the proposed NCBMLI (a) O/p voltage & current with capacitor voltages for R-load (b) for RL-load (c) Transition from R-load to RL-load(d) RL-load to R-load (e)M_i variation from 0.3-0.5 (f)M_i=0.5 to 0.7 (g)From M_i=0.7 to 1 (h)-(j) voltage stress across the switches.

1, which comply with the IEEE standards, as illustrated in Fig.11(a) and 11(b). Further, the variation of output voltage

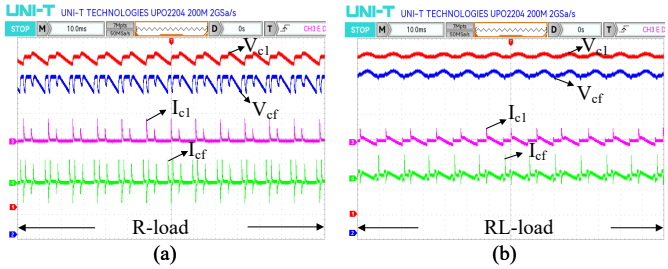

Fig. 10. Capacitor ripple voltage and current waveforms (a) R-load & (b) RL-load.

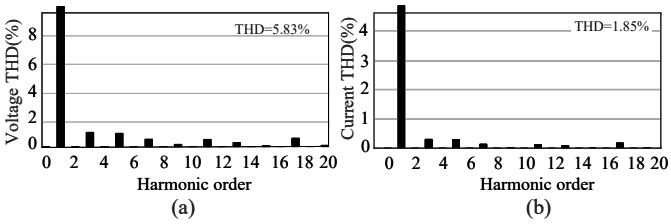

Fig. 11. THD of the proposed inverter (a) Output Voltage & (b) Output current.

THD with respect to the modulation index is illustrated in Fig.12. At the lowest modulation index of 0.1, the THD is substantially high at 52.27%. As the modulation index increases to 0.5, the THD drops to 13.56%. With further increase of the modulation index to unity, the THD is minimized to 5.83%. This demonstrates that the proposed inverter topology achieves a high quality output voltage waveform with reduced harmonic distortion. Therefore, the experimental results confirm the successful hardware implementation of the proposed NCBMLI.

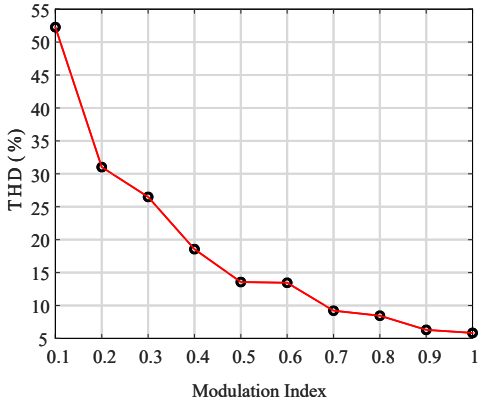

Fig. 12. variation of THD with respect to different modulation indices.

VII. Conclusion

A novel NCBMLI has been proposed, featuring a compact design with a reduced number of components. The operational modes of the proposed inverter are thoroughly analyzed, including detailed current paths for each voltage level and the corresponding capacitor charging and discharging sequences. An optimized type-II fuzzy logic switching strategy was implemented, employing sine quantizer and half height methods

to determine optimal firing angles. Further, the obtained angles are averaged and converted into constant magnitudes, which served as membership functions for fuzzy switching. A comprehensive comparison study highlighted the superiority of the proposed NCBMLI over conventional SCMLIs, emphasizing significant reductions in both the number of switches and capacitor count, which resulted in achieving the lowest total standing voltage and costfactor. In addition, it minimizes losses and delivers superior efficiency. The experimental validation of the proposed NCBMLI was carried out under various load conditions to assess its effectiveness, and the key advantages of the proposed inverter are as follows:

1) The proposed inverter validated at different load conditions, such as R, RL, and R-RL loads, confirming the stable performance with well-regulated voltage and current waveforms.
2) Tests performed at varying modulation indices confirmed the generation of higher voltage levels, resulting in output waveforms that closely resemble sinusoidal and improved overall performance.
3) The monitored voltage stress across switches remained within safe operating limits during all switching transitions.
4) Furthermore, the use of optimal value capacitors effectively minimized voltage ripples and enhanced the dynamic response across different load variations.
5) The proposed NCBMLI achieved a peak efficiency of 97.82%, demonstrating its suitability for practical applications, while maintaining low harmonic distortion with output voltage and current THD of 5.83% and 1.85%, respectively.

REFERENCES

[1] L. Tapia Hector Jua, A. Rodriguez Jose Juan, D. Gonzalez Aurelio, and R. Resendiz Juvenal, "Eight levels multilevel voltage source inverter modulation technique," *IEEE Latin America Transactions*, vol. 16, DOI 10.1109/TLA.2018.8362146, no. 4, pp. 1121–1127, 2018.

[2] V. L, G. K. S, M. Rivera, and E. Babaei, "Performance enhancement of reduced component multilevel inverter with optimal placement of level shifter," *IEEE Latin America Transactions*, vol. 22, DOI 10.1109/TLA.2024.10534310, no. 6, pp. 502–511, 2024.

[3] T. Bruckner, S. Bernet, and H. Guldner, "The active npc converter and its loss-balancing control," *IEEE Transactions on Industrial Electronics*, vol. 52, DOI 10.1109/TIE.2005.847586, no. 3, pp. 855–868, 2005.

[4] N. Yalla, N. Babu A, and P. Agarwal, "A new three-phase multipoint clamped 5l-hpfc with reduced psd count and switch stress," *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2910030, no. 4, pp. 2532–2543, 2020.

[5] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, DOI 10.1109/TIE.2009.2030767, no. 7, pp. 2197–2206, 2010.

[6] B. N. Rao, Y. Suresh, A. K. Panda, B. S. Naik, and V. Jammala, "Development of cascaded multilevel inverter based active power filter with reduced transformers," *CPSS Transactions on Power Electronics and Applications*, vol. 5, DOI 10.24295/CPSSTPEA.2020.00013, no. 2, pp. 147–157, 2020.

[7] R. Barzegarkhoo, M. Forouzesh, S. S. Lee, F. Blaabjerg, and Y. P. Siwakoti, "Switched-capacitor multilevel inverters: A comprehensive review," *IEEE Transactions on Power Electronics*, vol. 37, DOI 10.1109/TPEL.2022.3164508, no. 9, pp. 11 209–11 243, 2022.

[8] F. B. Grigoletto, "Space vector modulation for three-phase multilevel switched-capacitor inverter," *IEEE Latin America Transactions*, vol. 19, DOI 10.1109/TLA.2021.9448540, no. 4, pp. 575–583, 2021.

[9] A. K. Yadav, K. Gopakumar, K. R. R, L. Umanand, S. Bhattacharya, and W. Jarzyna, "A hybrid 7-level inverter using low-voltage devices and operation with single dc-link," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2018.2890371, no. 10, pp. 9844–9853, 2019.

[10] D. Kumar, R. Raushan, M. W. Ahmad, and S. Dutta, "A novel single source bridgeless nine-level switched-capacitor-based quadruple boost inverter with reduced voltage stress," *IEEE Access*, vol. 12, DOI 10.1109/ACCESS.2024.3480322, pp. 152 183–152 195, 2024.

[11] G. Dhasharatha, M. H. Khan, and B. Mangu, "A novel nine-level quadruple boost inverter for electric vehicle applications," *IEEE Access*, vol. 12, DOI 10.1109/ACCESS.2024.3393846, pp. 60 694–60 704, 2024.

[12] Z. Xun, H. Ding, Z. He, W. Zhou, and Y. Zheng, "A single-phase switched-capacitor nine-level inverter with reduced capacitance," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, DOI 10.1109/JESTPE.2022.3186926, no. 6, pp. 7410–7421, 2022.

[13] M. Jagabar Sathik, N. Sandeep, D. Almakhles, and F. Blaabjerg, "Cross connected compact switched-capacitor multilevel inverter (c3-scmli) topology with reduced switch count," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, DOI 10.1109/TCSII.2020.2988155, no. 12, pp. 3287–3291, 2020.

[14] M. Daula Siddique, M. Aslam Husain, A. Iqbal, S. Mekhilef, and A. Riyaz, "Single-phase 9l switched-capacitor boost multilevel inverter (9l-sc-bmli) topology," *IEEE Transactions on Industry Applications*, vol. 59, DOI 10.1109/TIA.2022.3208893, no. 1, pp. 994–1001, 2023.

[15] K. Varesi, F. Esmaeili, S. Deliri, and H. Tarzamni, "Single-input quadruple-boosting switched-capacitor nine-level inverter with self-balanced capacitors," *IEEE Access*, vol. 10, DOI 10.1109/ACCESS.2022.3187005, pp. 70 350–70 361, 2022.

[16] W. Lin, J. Zeng, J. Hu, and J. Liu, "Hybrid nine-level boost inverter with simplified control and reduced active devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, DOI 10.1109/JESTPE.2020.2983205, no. 2, pp. 2038–2050, 2021.

[17] Y. Nakagawa and H. Koizumi, "A boost-type nine-level switched capacitor inverter," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2018.2876158, no. 7, pp. 6522–6532, 2019.

[18] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and K. Vijayakumar, "Switched-capacitor-based quadruple-boost nine-level inverter," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2019.2898225, no. 8, pp. 7147–7150, 2019.

[19] J. Yao, Z. Zhang, X. Zheng, and A. Ioinovici, "A common ground switched-capacitor multilevel inverter with a low component count," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 60, DOI 10.1109/TAES.2024.3370895, no. 4, pp. 3779–3791, 2024.

[20] H. Khoun Jahan, M. Abapour, and K. Zare, "Switched-capacitor-based single-source cascaded h-bridge multilevel inverter featuring boosting ability," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2018.2830401, no. 2, pp. 1113–1124, 2019.

[21] K. Aditya, Y. Suresh, B. S. Naik, B. N. Rao, and A. K. Panda, "A novel quadruple boost inverter with new optimized fuzzy-based switching scheme," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, DOI 10.1109/TCSII.2023.3306742, no. 1, pp. 171–175, 2024.

[22] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of modulation and control techniques for multilevel inverters in traction applications," *IEEE Access*, vol. 9, DOI 10.1109/ACCESS.2021.3056612, pp. 24 187–24 204, 2021.

[23] A. A. Stonier, S. Murugesan, R. Samikannu, V. Krishnamoorthy, S. K. Subburaj, G. Chinnaraj, and G. Mani, "Fuzzy logic control for solar pv fed modular multilevel inverter towards marine water pumping applications," *IEEE Access*, vol. 9, DOI 10.1109/ACCESS.2021.3090254, pp. 88 524–88 534, 2021.

[24] S. Ranjan Das, A. Kumar Mishra, A. K. Sahoo, A. Prasad Hota, W. Viriyasitavat, N. Saleh Alghamdi, and G. Dhiman, "Fuzzy controller designed-based multilevel inverter for power quality enhancement," *IEEE Transactions on Consumer Electronics*, vol. 70, DOI 10.1109/TCE.2024.3389687, no. 2, pp. 4839–4847, 2024.

[25] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "Design and development of a novel 19-level inverter using an effective fundamental switching strategy," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, DOI 10.1109/JESTPE.2017.2776294, no. 4, pp. 1903–1911, 2018.

Eddu Karunakaran received his B.Tech. degree in Electrical & Electronics Engineering from Sri Venkateswara University Tirupati, in 2018 and M.Tech degree in Electrical Engineering from NIT Raipur in 2021. currently he is persuing Ph.D degree in Electrical & Electronics Department from National Institute of Technology Karnataka, Suarthkal, India. His current research interests include Multilevel inverters, power electronics, Power systems.

Yellasiri Suresh received the B.Tech. degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Anantapur, India, in 2004, and the M.Tech. and Ph.D. degrees in Power Control and Drives from the National Institute of Technology (NIT), Rourkela, India, in 2009 and 2013, respectively. Since 2015, he has been with the Department of Electrical and Electronics Engineering at the National Institute of Technology Karnataka (NITK), Surathkal, Mangalore, where he is currently serving as an Associate Professor. He has supervised five Ph.D. scholars and has authored or co-authored over 50 research publications in reputed international journals and conferences, including those published by IEEE, IET, Elsevier, and Springer. His research interests include multilevel inverters, power quality improvement in power systems, and control of electric drives.

Kancharapu Aditya received the B.Tech. degree in electrical and electronics engineering from Andhra University, India, in 2013 and the M.Tech. degree in power and energy systems from National Institute of Technology Karnataka, Surathkal, India, in 2016. He received a Ph.D. degree from the Department of Electrical and Electronics Engineering, National Institute of Technology Karnataka, Surathkal, India, in 2023. He is currently working in Alten Global Technologies Pvt Ltd (AGTSPL) as a technical Leader Systems, Bangalore, Karnataka, India. His current research interests include multilevel converters and High voltage DC-DC converters.

Bhukya Nageswar Rao received his B.Tech. degree in Electrical & Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2010 and M.Tech. degree in power electronics from National Institute of Technology Calicut, Kerala, India, in 2013, and the Ph.D. degree in Multilevel converters and its applications from National Institute of Technology, Karnataka, India, in 2023. He is currently working as assistant professor at the Department of Electrical Engineering, Dr B R Ambedkar National Institute of Technology, Jalandhar, Punjab, India. His current research interests include Multilevel inverters and power quality improvements in power systems.