A Soft-switched Induction Cooking System with Reduced Switch Count and Independent Control for Multiple Loads

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***Abstract*—In this paper, a three-load resonant inverter (3LRI) with independent power control is proposed for induction cooking (IC) applications. Resonant inverter circuits are commonly employed in induction cookers due to their superior efficiency and capability for soft switching operation. Among the various topologies, the half-bridge series resonant inverter (HBSR) topology is used for its optimal balance between performance and cost. The major advantages of this inverter circuit with cyclic ON and OFF control include simple, independent power control for every load, high efficiency for wide range of power variations, soft-switching and reduced number of switches per load. This configuration can be easily extended for multiple loads by addition of another inverter legs. This configuration has been simulated using PSIM software. A 629 W experimental prototype is built to verify the theoretical analysis. A peak efficiency of 96.1% is obtained. The experimental results confirm that this inverter configuration is a viable approach for multi-load induction cooking applications.**

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***Index Terms*—Induction cooking (IC), multi-output series resonant inverter, cyclic ON and OFF control, zero voltage switching (ZVS).**

I. Introduction

INDUCTION heating (IH) has emerged as an alternative to traditional heating methods due to its numerous advantages, such as high efficiency, precise power control, rapid heating, and enhanced safety measures [1], [2]. This technique is widely used in both industrial [3] and domestic applications [4]. Unlike conventional heating methods that often lead to uneven and slow heating, resulting in longer production times and increased energy consumption, IH offers a more versatile solution. It utilizes a resonant inverter [5] to generate high-frequency (HF) flux, which induces eddy currents and thereby heating the load material. The depth of HF current penetration into the material is influenced by the skin depth (δ), which is expressed as

$$\delta = \sqrt{\frac{\pi}{\mu f_{sw}}} \tag{1}$$

Hence, δ is affected by the operating frequency (f_{sw}), magnetic permeability (μ), and resistivity (ρ) of the material.

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Generally, in IH applications, the inverter is operated at frequencies ranging from 20 kHz to 100 kHz [6], [7]. The literature presents various resonant inverter topologies including half-bridge [8], full-bridge [9] and single-ended [10]. The inverter output power can be regulated using either variable or constant frequency methods. Variable frequency control techniques can present challenges such as electromagnetic interference (EMI), noise and reduced efficiency. Constant frequency control methods which include asymmetrical duty cycle control (ADC) [11], [12], phase shift control (PSC) [13], pulse density modulation (PDM) control [14]-[17], asymmetrical voltage cancellation control (AVC) [18]-[20] and cyclic ON and OFF control [21] provide effective solutions.

In IC applications, multi-output resonant inverters [22], [23] are the preferred choice for efficient and cost-effective operation. These inverters offer several advantages, including reduced component count, independent power control, high efficiency and high-power density. A series resonant inverter with a single resonant capacitor has been proposed to power two loads in [24]. This topology requires more switches, leading to higher gate driver demands and design cost. A half-bridge inverter with parallel connected loads is proposed in [25]. In this configuration, each load is controlled by a series switch, but the overall design cost is higher due to the increased number of switching components. A full-bridge topology using an additional leg with two switches using AVC control has been proposed in [26]. A dual half- bridge configuration with single resonant capacitor using PS control has been proposed for two loads in [27]. A three-level series resonant inverter with multiple outputs has been introduced in [28] to minimize total harmonic distortion (THD) and switch voltage stress. A three-leg inverter with PS control for multiple load applications has been proposed in [29]. However, only partial independent power control is possible. A half-bridge resonant converter for multiple vessel induction cooktops with buck-boost capabilities has been presented in [30]. This converter configuration operates at a constant frequency which employs ADC control to regulate power in both loads. A two load three-leg inverter configuration with PDM control has been proposed in [31]. In [32], a four-load series resonant inverter topology has been proposed. It uses hybrid power control and the device count is high. In [33], an inverter configuration has been proposed to power two loads with ON and OFF control. However, it employes a greater number of circuit components including free-wheeling diodes which may lead to more power loss. A three-switch inverter topology with ADC control has been

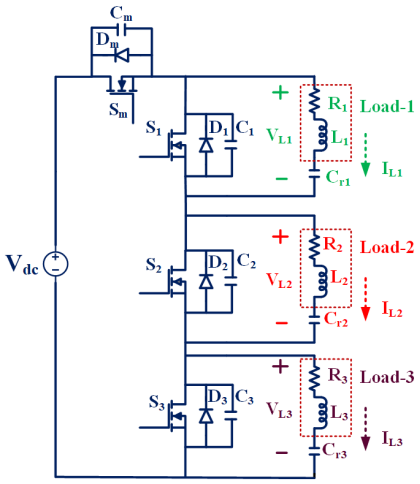


Fig. 1. Proposed three load resonant inverter.

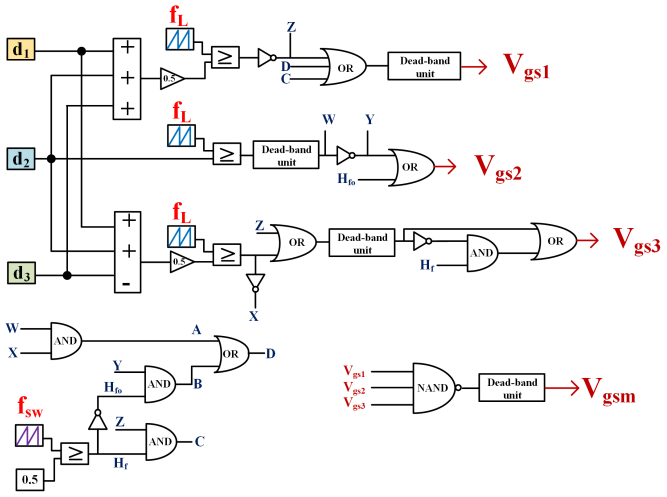


Fig. 2. Proposed control logic.

proposed in [34] for two loads. However, this configuration requires two additional split capacitors, which increases the overall component count. A full-range ZVS control strategy for a dual-port LLLC induction heating system has been proposed in [35]. A combination of dual-phase-shift (DPS) control is used for heavy loads and frequency-doubling pulse frequency modulation (FD-PFM) is used for light loads to ensure smooth power regulation. In [36], a constant-frequency duty cycle-controlled full-bridge inverter is designed for five-load induction cooking applications. This topology achieves a maximum efficiency of 92.7% using phase-shift control for one load and duty-cycle control for the remaining loads. A non-resonant full-bridge multi-output inverter topology for domestic induction heating applications has been proposed in [37]. PDM and pulse frequency modulation (PFM) control techniques are used to achieve independent power control for multiple loads. The SiC-based full-bridge series resonant inverter for domestic induction cooking applications has been proposed in [38]. SiC devices are more expensive than Si-based MOSFETs, which may increase the overall cost of the system.

However, these topologies suffer from one or many of the following limitations: high component count, low efficiency and lack of independent control. Considering the above, a three load resonant inverter (3LRI) topology is proposed in this paper. The proposed inverter is designed with only four switches with three loads powering capability which reduces component count. It is operated with cyclic ON and OFF control where any two loads are powered at a time. The key features of the proposed topology includes

1) An inverter configuration which can power three IH loads.
2) Independent power control for each load.
3) High efficiency (96.1%) for wide range of power variations.
4) Reduced number of devices per load.
5) Wider range of ZVS.
6) Easier extension for multiple loads by addition of another inverter leg.

This paper is divided into the following sections: Section II presents a detailed description of the proposed inverter operation at various modes. Section III describes the design aspects and output power control of the inverter. Section IV explains the simulation and experimental results of the proposed topology. Finally, conclusions are discussed in Section V.

II. Proposed Inverter Configuration

A. Circuit Description

The proposed inverter topology for multiple loads with cyclic ON and OFF control is presented in Fig. 1. It consists of a dc source (V_{dc}) and four switching devices S_m, S_1, S_2 and S_3. D_m, D_1, D_2 and D_3 are the body diodes of MOSFETs. C_m, C_1, C_2 and C_3 are the snubber capacitors. Three identical iron vessels are used as IH loads. R_1, R_2 and R_3 are equivalent resistances and L_1, L_2 and L_3 are equivalent inductances of IH coil-1, 2 and 3 with cooktops respectively. C_{r1}, C_{r2} and C_{r3} are the resonant capacitors for IH loads 1, 2 and 3 respectively. V_{L1}, V_{L2} and V_{L3} are the voltages across the resonant loads 1, 2 and 3 respectively. I_{L1}, I_{L2} and I_{L3} are the respective currents flowing through them. The resonant frequency of the loads are f_{r1}, f_{r2} and f_{r3}.

where,

$$\left.\begin{aligned} f_{r1} &= \frac{1}{2\pi\sqrt{L_1 C_{r1}}} \\ f_{r2} &= \frac{1}{2\pi\sqrt{L_2 C_{r2}}} \\ f_{r3} &= \frac{1}{2\pi\sqrt{L_3 C_{r3}}} \end{aligned}\right\} \quad (2)$$

As identical loads are considered $f_{r1} = f_{r2} = f_{r3} = f_r$. The switching frequency f_{sw} is selected to be slightly greater than f_r in order to provide ZVS.

The proposed inverter control logic is shown in Fig. 2. The load duty cycles d_1, d_2 and d_3 are decided based on the required load powers as described in Sections II & III. A combined duty ratio $(d_1+d_2+d_3)/2$ is compared with a low-frequency reference signal f_L, and the resulting signal

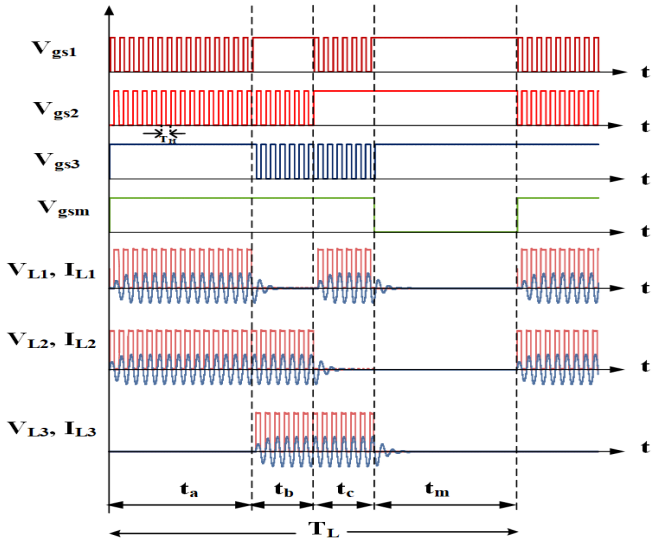


Fig. 3. Gate pulses of the proposed inverter for different duty cycles.

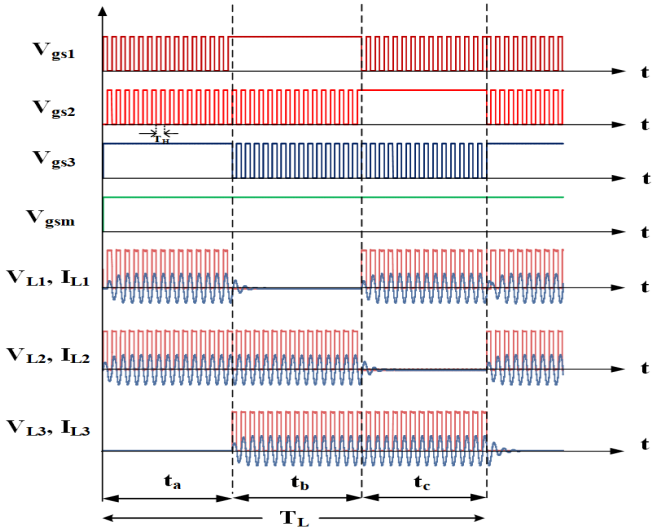


Fig. 4. Gate pulses of the proposed inverter at d_1=d_2=d_3=2/3.

is inverted and logically combined with auxiliary control inputs C and D through a three-input OR gate to produce gating pulse V_{gs1}. Similarly, d_2 is compared with f_L, and the inverted output is ORed with the high-frequency signal H_{fo} to produce V_{gs2}. The third gating pulse V_{gs3} is derived from $(d_1+d_2-d_3)/2$ compared with f_L, logically processed with the signal Z, and combined with H_f signal through OR and AND operations. The three pulses V_{gs1}, V_{gs2} and V_{gs3} are further combined using a NAND gate to obtain the final signal V_{gsm}. A dead-band circuit is provided for all gating pulses to mitigate switching overlap and ensure reliable inverter operation.

B. Operating Principle

The switching pulses V_{gs1}, V_{gs2}, V_{gs3} and V_{gsm} for devices S_1, S_2, S_3, and S_m respectively are shown in Fig. 3 along with the corresponding load voltages and currents when the loads are controlled independently at different duty cycles.

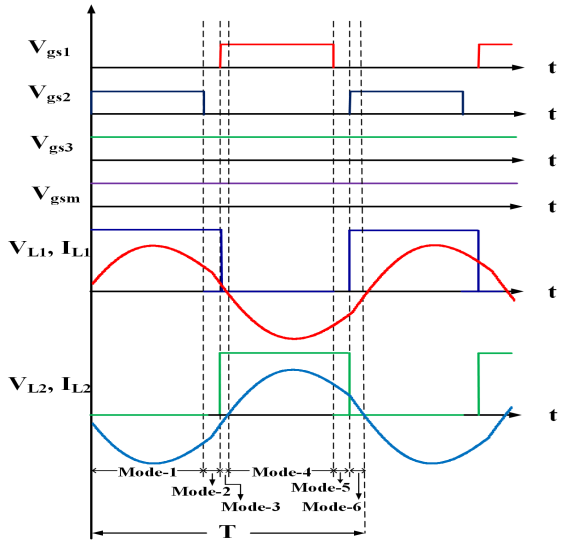


Fig. 5. Operational waveform of proposed inverter.

The loads are controlled independently with cyclic control. The cyclic load control is applied at a low frequency of f_L= 1kHz. S_1, S_2 and S_3 are operated at high frequency f_{sw} = 43 kHz. T_L= $\frac{1}{f_L}$ where,T_L indicates the time period of cyclic control duration. t_a denotes the time duration for which load-1 and load-2 are powered. t_b denotes the time duration for which load-2 and load-3 are powered. t_c denotes the time duration for which load-1 and load-3 are powered. During t_m, S_m is OFF and hence no load is powered. The duty cycles for load-1, load-2 and load-3 are expressed as

$$\left.\begin{aligned} d_1 &= \frac{t_a + t_c}{T_L} \\ d_2 &= \frac{t_a + t_b}{T_L} \\ d_3 &= \frac{t_b + t_c}{T_L} \end{aligned}\right\} \tag{3}$$

In Fig. 3 waveforms are shown for different duty cycles d_1 = d_2 = 0.5, d_3 = 0.1. Fig. 4 shows the gate pulses and corresponding load voltages and currents under equal duty cycle condition where d_1 = d_2 = d_3 = (2/3). Now the output power of each load is $(2P_m)/3$. Where P_m is the maximum power of the individual load. Hence the total power obtained is $2P_m$ which is the maximum of total power.

C. Operating Modes

Different operating modes during the interval t_a are shown in Fig. 5. During this interval load-1 and load-2 are powered as shown in Fig. 3.

1) Mode-1: During this mode of operation, S_m, S_2 and S_3 are conducting. Load-1 is powered through S_m, S_2 and S_3. Load-1 current is positive. Load-2 current freewheels through switch S_2. Now $V_{L1} = V_{dc}$ & $V_{L2} = V_{L3} = 0$. Fig. 6(a) shows the equivalent circuit during this operation.

2) Mode-2: S_2 is turned OFF. S_m and S_3 are conducting. S_1 is in OFF-state. Load-1 current discharges C_1 and then freewheels through D_1. Load-2 current is negative as shown in Fig. 6(b). Now $V_{L1} = V_{L3} = 0$ & $V_{L2} = V_{dc}$.

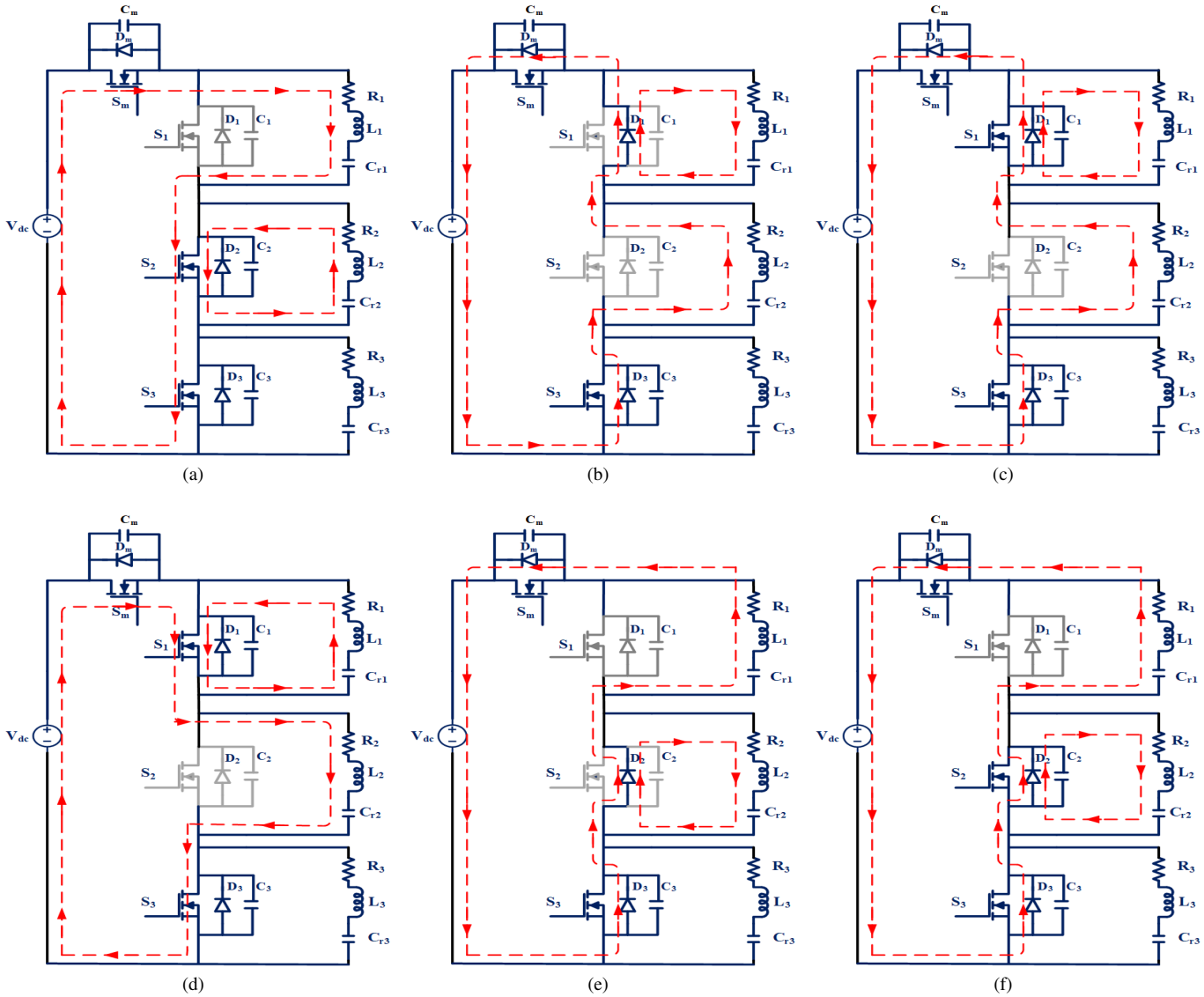


Fig. 6. Modes of operation (a) Mode-1 (b) Mode-2 (c) Mode-3 (d) Mode-4 (e) Mode-5 (f) Mode-6.

3) Mode-3: S_m and S_3 are conducting. S_1 is turned ON with ZVS. Load-1 current freewheels through D_1. Load-2 current is negative and flows through D_1, D_m and D_3. $V_{L1} = V_{L3} = 0$ & $V_{L2} = V_{dc}$. Fig. 6(c) shows the equivalent circuit during this operation.

4) Mode-4: S_m, S_1 and S_3 are conducting. Load-1 current is negative and flows through S_1. Load-2 current is positive and this load is powered through devices S_m, S_1 and S_3. C_2 is charged to $+V_{dc}$. $V_{L1} = V_{L3} = 0$ & $V_{L2} = V_{dc}$. Fig. 6(d) shows the equivalent circuit during this operation.

5) Mode-5: S_1 turns OFF and S_2 is in OFF-state. S_m and S_3 are conducting. Load-1 current is negative. Load-2 current is positive and it discharges C_2 and then freewheels through D_2. Now $V_{L1} = V_{dc}$ & $V_{L2} = V_{L3} = 0$. Fig. 6(e) shows the equivalent circuit during this operation.

6) Mode-6: S_2 turns ON with ZVS. S_m and S_3 are conducting. Load-1 current is negative and flows through D_m, D_2 and D_3. Load-2 current freewheels through D_2. Now $V_{L1} = V_{dc}$ & $V_{L2} = V_{L3} = 0$. Fig. 6(f) shows the equivalent circuit during this operation.

Similarly, during interval t_b load-2 and load-3 are powered. The device S_1 and S_m are ON. S_2 and S_3 are operated at high frequency. Similar operation exists for this interval. This operation also consists of six different modes. During interval t_c, load-1 and load-3 are powered. The device S_2 and S_m are ON. S_1 and S_3 are operated at high frequency. Similar operation exist for this interval. This operation also consists of six different modes. During interval t_m, no load is powered. At this instant, S_m is OFF and S_1, S_2, S_3 are ON.

III. Design Aspects and Output Power Control

A. Measurement of Load Parameters and Frequency Selection for Switching

For IH applications, the f_{sw} is chosen above 20 kHz. The vessel with inductor coil is modeled as a series combination of equivalent resistance (R) and equivalent inductance (L). These

parameters are measured at the switching frequency with an NumetriQ PSM1735 LCR meter which is presented in Table I. The load parameters are $R_1 = R_2 = R_3 = 7.4\ \Omega$, $L_1 = L_2 = L_3 = 79.1$ H, $C_{r1} = C_{r2} = C_{r3} = 0.2\ \mu$F. The f_{sw} is selected to be 43 kHz which has to be slightly greater than f_r in order to obtain ZVS. Hence, f_r is selected to be 40 kHz. The corresponding resonant capacitor C_r is obtained from Equation (2).

B. Selection of switching device

Switching devices must be able to block the maximum voltage and handle high currents. Hence, the proposed inverter uses a 250 V, 44 A MOSFET with a Rds_{on} of 38 mΩ.

C. Design of Snubber

ZVS can be achieved by operating the inverter at a frequency slightly greater than f_r during the turn-ON transition. Switching loss during turn-OFF can be eliminated using snubber capacitors across the devices. To ensure correct charging and discharging of snubber capacitors, dead-time is provided between device switching. Snubber capacitance C_s can be obtained as

$$C_s \geq \frac{t_d.\ i_{soff}}{V_{dc}} \tag{4}$$

Where t_d is the dead time, i_{soff} is the maximum turn-off current of the switches.

D. Output power control

The proposed inverter configuration employs cyclic ON and OFF control approach to power any two loads at a time. T_L is the total time period for one cycle. This period is divided into four-time intervals t_a, t_b, t_c and t_m. Hence $T_L = t_a + t_b + t_c + t_m$. The powering duration of each load is expressed as

$$\left.\begin{aligned} &\text{Total time that load-1 is powered} = (t_a + t_c)\\ &\text{Total time that load-2 is powered} = (t_a + t_b)\\ &\text{Total time that load-3 is powered} = (t_b + t_c) \end{aligned}\right\} \tag{5}$$

The average load powers can be expressed as

$$\left.\begin{aligned} P_{Load-1} &= \frac{(t_a + t_c)}{T_L} P_m = d_1 P_m\\ P_{Load-2} &= \frac{(t_a + t_b)}{T_L} P_m = d_2 P_m\\ P_{Load-3} &= \frac{(t_b + t_c)}{T_L} P_m = d_3 P_m\\ &\text{Load power during } t_m = P_{Lm} = 0 \end{aligned}\right\} \tag{6}$$

Hence, the total power

$$\left.\begin{aligned} &= P_{Load-1} + P_{Load-2} + P_{Load-3} + P_{Lm}\\ &= d_1 P_m + d_2 P_m + d_3 P_m + 0\\ &= \frac{2(t_a + t_b + t_c)}{T_L} P_m \end{aligned}\right\} \tag{7}$$

By solving Equation (6) and Equation (7) t_a, t_b, t_c and t_m are derived as

$$\left.\begin{aligned} t_a &= \frac{(P_{Load-1} + P_{Load-2} - P_{Load-3})}{2\frac{P_m}{T_L}}\\ t_b &= \frac{(P_{Load-2} + P_{Load-3} - P_{Load-1})}{2\frac{P_m}{T_L}}\\ t_c &= \frac{(P_{Load-3} + P_{Load-1} - P_{Load-2})}{2\frac{P_m}{T_L}}\\ t_m &= T_L - (t_a + t_b + t_c) \end{aligned}\right\} \tag{8}$$

Therefore, the operating times of t_a, t_b, t_c and t_m can be determined for the desired values of P_{Load-1}, P_{Load-2} and P_{Load-3}.

If we consider $P_{Load-1} = P_{Load-2} = P_{Load-3} = P_L$, then from Equation (7),

$$P_L = \frac{2}{3}\frac{(t_a + t_b + t_c)}{T_L} P_m \Bigg\} \tag{9}$$

Also for maximum output power,

$$\left.\begin{aligned} t_a &= t_b = t_c \text{ and } t_m = 0\\ &\text{Hence, } P_L = \frac{2}{3} P_m \end{aligned}\right\} \tag{10}$$

Therefore, when all loads are operated at equal powers under maximum output condition, each load power equals to $\frac{2}{3}P_m$.

IV. Simulation and Experimental Results

The proposed resonant inverter is simulated in PSIM software and hardware has been implemented. In Fig. 7 the experimental setup of the proposed system is shown. Table I displays the circuit parameters of the proposed inverter. The Spartan- 6 FPGA controller generate the gating signals. The experimental results are recorded using the Tektronix MDO3024.

TABLE I
Specifications of Proposed Inverter

Parameters	Values
Source voltage V_{dc}	120 V
Switching frequency f_{sw}	43 kHz
Resonant frequency f_r	40 kHz
Equivalent resistance of loads $R_1 = R_2 = R_3$	7.4 Ω
Equivalent inductance of loads $L_1 = L_2 = L_3$	79.1 µH
Resonant capacitor of loads $C_{r1} = C_{r2} = C_{r3}$	0.2 µF
Equivalent series resistance (r_{cr1}) of C_{r1}	16.5 mΩ
Equivalent series resistance (r_{cr2}) of C_{r2}	16.5 mΩ
Equivalent series resistance (r_{cr3}) of C_{r3}	16.5 mΩ
Parasitic resistance of load-1 (r_{f1}), load-2 (r_{f2}) and load-3 (r_{f3}) IH coils	190 mΩ
Cyclic control frequency, f_L	1 kHz
Snubber capacitor	1 nF, 300 V
Switching devices MOSFETs	IRFPB4229PbF

The simulation and experimental ZVS waveforms of S_1, S_2 and S_3 at equal duty cycles of $d_1 = d_2 = d_3 = 0.667$ are shown in Fig. 8. Fig. 9 shows simulation and experimental ZVS waveforms of S_1, S_2 and S_3 at different duty cycles of $d_1 = 0.5$, $d_2 = 0.5$ and $d_3 = 0.9$. It is observed that ZVS turn ON is obtained. Fig. 10 shows simulation and experimental

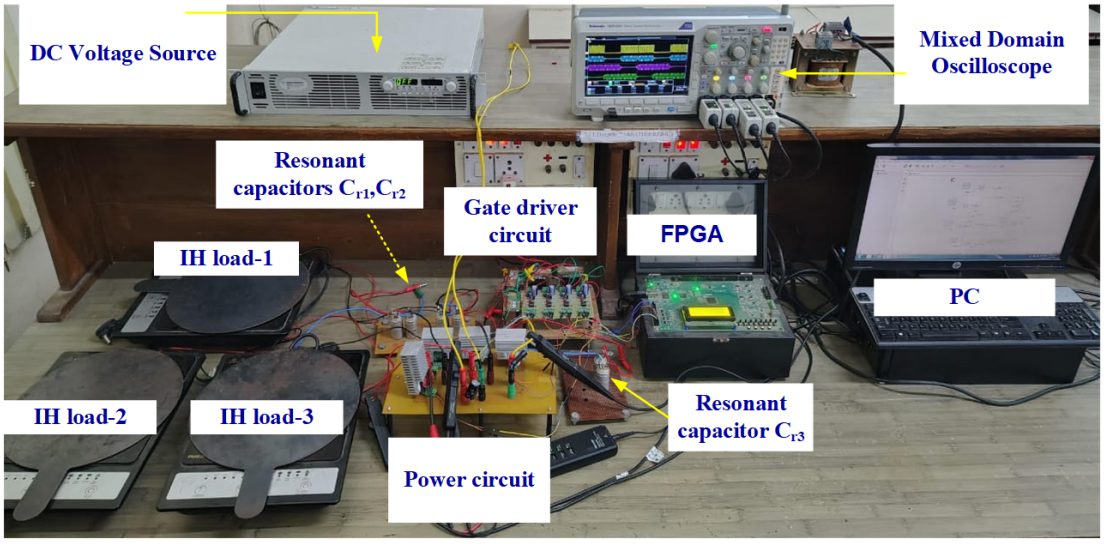


Fig. 7. Experimental prototype.

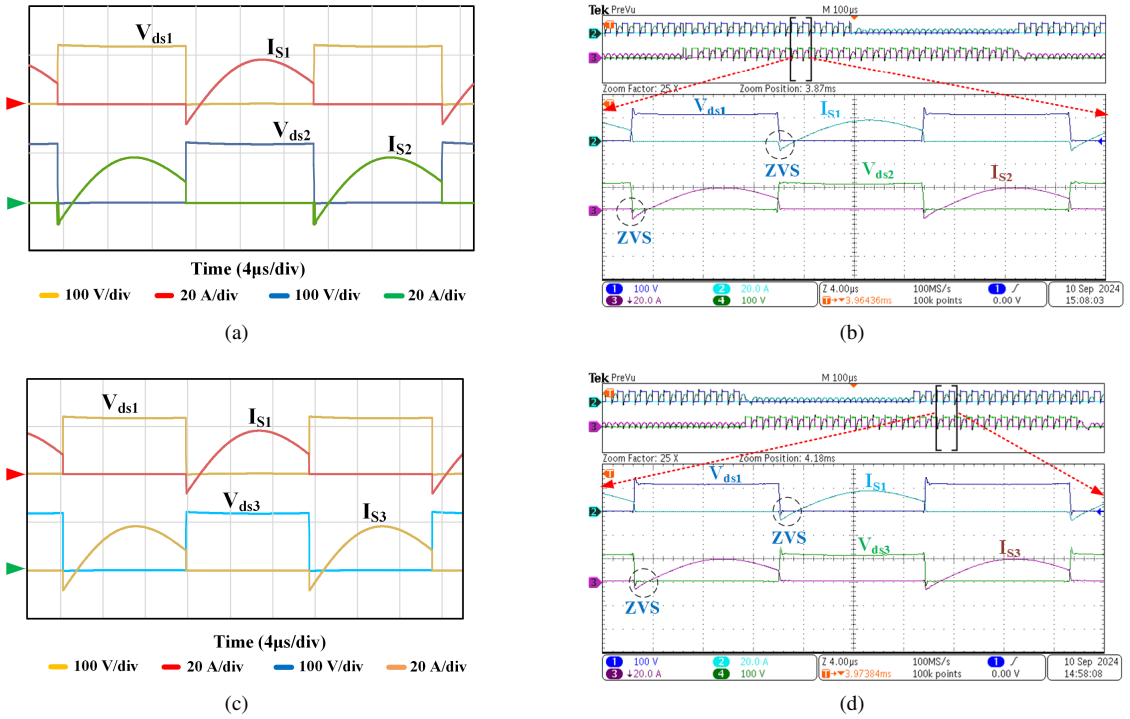
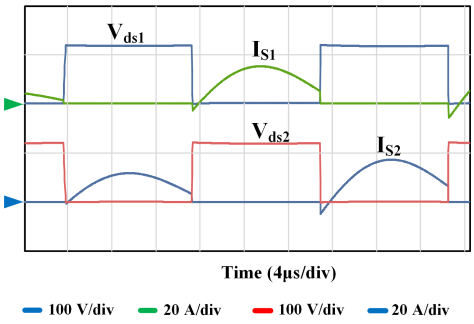


Fig. 8. ZVS waveforms at $d_1 = d_2 = d_3 = 0.667$: Voltages and currents for S_1 and S_2 (a) Simulation (b) Experimental; Voltages and currents for S_1 and S_3 (c) Simulation (d) Experimental.

waveforms of load-1 voltage and all load currents at equal duty cycles or maximum power condition of $d_1 = d_2 = d_3 = 0.667$. The experimental rms current flowing through load-1 is 5.17 A. Load-2 current is 5.4 A and load-3 current is 5.4 A. Fig. 11 shows simulation and experimental waveforms of load-1 voltage and all load currents at $d_1 = 0.5$, $d_2 = 0.5$ and $d_3 = 0.9$. The experimental rms current flowing through load-1 is 4.5 A. Load-2 current is 4.8 A and load-3 current is 6.28 A. Fig. 12 shows simulation and experimental voltages and currents of load-1, load-2 and load-3 at duty cycles of $d_1 = 0.2$, $d_2 = 0.5$ and $d_3 = 0.5$. The experimental rms current flowing through load-1 is 2.71 A, load-2 is 4.78 A and load-3 is 4.7 A. Fig. 13 shows simulation and experimental voltages and currents of load-1, load-2 and load-3 at duty cycles of $d_1 = 0.5$, $d_2 = 0.8$ and $d_3 = 0.5$. The experimental rms current flowing through load-1 is 4.56 A, load-2 is 6 A and load-3 is 4.63 A.

Fig. 14 shows graphs of output power versus duty cycle. In Fig. 14(a), d_1 varies while d_2 and d_3 remain constant. The output power P_{L1} varies, while P_{L2} and P_{L3} remain constant at $d_2 = d_3 = 0.5$. Similarly, in Fig. 14(b), When d_2 varies, d_1 and d_3 remains constant. The output power P_{L2} varies,



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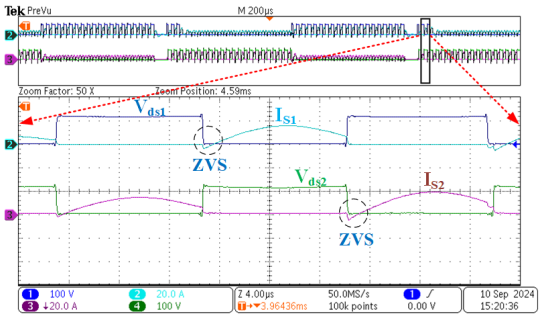

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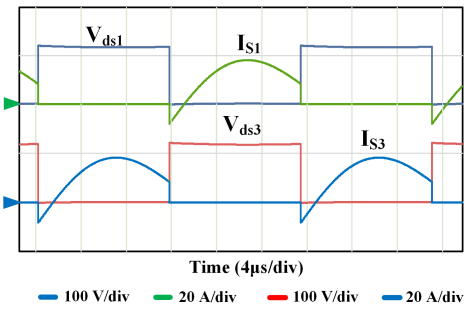

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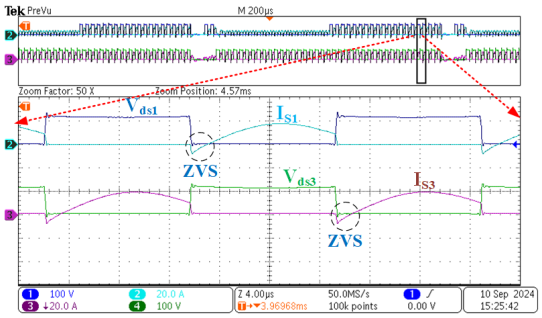
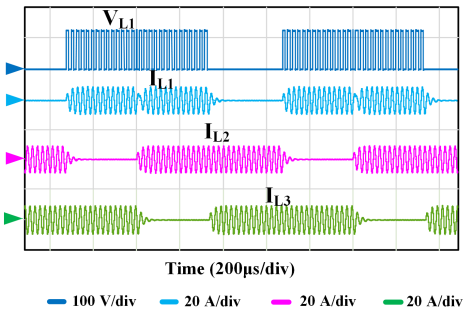
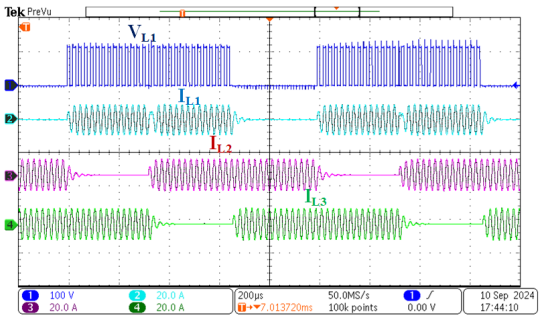


(d)

Fig. 9. ZVS waveforms at $d_1 = 0.5$, $d_2 = 0.5$, $d_3 = 0.9$: Voltages and currents for S_1 and S_2 (a) Simulation (b) Experimental; Voltages and currents for S_1 and S_3 (c) Simulation (d) Experimental.

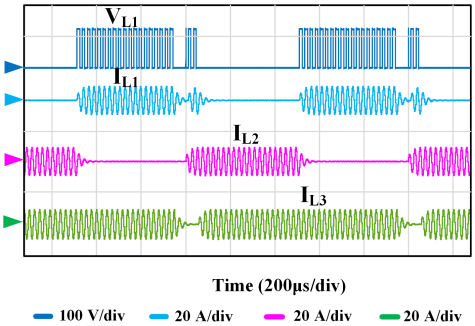


(a)

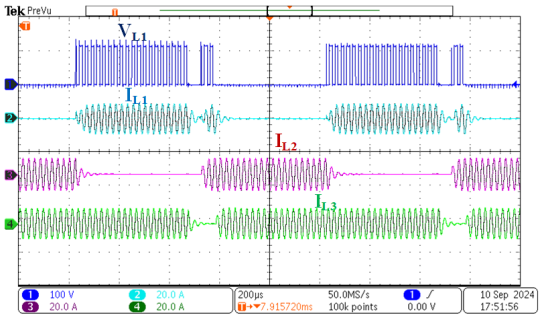


(b)

Fig. 10. Load-1 voltage and all load currents for $d_1 = d_2 = d_3 = 0.667$: (a) Simulation (b) Experimental.



(a)



(b)

Fig. 11. Load-1 voltage and all load currents for $d_1 = d_2 = 0.5$, $d_3 = 0.9$: (a) Simulation (b) Experimental.

while P_{L3}, P_{L1} remains constant at duty cycle $d_1 = d_3 = 0.5$. Fig. 14(c) shows that d_3 varies while d_1 and d_2 remain constant. Output power P_{L3} varies, while P_{L1}, P_{L2} remains constant at duty cycle $d_1 = d_2 = 0.5$. Fig. 15 shows variation

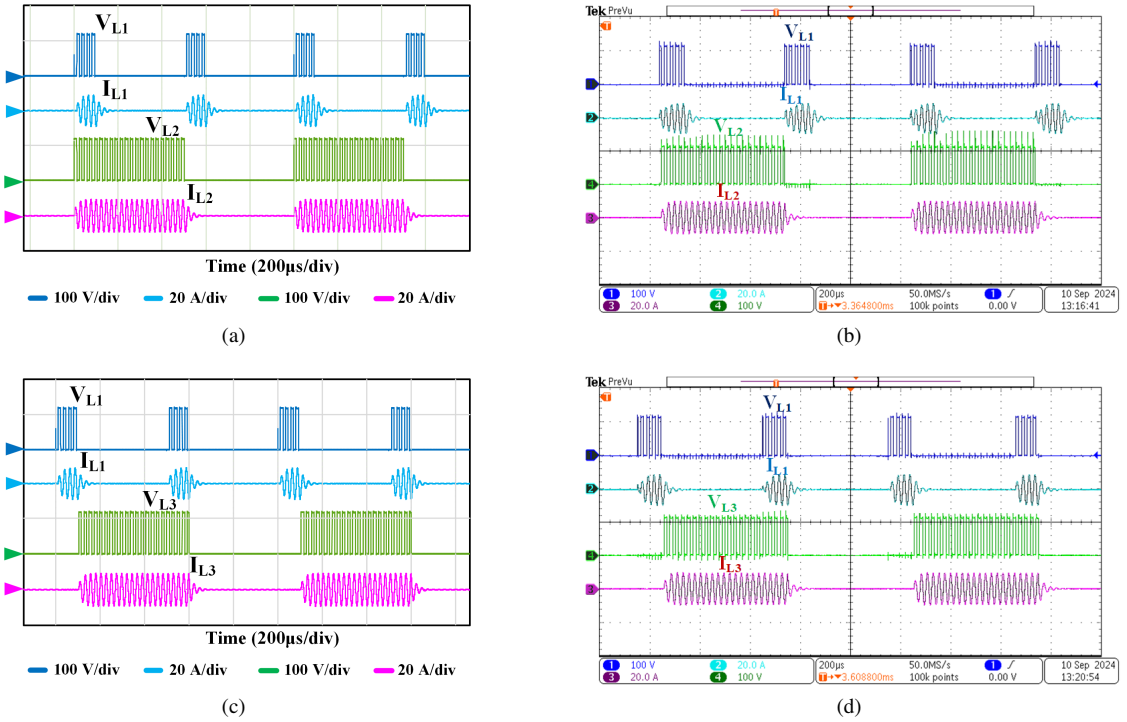


Fig. 12. Load voltages and currents at d_1 = 0.2, d_2 = 0.5, d_3 = 0.5: Load-1 and 2 voltages and currents (a) Simulation (b) Experimental; Load-1 and 3 voltages and currents (c) Simulation (d) Experimental.

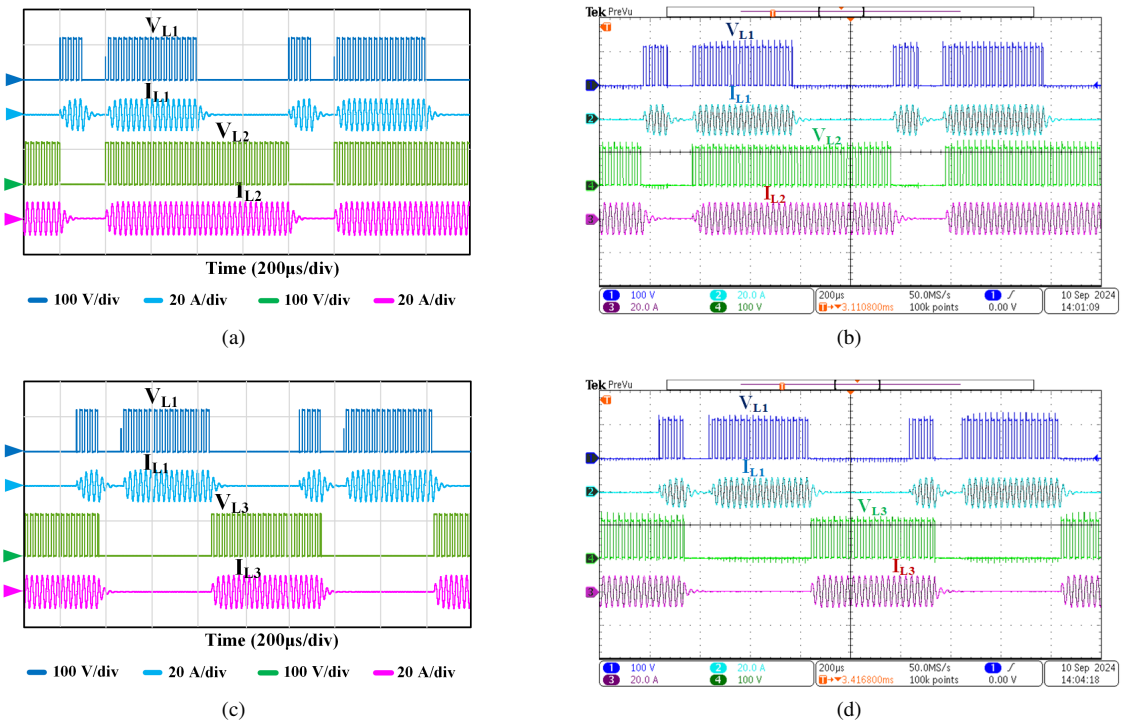
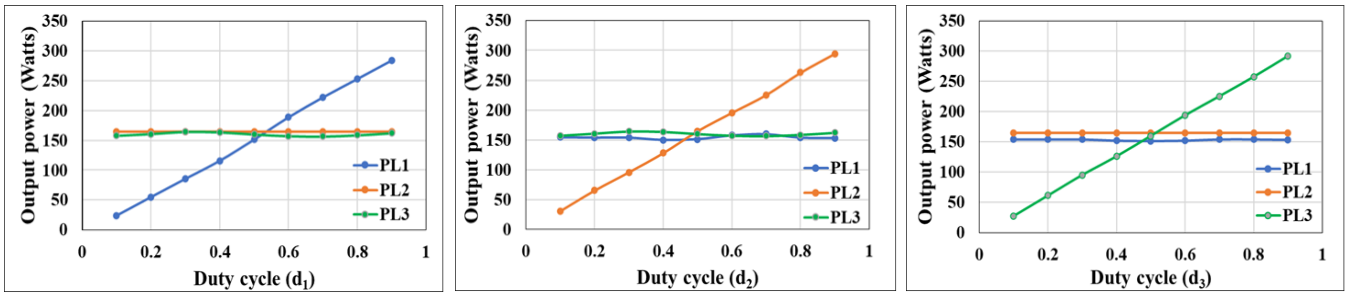


Fig. 13. Load voltages and currents at d_1 = 0.5, d_2 = 0.8, d_3 = 0.5: Load-1 and 2 voltages and currents (a) Simulation (b) Experimental; Load-1 and 3 voltages and currents (c) Simulation (d) Experimental.

of efficiency versus total output power graph. In Fig. 15(a), the output power P_{L1} is varied, while P_{L2} and P_{L3} are remained constant. In Fig. 15(b), P_{L2} is varied, while P_{L3} and P_{L1} are remained constant. Similarly, in Fig. 15(c), the P_{L3} is varied, while P_{L1} and P_{L2} are remained constant. The proposed inverter achieves a peak efficiency of 96.1%.



(a) (b) (c)

Fig. 14. Experimental graphs for independent power control (a) d_1 varying (b) d_2 varying (c) d_3 varying.

TABLE II
COMPARISON OF VARIOUS TOPOLOGIES FOR MULTI-LOAD IH APPLICATIONS

Reference	Total number of switches	Switching frequency (kHz)	Number of loads	Maximum Efficiency (%)	Independent control	Control technique used	Switch count to load ratio	No. of additional components required
[17]	3	25-40	2	96	Yes	-	1.5	4-diodes
[19]	4	30,150	2	92	Yes	ADC	2	0
[22]	4	20-100	2	98	NO	PDM	2	8-diodes
[23]	8	30	2	91	Yes	ON and OFF	4	0
[24]	6	30.5	3	95	Yes	ON and OFF	2	0
[32]	7	30	4	94.6	Yes	AVC, ON and OFF	1.75	2-diodes
[29]	6	30	3	95	No	PSC	2	0
[31]	6	30	2	93	Yes	PDM	3	0
[33]	6	30, 220	2	94.3	Yes	ON and OFF	3	2-diodes
[34]	3	28	2	96.3	Yes	ADC	1.5	2-capacitors
Proposed Topology	**4**	**43**	**3**	**96.1**	**Yes**	**ON and OFF**	**1.33**	**0**

A. Power Loss Analysis

Efficiency of any power converter is mainly affected by losses. Losses are divided into conduction and switching losses. Conduction losses include losses in MOSFETs, ESR of induction coil and capacitor. Switching losses occur in MOSFETs. Conduction losses depend on device currents and are independent of frequency. But switching losses are proportional to the operating frequency. Hence efficiency may affect by varying the switching frequency. At lower switching frequencies, the inverter efficiency is high. At higher switching frequencies, the inverter efficiency will be reduced.

Power loss analysis is conducted using PSIM software by developing thermal models of the switching devices listed in Table I, based on their respective datasheets. The simulation is performed under the same operating conditions as the experimental prototype. When the inverter operates at peak efficiency with a duty cycle of d_1 = 0.5, d_2 = 0.5 and d_3 = 0.1, it experiences a power loss of 13.79 W, corresponding to an efficiency of 96.1%. The detailed power loss distribution is illustrated in Fig. 16. The total switching power loss includes contributions from both the transistor and their body diode. Losses in the IH coil are attributed to its parasitic resistance, while power losses in the resonant capacitors result from their ESR. In the proposed inverter, the switching losses are relatively minimal when compared to conduction losses. This reduction is due to the ZVS achieved by the switching devices.

Conduction losses in resonant capacitors are given as

$$P_{cond,cr} = (I_{rms,cr})^2 \times r_{cr}$$
$$\left.\begin{aligned} P_{cond,cr1} &= 0.33W \\ P_{cond,cr2} &= 0.36W \\ P_{cond,cr3} &= 0.05W \end{aligned}\right\} \quad (11)$$

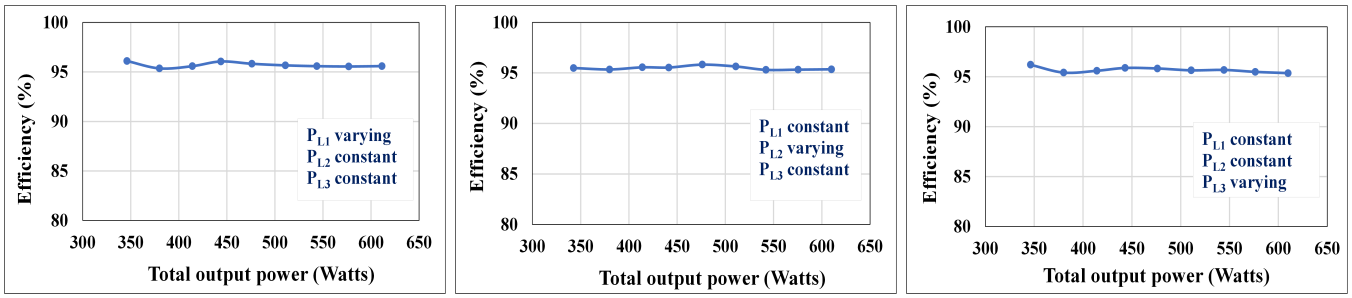
Total conduction losses in resonant capacitors = 0.74 W Where $I_{rms\ ,cr}$ denotes the rms current flowing through the resonant capacitor and r_{cr} denotes the ESR of the resonant capacitor.

Conduction losses in IH coil are expressed as

$$P_{cond,coil} = (I_{rms,coil})^2 \times r_f$$
$$\left.\begin{aligned} P_{cond,coil-1} &= 3.84W \\ P_{cond,coil-2} &= 4.19W \\ P_{cond,coil-3} &= 0.68W \end{aligned}\right\} \quad (12)$$

Total conduction losses in resonant capacitors = 8.71 W. Where, $I_{rms,coil}$ denotes the rms current flowing through the coil and r_f denotes the ESR of coil.

Conduction losses in the switches are expressed as



(a) (b) (c)

Fig. 15. Experimental graphs of efficiency vs total output power (a) d_1 varying (b) d_2 varying (c) d_3 varying.

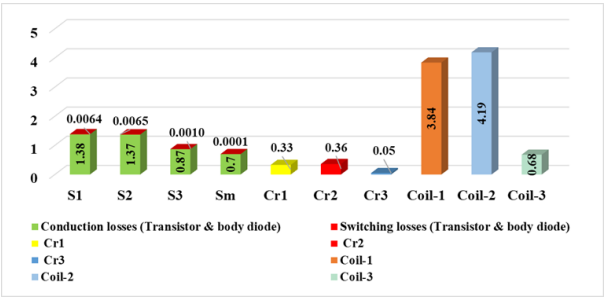
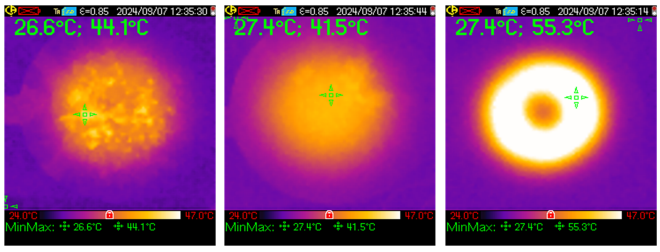


Fig. 16. Power loss diagram.



(a) (b) (c)

Fig. 17. Thermal images (a) load-1 (d_1) = 0.5 (b) load-2 (d_2) = 0.5 (c) load-3 (d_3) = 0.9.

$$P_{con,switch} = (I_S)^2 \times R_{dson}$$

$$\left.\begin{aligned} P_{cond,S1} &= 1.36W \\ P_{cond,S2} &= 1.36W \\ P_{cond,S3} &= 0.87W \\ P_{cond,Sm} &= 0.7W \end{aligned}\right\} \quad (13)$$

Total conduction losses in switches = 4.29 W
Where, I_S is the rms current flowing through the switch and R_{dson} is the drain-source resistance.

Switching losses in switch during turn-OFF is expressed as

$$P_{turn-off} = \tfrac{1}{2} f_{sw} V_{dsoff} I_{swoff} t_f$$

$$\left.\begin{aligned} P_{S1-off} &= 4.35mW \\ P_{S2-off} &= 4.5mW \\ P_{S3-off} &= 0.48mW \\ P_{Sm-off} &= 0.10mW \end{aligned}\right\} \quad (14)$$

Total switching losses in switch during turn-off transition = 9.43 mW
Where, f_{sw} is switching frequency, V_{dsoff} and I_{swoff} are drain source voltage and switch current at turn off instant respectively, t_f is the fall time of the switch.

Switching losses of body diode is expressed as

$$P_D = Q_{rr} f_{sw} V_{ds}$$

$$\left.\begin{aligned} P_{D1} &= 2.07mW \\ P_{D2} &= 2.04mW \\ P_{D3} &= 0.48mW \\ P_{Dm} &= 0.0154mW \end{aligned}\right\} \quad (15)$$

Total switching losses of body diode = 4.6 mW
Where, Q_{rr} is reverse recovery charge, f_{sw} is switching frequency and V_{ds} is drain- source voltage during recovery.

Conduction losses of body diode is expressed as

$$P_{cond,\ body\ diode} = V_f I_{avg} D_{diode}$$

$$\left.\begin{aligned} P_{cond,D1} &= 28mW \\ P_{cond,D2} &= 14.9mW \\ P_{cond,D3} &= 3mW \\ P_{cond,Dm} &= 0.001mW \end{aligned}\right\} \quad (16)$$

Total conduction losses of body diode = 45 mW
Where, V_f is forward voltage drop of body diode, $I_{avg\ is}$ average current through the diode, D_{diode} is the duty cycle during which the diode conducts.

Total power losses = 13.79 W
Output power = I^2R

$$\left.\begin{aligned} P_{L1} &= 149.85W \\ P_{L2} &= 163.46W \\ P_{L3} &= 26.71W \end{aligned}\right\} \quad (17)$$

$$P_L = P_{L1} + P_{L2} + P_{L3} = 340.02W$$

Efficiency (%) = $\frac{P_L}{P_L + Total\ power\ losses} \times 100 = 96.1\%$

The thermal images of all loads are captured at duty cycle of d_1 = 0.5, d_2 = 0.5 and d_3 = 0.9 respectively are shown in Fig. 17. The proposed topology is compared with the existing topologies for multi-load IH applications presented in the literature. The detailed comparison is provided in Table

II and it is observed that proposed inverter offers superior performance with a efficiency of 96.1%, switch to load ratio of 1.33 and No. of additional components required is zero.

V. Conclusion

A resonant inverter-based IH system capable of powering three loads using an ON and OFF control technique is introduced in this paper. Two loads are powered at a time and independent power control is provided for all loads. The inverter is designed to ensure soft switching over a wide range of output power, which minimizes switching losses. The inverter configuration uses only four switching devices to power three IH loads, resulting in a simplified design with a reduced component count. The inverter achieves a peak efficiency of 96.1%. Experimental results validate the effectiveness of the proposed inverter, and its ability to maintain high efficiency and independent power control. This configuration can be easily extended for a greater number of IH loads with additional inverter legs.

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